

Recent results with HV-CMOS and planar sensors for the CLIC vertex detector

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Abstract

The physics aims for the future multi-TeV e^+e^- Compact Linear Collider (CLIC) impose high precision requirements on the vertex detector which has to match the experimental conditions, such as the time structure of the collisions and the presence of beam-induced backgrounds. The principal challenges are: a point resolution of $3 \mu m$, 10 ns time stamping capabilities, low mass ($\sim 0.2\%$ X₀ per layer), low power dissipation and pulsed power operation. Recent results of test beam measurements and GEANT4 simulations for assemblies with Timepix3 ASICs and thin active-edge sensors are presented. The 65 nm CLICpix readout ASIC with 25 μ m pitch was bump bonded to planar silicon sensors and also capacitively coupled through a thin layer of glue to active HV-CMOS sensors. Test beam results for these two hybridisation concepts are presented.

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The physics aims for the future multi-TeV e^+e^- Compact Linear Collider (CLIC) impose high precision requirements on the vertex detector which has to match the experimental conditions, such as the time structure of the collisions and the presence of beam-induced backgrounds. The principal challenges are: a point resolution of $3 \mu m$, 10 ns time stamping capabilities, low mass $(\sim 0.2\%$ X₀ per layer), low power dissipation and pulsed power operation. Recent results of test beam measurements and Geant⁴ simulations for assemblies with Timepix3 ASICs and thin active-edge sensors are presented. The 65 nm CLICpix readout ASIC with 25 μ m pitch was bump bonded to planar silicon sensors and also capacitively coupled through a thin layer of glue to active HV-CMOS sensors. Test beam results for these two hybridisation concepts are presented.

Keywords: Silicon pixel vertex detector, Active edge sensors, Guard ring, HV-CMOS, CLICpix, Geant4 simulations

1. Introduction

The Compact Linear Collider (CLIC) [\[1\]](#page-5-0) concept for a future linear e^+e^- collider has the potential to complement the measurements done by the LHC experiments. With proposed centre-of-mass energies of 380 GeV, 1.5 TeV and 3 TeV and with instantaneous luminosity up to 6×10^{34} cm⁻² s⁻¹, it allows for high precision measurements of Standard Model physics and of new physics potentially discovered at the 13 TeV LHC. The precision physics requirements and experimental conditions set challenging demands for the vertex detector in terms of spatial resolution, material budget, timing resolution and efficient heat removal from sensors and readout. The CLIC vertex detector R&D programme studies different sensor technologies and takes into account constraints from mechanics, power delivery and cooling. The goal is to achieve a single-point resolution of $3 \mu m$ with $50 \mu m$ thick sensors coupled to $50 \mu m$ thick readout ASICs with 25 µm pixel pitch.

The feasibility of thin sensors for operation for the CLIC vertex detector is studied with the Timepix3 [\[2\]](#page-5-1) readout chips with a pixel size of 55 μ m. Test beam data for 50 μ m thick sensors is compared to Geant4-based [\[3\]](#page-5-2) simulations. The simulation is extrapolated for smaller pixels of $25 \mu m$, as presented in Section [2.1.](#page-2-0)

Different guard ring solutions for thin active-edge sensors and their test beam results are introduced in Section [2.2.](#page-2-1)

CLICpix $[4]$, a readout ASIC with $25 \mu m$ pixel pitch, is developed in 65 nm CMOS technology. CLICpix is either bump bonded to planar silicon sensors or capacitively coupled through a thin layer of glue to active sensors implemented in

a commercial 180 nm High-Voltage (HV) CMOS process [\[5\]](#page-5-4). Results of recent test beam measurements for these two hybridisation concepts are presented in Section [3.](#page-4-0)

2. Thin sensor studies with the Timepix3 readout ASIC

Thin n-in-p planar sensors with active edge produced by Advacam [\[6\]](#page-5-5), using a Deep Reactive Ion Etching (DRIE) process, are bump bonded to the Timepix3 readout chips $(55 \mu m)$ pixel pitch). The tested assemblies with $50 \mu m$ thick sensors are listed in Table [1.](#page-1-0) They are studied in test beams and compared with simulations.

Table 1: Advacam active-edge n-in-p planar pixel sensor assemblies. The sensors are $50 \mu m$ thick. The edge distance is defined by the distance between the last pixel implant and the physical sensor edge.

Assembly	Edge distance $[\mu m]$	Guard ring type
$20-NGR$	20	No guard ring
$23-FGR$	23	Floating guard ring
28-GNDGR	28	Grounded guard ring
55-GNDGR	55	Grounded guard ring

Active-edge sensors allow for seamless tiling of pixel sensors of a vertex detector by depleting the sensors up to their physical edges. This allows for high coverage without creating overlaps between the pixel sensors and therefore reduces the material. consists of extending the backside implantation to the Figure [1](#page-2-2) illustrates a cross section of an active-edge sensor. The backside implantation, as well as the bias voltage, is extended to the edge of the sensor. The gradient of potential between the edge and the last pixel can be very high and could lead to a breakdown of the sensor. A guard ring consists of an n-implant with a metallic contact on top of it surrounding the pixel matrix close to the edge and thereby smoothening the potential transition between the edge and the neighbouring pixels. The guard ring can

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be kept floating or grounded by connecting it to the ground potential of the readout ASIC. Timepix3 ASICs provide an extra row of bumped pixels allowing to connect the guard ring to the ground potential.

Figure 1: Schematic showing the cross section of a sensor with active-edge technology and a guard ring in the edge. The electric field distribution is illustrated.

Figure [2](#page-2-3) shows the measured leakage current in the different assemblies as a function of the bias voltage. The breakdown occurs earlier for the assembly without guard ring (20-NGR) compared to the other assemblies. For the nominal operation at -15 V, none of the assemblies reach the breakdown leakage current.

Figure 2: Measured leakage current as a function of bias voltage for the assemblies listed in Table [1.](#page-1-0)

The assemblies were tested at the CERN SPS with 120 GeV pions, making use of a beam reference telescope. The telescope, as shown in Figure [3a,](#page-2-4) is made of 6 planes of Timepix3 ASICs bump bonded to 300 µm thick p-in-n planar sensors. The planes are rotated by 9° around the x axis (perpendicular to the beam axis) and the z axis (parallel to the beam axis) to optimise the charge sharing within the sensors and obtain a pointing resolution of \sim 2 μ m on the device under test (DUT).

2.1. Sensor performance

The cluster-size distribution and the hit residuals for $50 \mu m$ thick sensors are investigated in data and simulation. The simulation of the test beam setup is done using the Geant4-based

package AllPix [\[7\]](#page-5-6). The test beam simulation geometry is shown in Figure [3b.](#page-2-4) Digitisers for the telescope planes and the DUT take into account the semiconductor physics, drift, diffusion, charge sharing in the planar sensors and also noise in the readout ASICs.

Figure 3: (a) The Timepix3 telescope and (b) its GEANT4-based simulation model.

The cluster-size distribution and the hit residuals for the DUT operating at a threshold of $~500$ electrons are shown in Fig-ure [4.](#page-2-5) The track resolution of \sim 2 μ m is not unfolded. For $50 \mu m$ thick sensors, the large fraction of single-pixel clusters contributes to the wide component of the residual distribution. The narrow component of the residual distribution is obtained by multi-pixel clusters where the charge sharing information is used to improve the hit reconstruction. The simulation is in good agreement with the data.

Figure 4: (a) Cluster-size distribution and (b) hit residuals in x-direction in a 50 µm thick planar sensor bump bonded to a Timepix3 ASIC with 55 µm pitch.

Figure [5](#page-3-0) shows the cluster-size distribution and the hit residuals for an extrapolation of the simulation to $25 \mu m$ pitch pixels with $50 \mu m$ thick sensors with a Timepix3-type readout chip operated at 500 electrons threshold with 10-bit TOT measurement and an electronic noise of \sim 90 electrons. The same digitiser as the one used to validate the simulation in Figure [4](#page-2-5) is used for the extrapolation. Even with a small pitch, in such thin sensors, only \sim 16% of clusters originating from minimum ionising particles contain more than one pixel. The residual distribution is therefore dominated by the broad peak from single-pixel clusters and the resulting resolution of $~6 \mu m$ is still significantly worse than the required $3 \mu m$.

2.2. Edge performance

The performance of active edge solutions with different guard ring layouts for thin sensors are presented in this section. Fig-

Figure 5: (a) Cluster-size distribution and (b) hit residuals in x-direction for the extrapolation of the simulation to 25 µm pixel pitch with a 50 µm thick sensor and a threshold of $~500$ electrons.

ure [6](#page-3-1) shows the layout of the assemblies listed in Table [1.](#page-1-0)

Figure 6: Sensor layouts for different guard-ring solutions for the assemblies described in Table [1.](#page-1-0) (a) shows the convention used in Figures [7,](#page-3-2) [8,](#page-3-3) [9](#page-3-4) and [10](#page-4-1) to express the efficiency and the charge distribution at the edge as a function of the track position. The border of the last pixel before the edge is indicated by a dashed line (at position 0 mm) and the physical sensor edge with a continuous line. The edge distance is defined by the distance between the last pixel implant and the physical sensor edge.

The efficiency and the collected charge (time-over-threshold TOT) on the edge as a function of the track position are shown in Figures [7,](#page-3-2) [8,](#page-3-3) [9](#page-3-4) and [10](#page-4-1) with the convention as illustrated in Figure [6a.](#page-3-1) The border of the last pixel (at 0 mm) is indicated with a dashed line and the physical sensor edge is shown in continuous line. The detection efficiency is calculated by counting the number of matched tracks to hits on the DUT divided by the total number of tracks projected on the DUT. The efficiency within the pixels is then mapped into a grid of 2×2 pixels. The x-axis shows the track position relative to the last pixel. The y-axis combines the tracks for the even rows (in the coordinates between 0 mm and 0.055 mm) and the odd rows (in the coordinates between 0.055 mm and 0.11 mm). The z-axis shows the efficiency. To increase the statistics, the beam was focused on only one of the edges during the data taking.

The assemblies without (Figure [7\)](#page-3-2) and with floating guard ring (Figure [8\)](#page-3-3) are efficient up to the physical edge of the sensor. The charge is fully collected by the last pixel for 20-NGR. For

23-FGR, a loss of the charge near the edge is observed (charge lost in the guard ring).

Figure 7: (a) Efficiency and (b) charge (TOT) collected as a function of the track position for the assembly 20-NGR.

Figure 8: (a) Efficiency and (b) charge (TOT) collected as a function of the track position for the assembly 23-FGR.

The grounded guard ring degrades significantly the detection efficiency at the edge. For 28-GNDGR, the efficiency drops between pixels as shown in Figure [9.](#page-3-4) A large part of the charge is collected by the guard ring. For 55-GNDGR, as shown in Figure [10,](#page-4-1) the edge is not efficient anymore due to the reduced amount of detected charge in thin sensors and its low sharing to the neighbouring pixels (lower than the threshold of the readout chip). All of the charge created in the edge is collected by the guard ring.

Figure 9: (a) Efficiency and (b) charge (TOT) collected as a function of the track position for the assembly 28-GNDGR.

For thin sensors, a floating guard ring appears to be the most suitable solution, as it shows a high detection efficiency at the

Figure 10: (a) Efficiency and (b) charge (TOT) collected as a function of the track position for the assembly 55-GNDGR.

edge and an acceptable breakdown behaviour (Figure [2\)](#page-2-3). Tests with additional assemblies will be needed to confirm this observation.

3. CLICpix readout ASIC

CLICpix is a pixel detector ASIC demonstrator developed for the CLIC vertex detector. It is designed in a commercial 65 nm CMOS process with a pixel pitch of $25 \mu m$ and the ability of simultaneous 4-bit energy (time-over-threshold TOT) and time (time-of-arrival TOA) measurements (<10 ns hit-time resolution). The demonstrator chip consists of a matrix of 64×64 pixels and was tested with $200 \mu m$ thick n-in-p planar sensors as well as active HV-CMOS sensors capacitively coupled through a thin layer of glue.

3.1. CLICpix and planar sensors

A single-chip indium bump bonding process for $25 \mu m$ pitch has been developed at SLAC [\[8\]](#page-5-7). 200 μ m thick n-in-p planar sensors have been bump bonded to CLICpix readout ASICs. Beam tests were carried out with the EUDET/AIDA telescope [\[9\]](#page-5-8) at the CERN SPS. Figure [11](#page-4-2) shows the average signal of the pixel with the highest charge (the leading pixel) in a cluster as a function of the track position for one of the assemblies. In this Figure, unconnected (1.8%), dead (0.3%) and shorted (1.0%) pixels can be seen. For shorted pixels, less charge can be detected by each pixel since the charge is shared equally. Missing solder connections caused the unconnected channels. A detection efficiency of greater than 99% was observed when excluding unconnected, dead and shorted pixels.

3.2. CLICpix and HV-CMOS active sensors

A capacitively coupled pixel detector (CCPDv3) implemented in a commercial 180 nm High-Voltage (HV) CMOS process is used as active sensor with integrated amplification. The CCPDv3 chip is capacitively coupled from its amplifier output to the CLICpix readout ASIC through a thin layer of glue. Figure [12](#page-4-3) shows a cross-section of the device and the glue between the sensor and CLICpix.

The CCPDv3 is biased at -60 V, resulting in a depletion layer below the charge collecting electrode with fast signal collection through drift. The tested assemblies show a high single-hit

Figure 11: Average signal of the pixel with the highest charge in a cluster as a function of the track intercept position on the planar sensor bump bonded to CLICpix.

Figure 12: Cross-section of a CCPDv3-CLIC pix assembly taken with an optical microscope [\[5\]](#page-5-4).

detection efficiency even for low bias voltages, as shown in Figure [13.](#page-4-4) For the nominal operation threshold of 1200 electrons, the efficiency is better than 99.9%. The spatial resolution is not sensitive to the applied bias voltage and is $~6 \mu m$ after subtraction of the track resolution [\[5\]](#page-5-4).

Figure 13: Hit-detection efficiency as a function of the bias voltage with a threshold of \sim 1200 electrons [\[5\]](#page-5-4).

4. Conclusions

The R&D on sensor and readout ASICs for the CLIC vertex detector addresses the requirements by performing measurements and simulations for a variety of thin planar sensor assemblies hybridised to the Timepix3 readout ASICs. Different guardring solutions for thin active-edge sensors are under study. The 25 µm pitch CLICpix readout ASIC demonstrator was tested successfully with planar and active HV-CMOS sensors. The results of the R&D gradually approach the challenging CLIC vertex detector requirements.

References

- [1] L. Linssen, et al., Physics and Detectors at CLIC: CLIC Conceptual Design Report, [CERN-2012-003](https://cds.cern.ch/record/1425915) (2012).
- [2] T. Poikela, et al., Timepix3: a 65k channel hybrid pixel readout chip with simultaneous toa/tot and sparse readout, [Journal of Instrumentation](http://stacks.iop.org/1748-0221/9/i=05/a=C05013) 9 (05) C05013.
- [3] S. Agostinelli, et al., GEANT4 – a simulation toolkit, Nucl. Instrum. Methods Phys. Res., Sect. A 506 (3) (2003) 250–303.
- [4] P. Valerio, et al., Design of the 65 nm clicpix demonstrator chip, [LCD-](https://cds.cern.ch/record/1507691)[Note-2012-018](https://cds.cern.ch/record/1507691) (2012).
- [5] N. Alipour Tehrani, et al., Capacitively coupled hybrid pixel assemblies for the CLIC vertex detector, [CLICdp-Pub-2015-003](https://cds.cern.ch/record/2048684) (2015).
- [6] X. Wu, et al., Recent advances in processing and characterization of edgeless detectors, [Journal of Instrumentation](http://stacks.iop.org/1748-0221/7/i=02/a=C02001) 7 (02) C02001.
- [7] [Allpix.](https://github.com/ALLPix/allpix)
- URL <https://github.com/ALLPix/allpix>
- [8] A. Tomada, C. Kenney, SLAC private communication (2015).
- [9] I. Rubinskiy, An eudet/aida pixel beam telescope for detector development, Physics Procedia 37, proceedings of the 2nd International Conference on Technology and Instrumentation in Particle Physics (TIPP 2011).