UPGRADE AND OPERATION OF THE DEMONSTRATION 4GS/SEC. INTRA-BUNCH INSTABILITY CONTROL SYSTEM FOR THE SPS *

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Abstract

We present the expanded system implementation and operational experience details for the "Demo" technology platform commissioned at the SPS in January 2015. The system has been expanded during the LS1 shutdown with added features. The upgraded system has enhanced performance and more robust synchronization to the beam and accelerator timing system. Central to the new features are 1 GHz bandwidth kickers and RF amplifiers (including associated equalizers) which allow excitation and control of higher modes within the 2 ns bunch. We highlight the expanded features, and present their details.

BACKGROUND

Following the success of the initial run of the CERN LHC, the LHC injector complex is being upgraded to provide higher intensity and brightness beams to enable the discovery of new physics. As part of the LHC Injectors Upgrade (LIU) project, the entire injector chain from Linac4 to the SPS is being upgraded [1]. One performance limitation in the SPS is the formation of transverse vertical intra-bunch instabilities due to electron cloud instability (ECI) and transverse mode coupled bunch instability (TMCI) effects. These effects limit the intensity of the beam injected into the LHC.

A collaborative research and development project to mitigate these intra-bunch instabilities involving simulation and modelling [2], hardware development and measurement efforts has been undertaken. One outcome of this work has been the development of a feedback control demonstration system. This demonstration system has provided encouraging results [3] in Machine Development (MD) studies at the SPS, undertaken during LHC Run1, just prior to Long Shutdown 1. The next step in the evolution of the demonstrator system is the upgrade of several key components.

OVERVIEW OF SYSTEM

The feedback demonstrator or demo system [4] consists of multiple components as shown in the diagram of Figure 1. Items targeted for upgrades are indicated here as well. Vertical beam displacement is sensed using a stripline BPM pickup structure and the Δ output of a hybrid is filtered, equalized and amplified by the analog front end. The analog signal is then digitized by the feedback processor, which is essentially a reconfigurable high speed digital signal processor. Sampling at 4GSa/s the system takes 16 samples across a single 4ns SPS injection bunch. We treat these 16 samples or slices independently and process each with a separate 16-tap FIR filter inside the processor. The FIR coefficients are the same for each slice. The filtered data is translated back into the analog domain by a 4GSa/s DAC. The converted analog signal is presented to the analog back end where it is filtered, equalized, amplified and split before being sent to the power amplifiers and finally to the kicker structure which applies a corrective field to the beam.

Additional components include the frequency multiplier which generates the 2GHz sample clock (both edges are used, giving 4GHz effectively) from the 200MHz SPS RF reference. And the excitation system which allows us to generate a perturbation signal onto the beam for driven motion studies. Finally, a set of adjustable delay lines are required to provide phase alignment of the timing of the beam arrival with the sampling operation at the pickup and the application of correction and excitation signals with beam in the kicker.

WORK TO DATE

The demo system platform in being upgraded in two phases as described in [5], [6]. Phase 1 upgrades include mitigation of ADC spectral lines driven by noise pickup and ground loops inside the feedback processor chassis. Improvements in the timing and synchronization of the reference and sampling clocks; and the migration of the excitation function to inside the feedback processor, allowing feedback and excitation signals to be summed digitally. Phase one upgrades have been completed, while phase 2 work is now underway. These include the expansion of processing beyond one bunch to handle 16 bunches. As well as the addition of an orbit offset compensation mechanism to dynamically remove the beam orbit offset, which limits the overall dynamic range of the system. Beyond these, some additional features and improvements have been and are being made to the feedback processor. Central to the effectiveness of the feedback system are the RF power amplifiers and kicker structure, which are also being upgraded.

UPGRADES

Feedback Processor

The feedback processor was built to initially process a single SPS bunch at injection. The system is being expanded to handle multiple bunches with processing occurring is a parallel, pipelined manner. The ADC snapshot memory currently uses internal FPGA SRAM limiting capture lengths to 32000 turns. An upgrade

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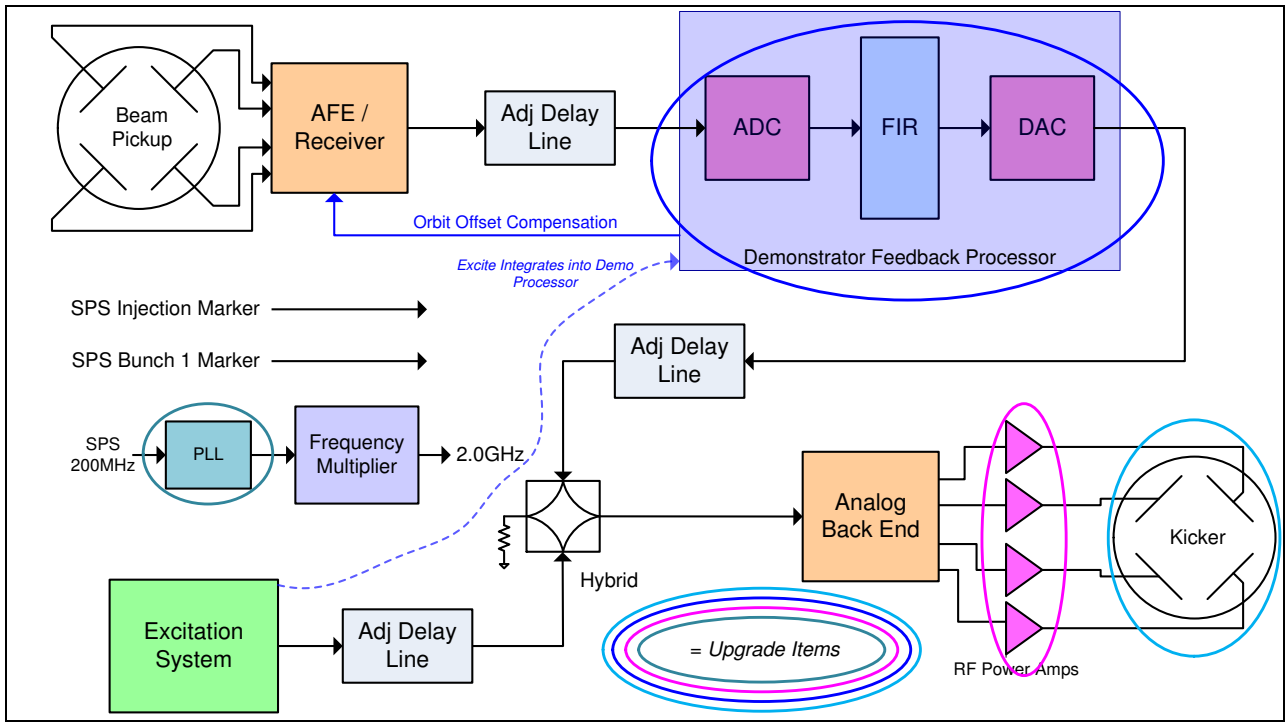

Figure 1: The Feedback Demonstrator System block diagram

to utilize the FPGA motherboard on-board DDR3 SDRAM will allow much longer captures. Along with this, a Gigabit Ethernet interface will be added to improve data transfer speed to and from the processor beyond the limitations of the current USB 2.0 interface. To support the SPS adjacent bucket fill scrubbing pattern, a special 32-sample processing mode was added that essentially processes two adjacent bunches. This development provides a path towards multibunch processing.

The 4GSa/s ADC is realized as two interleaved 2GSa/s devices. Each ADC has a reset input for its data clock divider logic. Reset synchronization between the two devices is critical and it was found that the original FPGA-based reset driver circuit would sometimes glitch, resulting in mis-interleaved ADC samples. An external reset driver circuit, synchronized to the 2GHz sample clock was added to resolve this issue.

Driven by simulation studies, expansion of the signal processing function beyond simple FIR structures is being investigated, including IIR and off-diagonal controllers. The flexibility of FPGA technology makes such implementations relatively easy to rapidly prototype, using the Xilinx DSP Simulink design tool. Finally, an automatic delay adjustment mechanism will be added to allow processing of the bunch over the full SPS acceleration ramp.

RF Power Amplifiers

The RF power amplifiers perform the crucial task of converting the small correction signal from the output of the DAC to one of significant power and high fidelity for application of the correction field to the beam. Requirements for our system dictated power levels of 100…500W with a frequency response between 10…1000MHz. The power amplifiers used initially suffered channel to channel amplitude mismatches as well as poor transient response. This latter characteristic is typically not well-defined for RF amplifiers. In evaluating possible candidates for better performance, a set of standardized frequency- and time-domain characterization tests were developed. An evaluation program led to the selection of amplifiers from R&K Company, Fuji-city, Japan. The unit chosen exhibited the best transient response behaviour which was even further improved by the company resulting in a semi-custom version. Figure 2 shows test results of the initial and improved versions of the amplifier. In this test, a single-cycle 200MHz sinewave burst at +4dBm was produced using an arbitrary waveform generator. Two of these amplifiers were installed at the SPS in March 2015 to drive the new stripline kicker structures.

Wideband Kicker

Of equal importance to the RF amplifiers is the structure that transfers the RF power in the form of an electromagnetic field onto the beam. The kicker used in initial studies was a tapered stripline structure with an overall bandwidth of 200MHz. This limited stability control to only lower order (0, 1) modes.

A design study was performed [7] to examine different implementations for a wideband (1GHz) kicker. Two designs were chosen, stripline and slotted waveguide, for further development. A prototype stripline kicker has been constructed and two instances were installed into SPS as of January 2015. The slotline

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design is in its final stages. A prototype is planned to be built in the late 2015 timeframe.

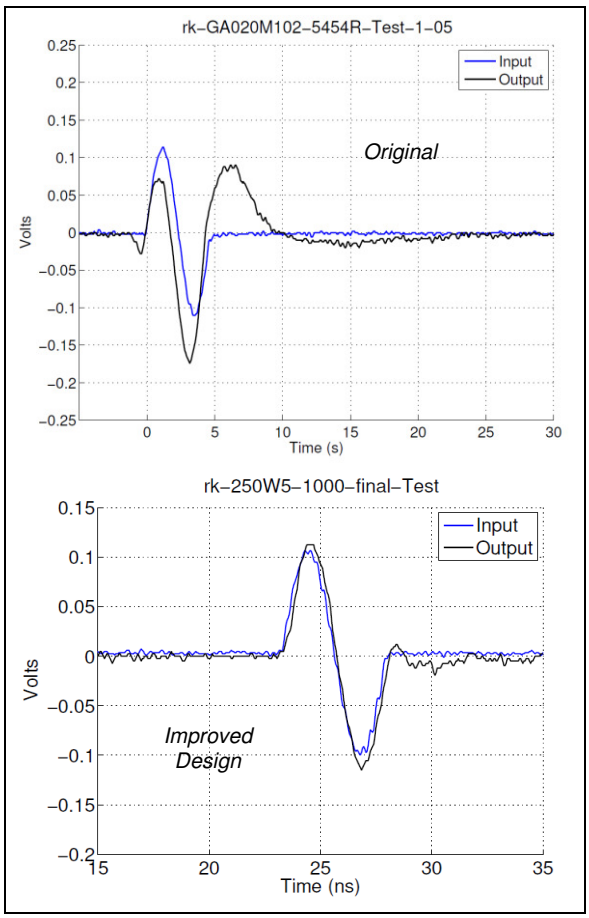

Figure 2: R&K RF Amplifier Transient Response

Timing PLL

The DAC in the feedback processor provides a divide-by-four dataclock for sampling the four parallel data streams fed to it, but offers no way of synchronizing this divide operation leading to phase shifts between power cycles. A Phase Locked Loop chassis was built to lock the SPS 200MHz reference phase to the DAC dataclock by means of servoing a phase shifter, ensuring consistent phase lock. This unit has been built and integrated into the system.

Output Equalizer

The system contains analog equalizers in the front and back ends to compensate for phase distortion introduced by the pickup, kicker and their respective cable plants. Because of the kicker upgrades, the back end equalizer needs to be re-designed to match the new kicker and cable plant characteristics. This work will be performed over the Summer of 2015.

OPERATIONAL EXPERIENCE

The phase 1 upgrades to the feedback chassis were completed and shipped to CERN along with the PLL chassis in the Fall of 2014. The system was integrated into the SPS and re-commissioned with just prior to the December 2014 technical stop. MD measurements from that time indicate feedback control of Mode 0 and 1 instabilities. Following the installation of the new amplifiers and stripline kickers, another MD in April 2015, will be carried out to characterize their performance.

TOWARDS AN 8GS/S ARCHITECTURE

In parallel with the ongoing development and upgrades of the feedback demonstration processor, a research and development effort is being made into increasing the input and output sampling rates of the system to 8GSa/s. This twofold increase provides more sample data, further reducing noise. It also provides a path for further explorations into different processing configurations including multiple pickups. Higher resolution sampling also provides more diagnostic capabilities, which would have accelerator applications beyond transverse feedback control.

Work done to date includes surveys into commercially available high-speed data converters, leading to the purchase of evaluation boards for selected devices. Characterization of the data converter performance is beginning, with the conclusion leading to the definition of the higher sampling rate system architecture. This architecture will merge with that of the demo system to produce the final full-featured prototype.

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