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1 MHz SAMPLING RATE 12-BIT LOW-POWER ANALOG-TO-DIGITAL CONVERTER FOR DATA PROCESSING IN PARTICLE DETECTORS

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Presented by F. Anghinolfi

A very low-power (12 mW), 1 MHz sampling rate 12-bit ADC circuit, using a commercial 3 μm CMOS process has been developed. This ADC component is well-adapted to use in front-end electronics for the readout of particle detectors in high-luminosity hadron colliders such as LHC or SSC. We discuss here the design options and report on the performance.

1. INTRODUCTION

In particle detector readout systems usually all analog detector signals pertaining to a triggered event are digitized in real time, and stored in temporary or mass memory for further information processing. In the proposed high-luminosity hadron colliders SSC and LHC, detectors will have to handle electronic signals coming at the crossing frequency of the beams, one crossing every 15 to 16 ns, on several millions of channels. The trigger decision time will be much longer than the event rate, thus the data from all channels will have to be buffered until trigger decisions are available for data selection and reduction. Real time digitization of all the signals for buffering in digital form would generate a large amount of raw data at the cost of very high-power consumption. An alternative approach, named Hierarchical Analog Readout Processor (HARP), has been proposed in 1988 [1]. It is based on the use of Very Large Scale Integration (VLSI) technologies to provide maximum electronic channel density, early data reduction and low power consumption. In the HARP system, data from each detector channel are stored in analog form and the digitization occurs only on a small fraction of the data selected by the first level trigger decision. The digitization is performed by the A/D converter at the output of the analog buffer and can therefore be done at a reduced speed of 100 kHz to 1 MHz. Various types of A/D converters running at these rates, based on pipeline methods, have recently been developed in CMOS technology, with medium-high resolutions and good linearity [2-4]. The implementation described here has the additional important feature of a very low-power consumption.

2. THE HARP ARCHITECTURE

The structure of the front–end data acquisition channel in the HARP architecture is shown in fig. 1. Charge or voltage signals from a detector element are sampled and, after amplification, stored as an analog signal at the speed of the beam bunch-crossing in an array of CMOS integrated capacitors. The data remain in the analog storage elements until the first-level trigger decision indicates if the information has to be transferred to the digitizer for further computation. The data reduction is equivalent to the rejection ratio of the first-level trigger, which may be 10^{-2} to 10^{-3}. The digitization is performed at a sampling rate of 100 kHz to 1 MHz with an A/D component using

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a small area of silicon and a pipeline conversion technique to achieve high resolution (10–12 bits) with a low-power consumption (10 mW range). Additional data reduction could be achieved by using a digital buffer after the A/D component which waits for the second-level trigger decision.

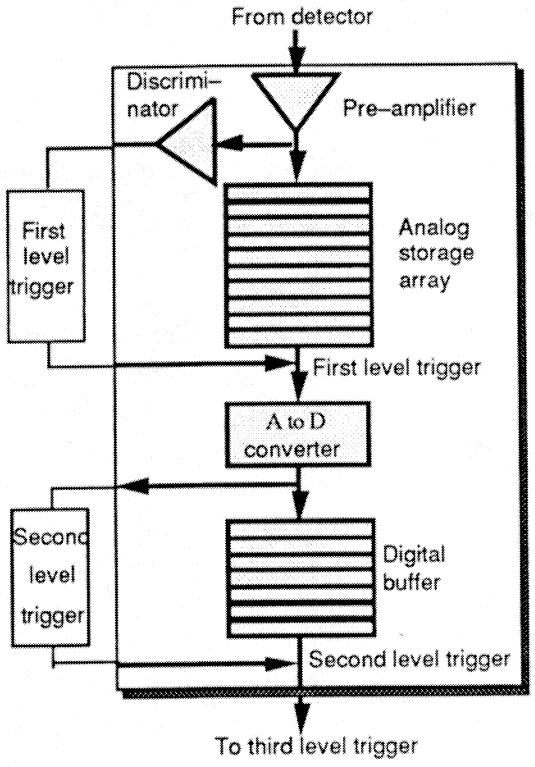

FIGURE 1
HARP schematic design, in which several components of a single readout channel are integrated on a single silicon chip.

With the high level of integration which is possible with modern CMOS VLSI technologies, several identical channels could be put on the same silicon chip, adding the benefit of excellent reproducibility of performance among channels. Through the use of rad-hard technologies, such low-power processors for on-board data reduction are eminently adapted to application in power-critical chips for the readout of detector systems inside the compact central region of collider experiments.

3. THE PIPELINE ADC DESIGN

3.1 Circuit principle

The basic idea of the pipeline analog-to-digital converter is to sample the analog voltage in a pipeline chain of 1-bit converter stages. For a n–bit pipeline A/D converter architecture [5], n – 1 identical stages are cascaded in front of the last simplified stage as is shown in the block diagram of fig. 2. Each stage, except the last one, consists of two principal components: a comparator to determine one bit of conversion; a multiplier and subtractor unit to determine the analog remainder voltage, called the residue, which has to be transferred to the following stage of the pipeline chain. The final stage consists only of a comparator, as there is no further need for a residue. Thus, within n–time steps, one sample of the input analog voltage and the subsequent residues are sequentially transferred through the successive stages. After the n–time steps, the n–bits of conversion for this sample are fully determined. In each time step, one new sample and n – 1 consecutive residues are simultaneously processed in the pipeline converter. In this way, the digital throughput rate of a pipeline converter is equal to its input sampling rate, with no dead-time between each sampling, as is characteristic of a flash A/D converter.

A simplified representation of a single stage is given in fig. 3. It consists of a voltage gain amplifier [6], and a positive feedback low–power comparator [7] with internal offset compensation. In the figure, A_{AB} represents a class AB CMOS inverter-amplifier [8] with a very good slew–rate characteristic. It uses less power and silicon area than a classical differential input amplifier.

Each stage performs in an identical way the two following operations: the comparison of its input voltage to half of the reference voltage ($V_R/2$); the sampling and multiplication by two of its input voltage, and the conditional subtraction of the reference voltage V_R, depending on the

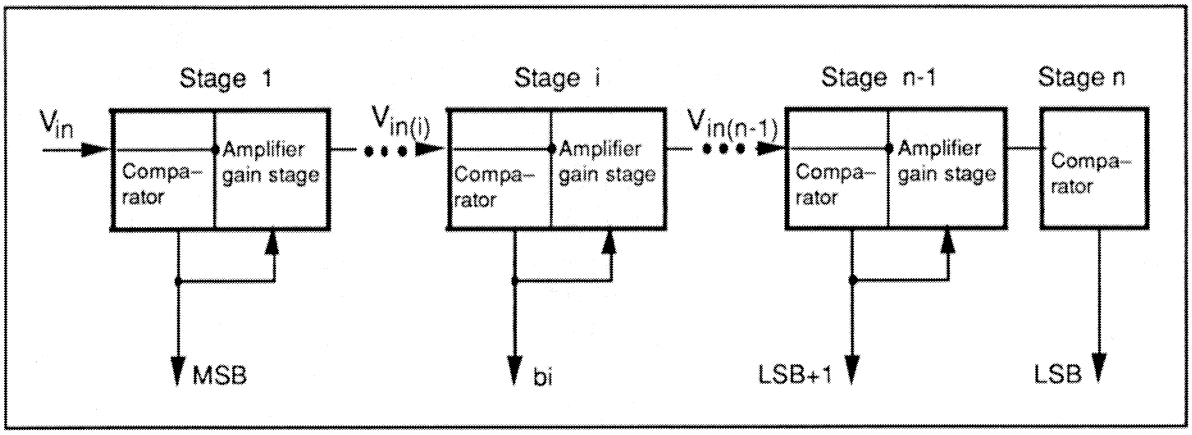

FIGURE 2
Block diagram of the n stages of the pipeline A/D converter. Stage 1 determines the value of the most significant bit (MSB), and stage n that of the least significant bit (LSB).

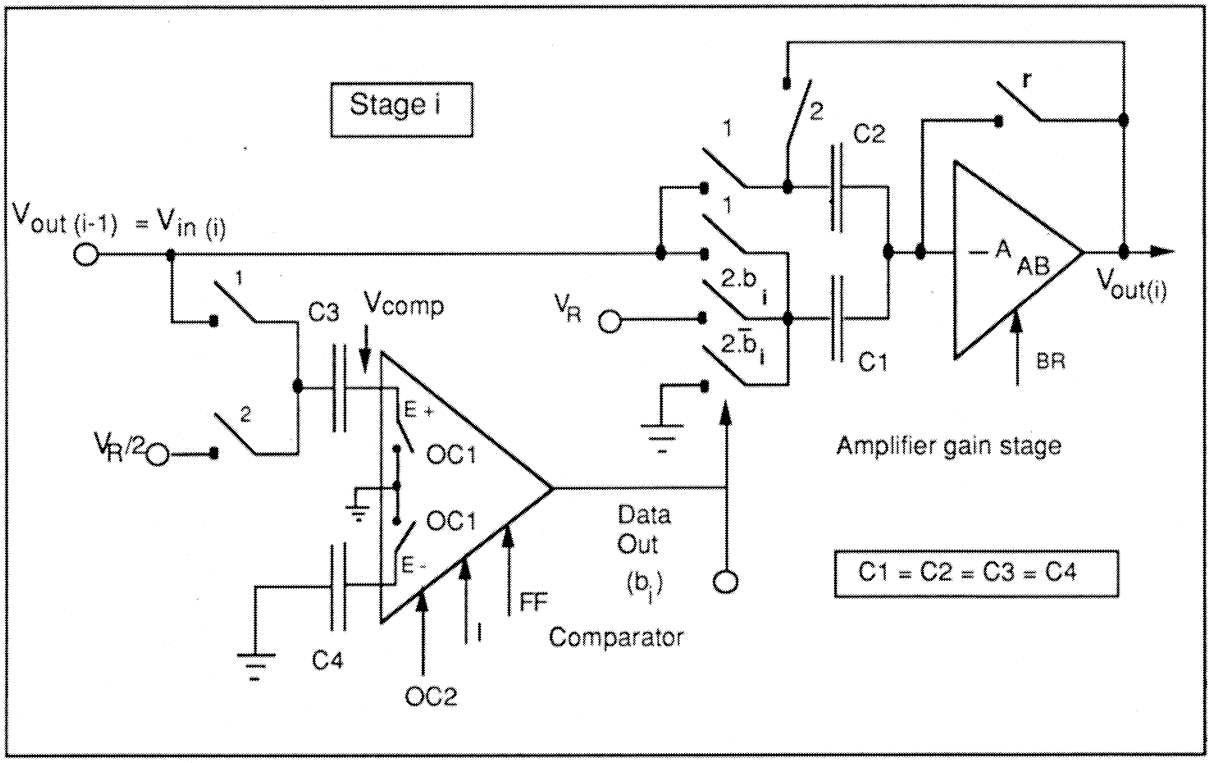

FIGURE 3
Schematic of one single stage of the pipeline A/D converter. The comparator determines the value of the digital bit, while the amplifier performs the analog calculation of the residue.

result of the comparison. These operations are accomplished using a switched–capacitor technique with two non–overlapping clocks T1 and T2. Consider the i–th stage of fig. 3. When T1 is high (switches labelled "1" and "r" are closed), capacitor C_3 is charged to V_{in} and the comparator determines the value of bit b_i by comparison of V_{in} to $V_R/2$. During the same period, capacitors C_1 and C_2 are also charged to V_{in}. The amplifier's bias point, corresponding to an offset voltage, is sampled during this period on the input capacitors by connecting the amplifier in a unity-gain configuration. The input voltage is thus referenced to the amplifier offset, and any change in the input values will be transferred to the output with no offset error. When T1 goes low, the value of bit b_i is latched. When T2 is high (switches labelled "2" and "OC1" are closed), the amplifier output voltage V_{out} becomes twice the input voltage if b_i is low and twice the input voltage minus V_R if b_i is high. This period is also used by the comparator for its internal offset compensation. Assuming ideal components (C_1=C_2), the expression for the residue V_{out}, which becomes the input voltage of the next stage, is then

$$V_{out} = 2V_{in} - b_i.V_R \quad . \qquad (1)$$

In order to reduce the clock feedthrough effect caused by the comparator input switches, a cancellation technique [9] is used. It consists of equalizing the capacitor charge at the comparator's inputs. This explains the presence of the additional capacitor C_4 (which is equal to C_3) at the negative input of the comparator.

It is well known that the linearity of pipelined A/D converters depends essentially on the first few stages. The present structure has, therefore, the advantage to obtain the most significant bit (MSB) directly from the comparator of the first stage according to fig. 2.

The evident complexity of each stage does not allow the pipeline converter to go as fast as a true flash converter, but the structure is offering a speed sufficient for the HARP application, a high accuracy (more than 10 bits) and a very low power consumption. Compared to a n–bit flash A/D converter which requires 2^n comparators, the pipeline structure needs only n comparators and n – 1 amplifiers.

3.2 Gain error correction technique

The performance limits of switched-capacitor A/D converters are mainly determined by practical circuit and technology limitations. Two fundamental factors affect the converter linearity: these are capacitor mismatch and finite amplifier DC gain. Both factors affect the precision of the: "multiply by two" and "subtract" operations done by the switched capacitor amplifier in each stage.

The basic idea of the proposed gain error correction technique is to use the ratio error between two nominally identical capacitors (in the amplifier gain stages) to compensate for the gain error due to the finite amplifier gain. The effect of this technique on the converter linearity can be shown with a simple simulation of the pipeline algorithm. For this, consider the general expression of the output voltage of stage i (fig. 3), excluding offsets and charge injection

$$V_{out(i)} = \frac{V_{out(i-1)}(1+C_1+C_2) - b_i(C_1/C_2)V_R}{[1+(1+C_1/C_2)/A_0]}, \qquad (2)$$

where i = 1, 2... n-1, and A_o represents the finite amplifier gain. If the capacitors C_1 and C_2, which should ideally be equal, are slightly mismatched and the amplifier gain is finite, the output will deviate from the ideal value. For a given A_o, the simulation of the iterative eq. (2) for a n–bit conversion shows two opposite directions in the converter non-linearity: if $C_1/C_2 > 1$, the non-linearity is reduced while, if $C_1/C_2 < 1$, the non-linearity increases.

The gain error correction technique consists, first, in detecting the sense of the capacitor

mismatch due to the process. The largest capacitor is made as C_1 and the smallest as C_2 so that the ratio C_1/C_2 is more than one. The gain error correction technique is applied to the first six stages, as the overall performance of the converter is essentially determined by the characteristics of the first stages. Simulations have shown that applying the correction technique to all stages will not further improve the linearity. This technique is effective if the amplifier gain is sufficiently high, so special care has been taken for the amplifier design in order to maximize the DC gain.

4. EXPERIMENTAL RESULTS

A 12-bit pipelined analog-to-digital converter has been realized in a low-voltage 3 μm SACMOS process by Faselec A.G., Zurich, a subsidiary of Philips N.V.

The microphotograph of the chip is shown in Fig. 4.

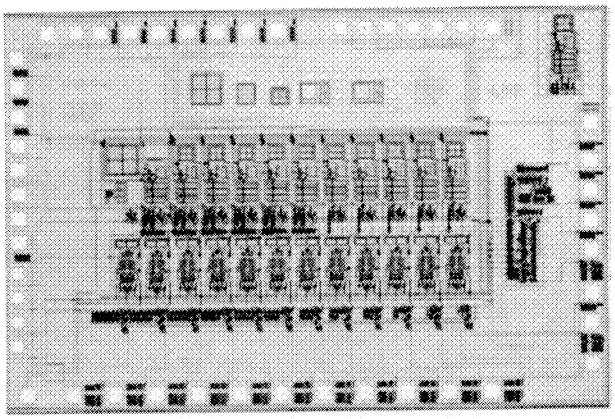

FIGURE 4
Photograph of the chip. Active area (excluding) pads is 5.25 mm^2. Repetitive analog cells are at the centre. At the right is the small logic bloc for the generation of internal phases. Below are the output shift registers which store the successive digital bits per stample.

The active area, including control logic and output registers, is 5.25 mm^2. The measured integral non-linearity (INL) error functions for the *worst* and the *best* case of the capacitors configuration (permutation of C_1 and C_2) are shown in figs 5 and 6, respectively. For 11-bit resolution, an integral non-linearity INL ≤ ± 0.75 LSB is obtained in the best-case configuration. For these tests, the A/D conversion rate was 1 Msample/s. The DC gain of the amplifiers was approximately 70 dB. The power consumptions of the analog and the digital part as a function of the sampling frequency are shown in fig. 7. At 1 MHz sampling rate the total power dissipation of the chip is 12 mW. The measured characteristics of the converter are summarized in table 1.

5. CONCLUSIONS

A 12-bit A/D converter has been developed with good accuracy and a very low power consumption in the order of only 12 mW. This compares very favourably with e.g. flash A/D converters which often use as much as 500 mW for 8 bits conversion, but at higher sampling rates. It is intended to be used as a building block for VLSI chips which will perform the front–end signal processing of future detectors. The evolution of the CMOS technologies in the coming years will allow a reduction in size as well as improved performance in power and speed. Additional digital correction logic at the output of the ADC can also be used to improve the linearity of the conversion.

TABLE 1
Summary of the pipeline A/D converter characteristics

Technology	CMOS 3 μm
Resolution	11 bits
INL & DNL	≤ ± 0.75 LSB
Supply Voltage	± 3 V
ReferenceVoltage	1.5 V
Power consumption	12 mW
Sampling frequency	1 MHz
Active die area (excludes pads)	5.25 mm^2

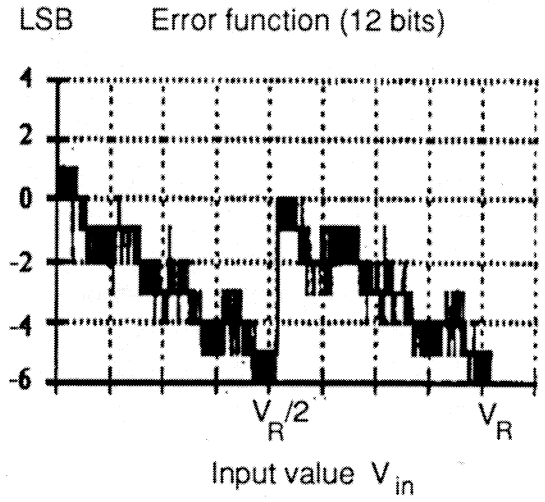

FIGURE 5
Error function of the 12-bit pipeline A/D converter showing the difference in LSB between the ideal and the measured output code for the worst case capacitor configuration ($C_1/C_2 < 1$), at 1 MHz sampling rate.

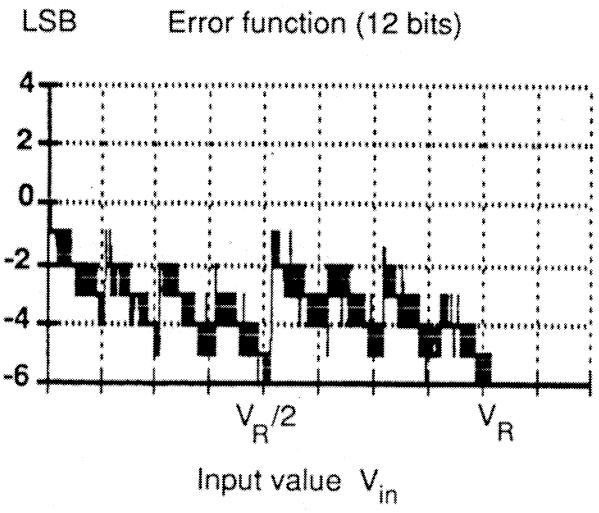

FIGURE 6
Error function of the 12-bit pipeline A/D converter for the best case capacitor configuration ($C_1/C_2 > 1$), at 1 MHz sampling rate.

Acknowledgements

The authors would like to thank F. Rahali for his helpful suggestions for the amplifier design. This development is part of the CERN LAA R&D program for future detectors in particle physics.

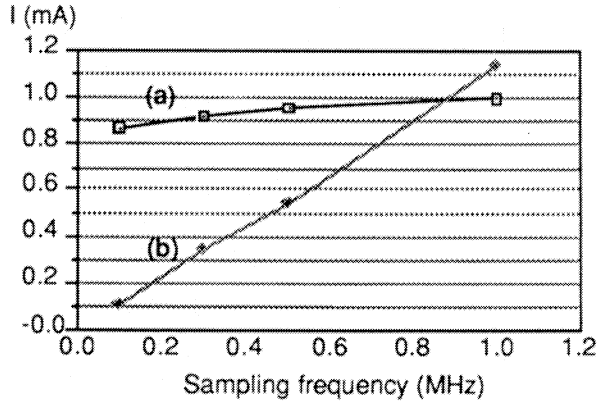

FIGURE 7
Current consumption of the analog (a) and digital (b) parts of the pipeline A/D converter as function of sampling frequency, for ± 3 V power supplies.

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