gFEX, the ATLAS Calorimeter Level 1 Real Time Processor

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on behalf of the ATLAS collaboration
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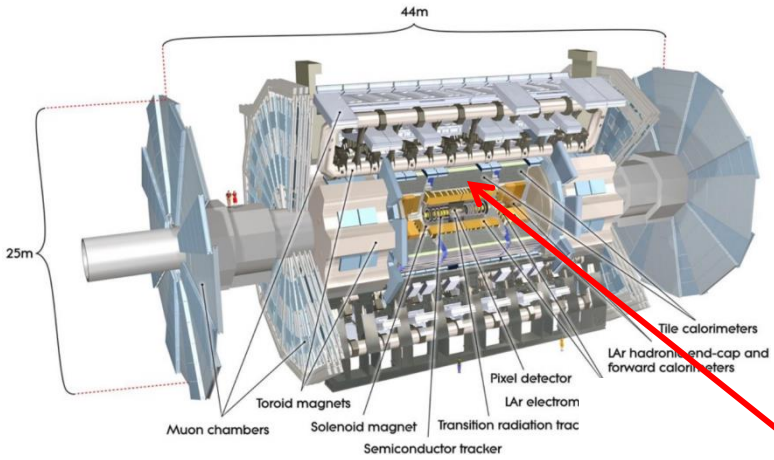
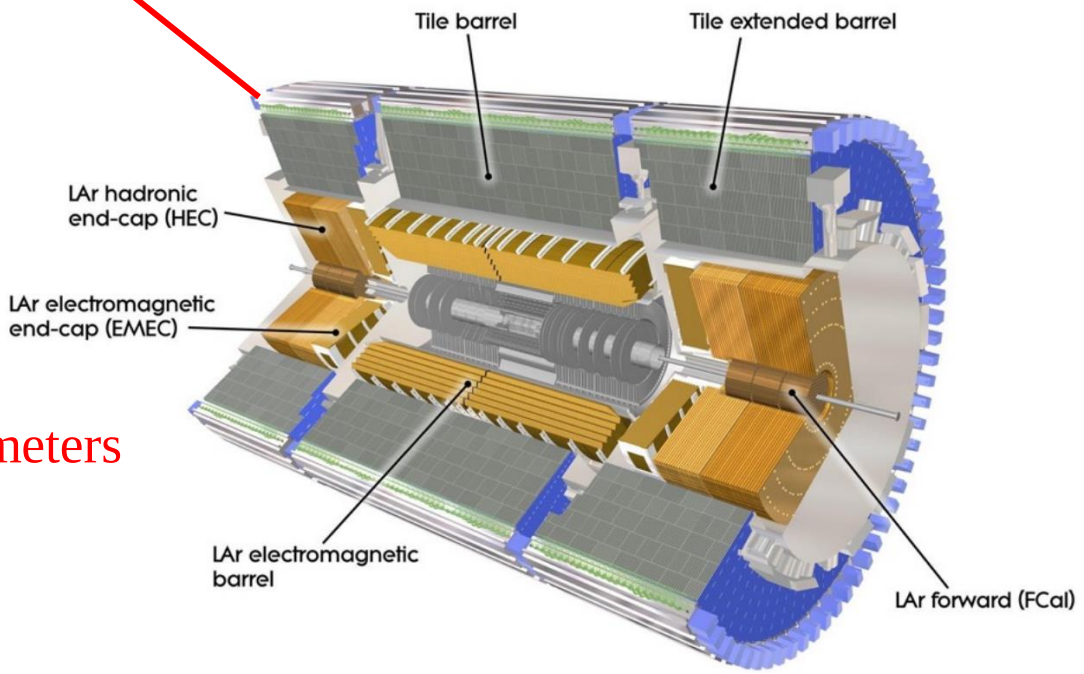
The ATLAS Experiment

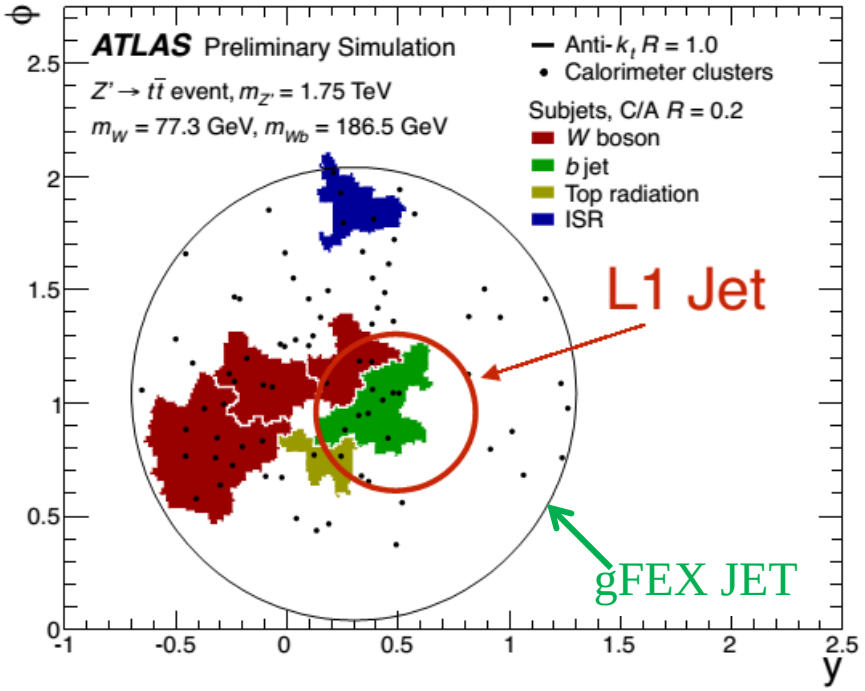




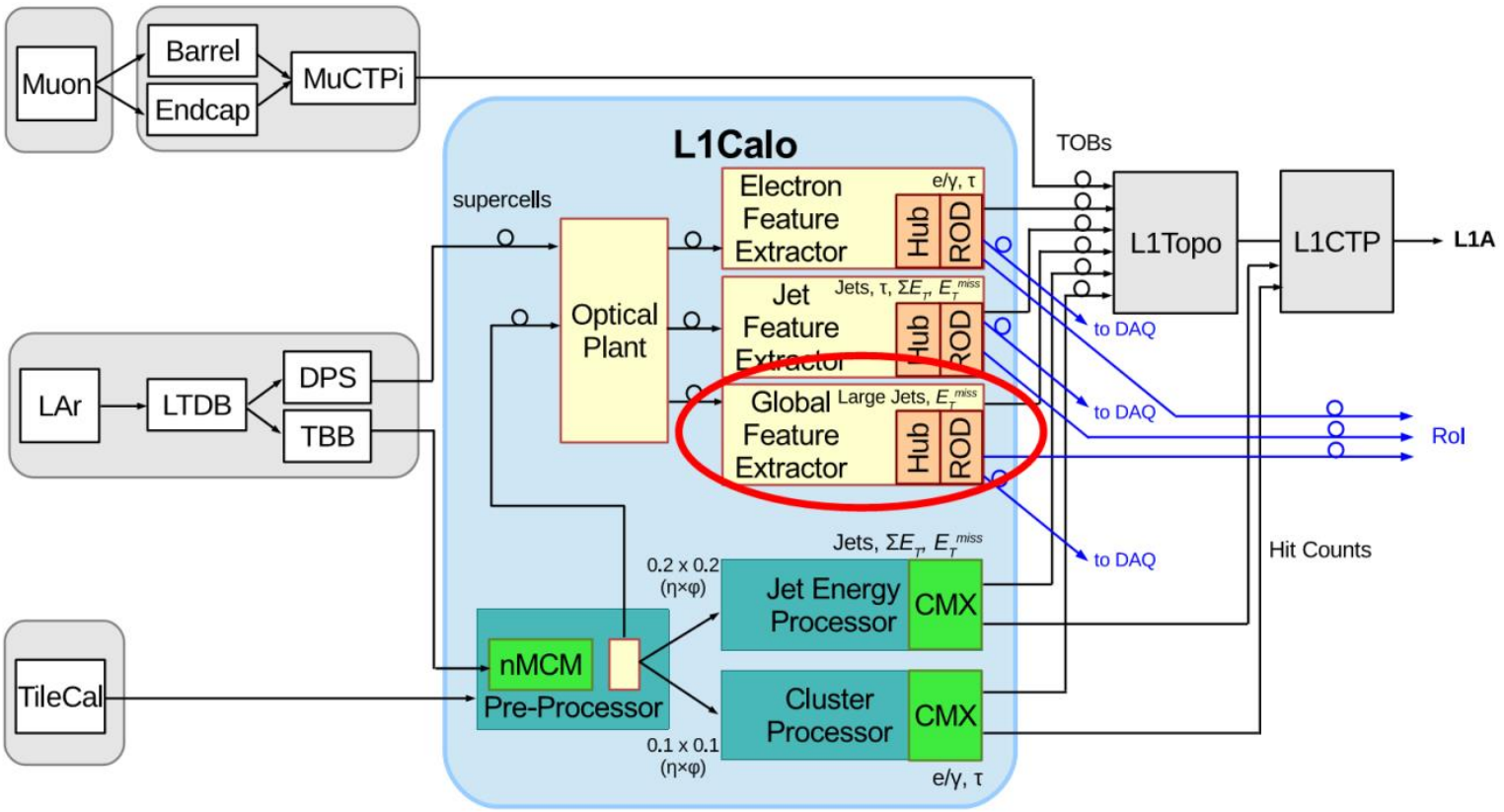
ATLAS Calorimeters

Motivation

- High p_T bosons and fermions are a key component of ATLAS physics.
  - W, Z and H bosons, top quarks and exotic particles
  - Many analyses with boosted objects
- Analyses that addresses this physics use large R jets with R > 1.
- The ATLAS Level 1 trigger was designed for narrow jets, with limited acceptance for large objects. Adding the gFEX, we can accept the boosted objects.



gFEX in ATLAS L1Calo



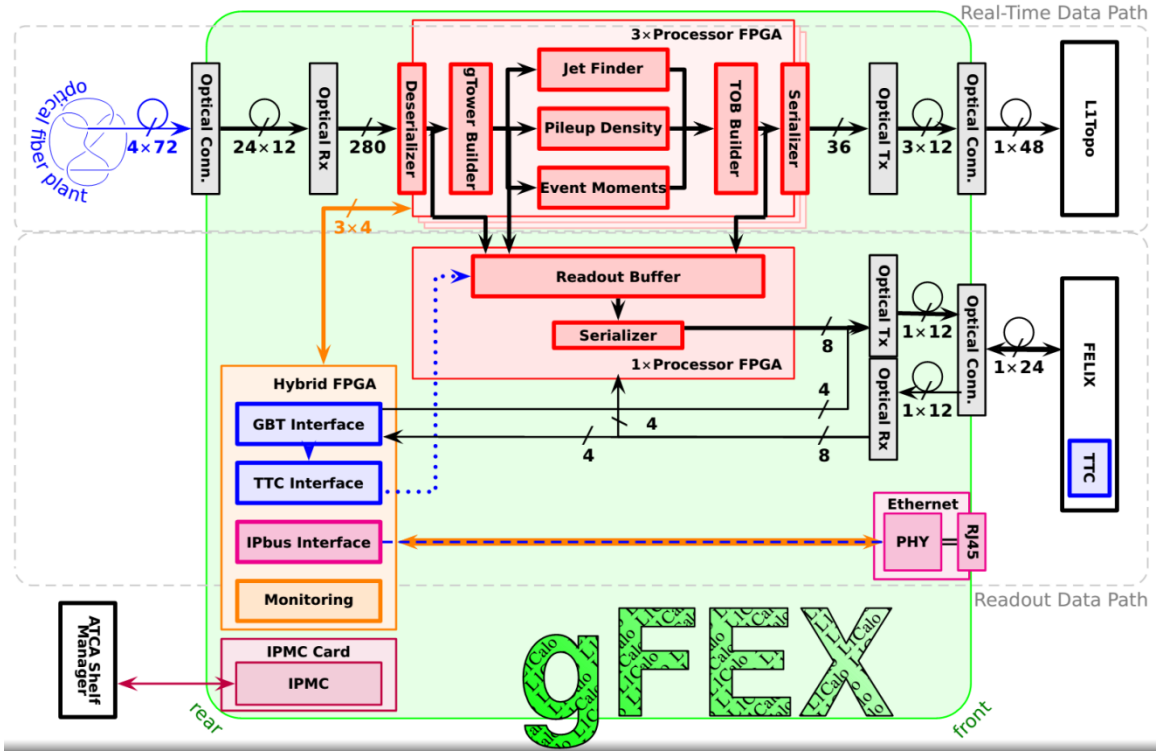
Global Feature Extractor (gFEX) is a component of the ATLAS L1 Calo system in Phase I upgrade. It complements the electron and jet feature extractors. It is a single board system. Both eFEX and jFEX are multi-board systems.

The green ones are for run 2 and the yellow ones are added for run 3.

Phase I is installed during 2019-2020 and will be used for triggering starting 2021

gFEX Interfaces

Input



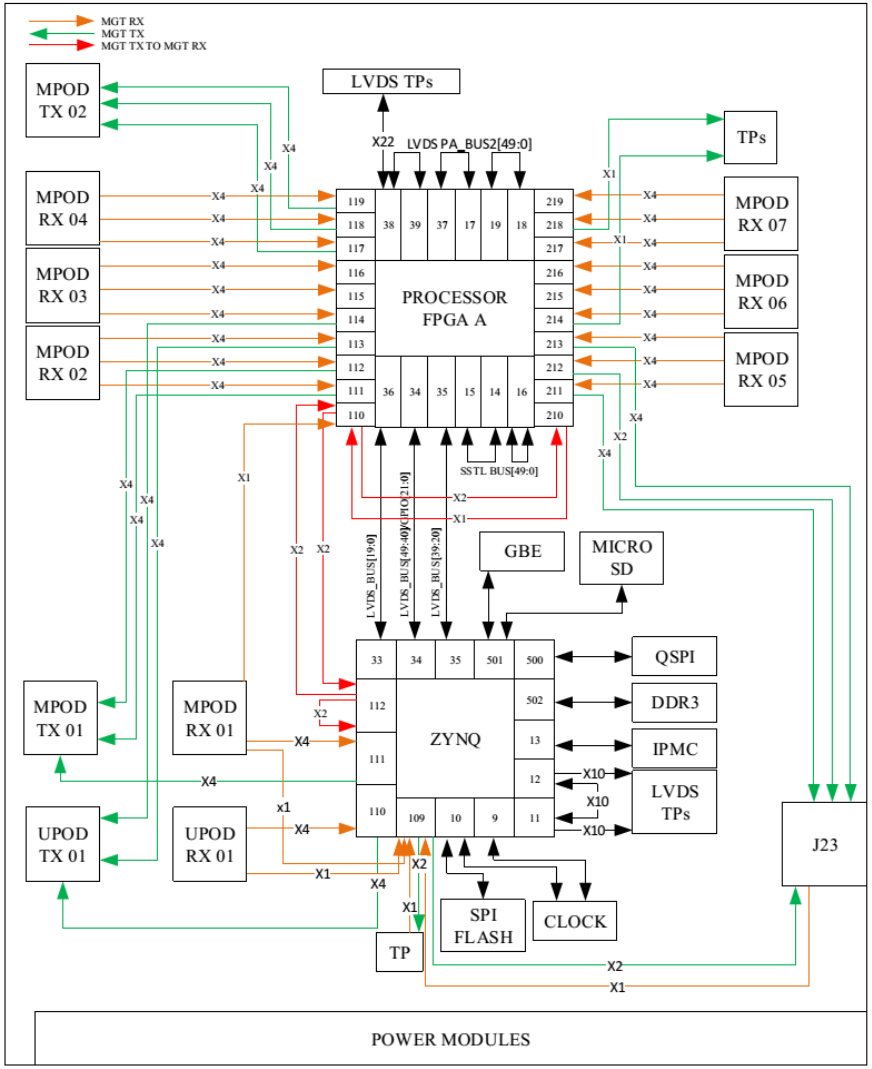
Output

- 4x72 channels fibers come from optical fiber plant (280 channels are used)
- 3 Ultrascale Vertex FPGA function as processor FPGA.(Algorithms are running here)
- ZYNQ for control and monitoring
- IPMC for communicating with ATCA shelf manager and monitoring
- 1x48 channel fibers to L1 Topological Trigger (L1Topo)
- 12 channel fibers to/from FELIX (FELIX is a PCIe module designed for ATLAS System)

Design Purpose of gFEX Pre-prototype

- To verify the boot of FPGAs
  - QSPI, JTAG and SD card boot modes for ZYNQ
  - SPI, JTAG and multi-boot modes for Processor FPGAs
- To verify the control and monitoring function of ZYNQ
  - I2C, SPI, SD,DDR3 and Ethernet interfaces.
- Card powering verification
  - Power sequence
  - Power load
- GTH and GTX link speed test
  - On board loop back with different trace length
  - With MiniPODs and MicroPODs
  - Between GTH and GTX
  - With HUB
- High speed parallel bus verification
  - 50 bits LVDS data bus from Processor FPGA to Processor FPGA
  - 50 bits HSTL data bus from Processor FPGA to Processor FPGA
  - 50 bits LVDS data bus from Processor FPGA to ZYNQ

Block Diagram of gFEX Pre-prototype



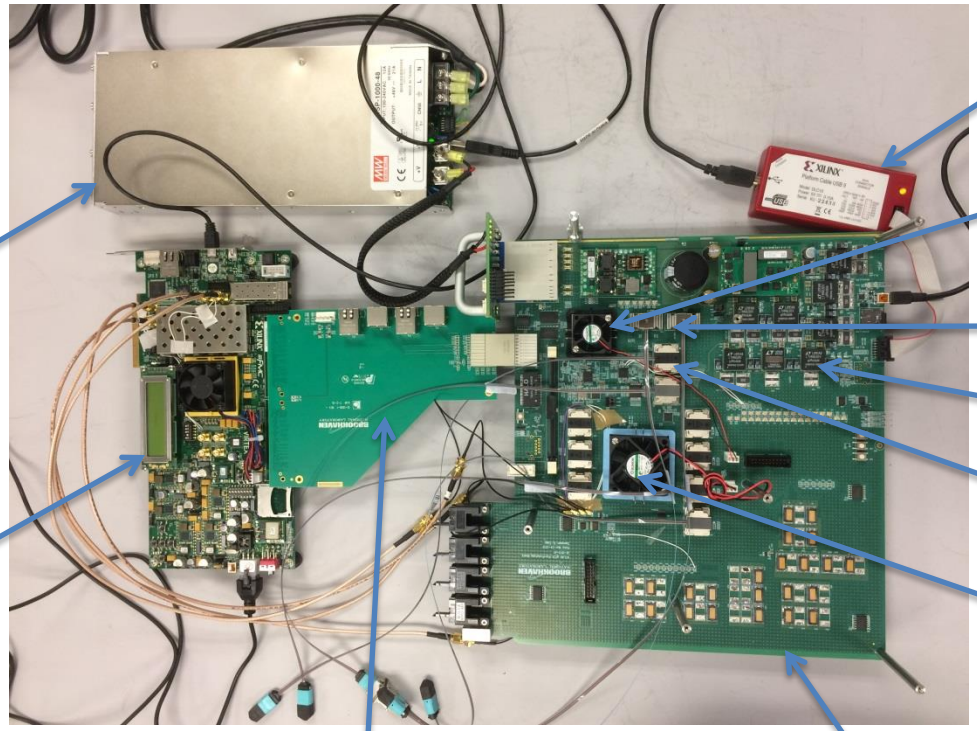
Processor FPGA A :

- 72 GTH RX from Calo (6 MiniPODs)
- 2 GTH RX from ZYNQ
- 12 GTH TX to L1Topo
- 10 GTH TX to HUB
- 2 GTH TX to ZYNQ
- 5 GTH TX to RX loopback (different trace length)
- 50 bits LVDS parallel data bus
- 50 bits HSTL parallel data bus
- 50 bits LVDS parallel data bus to ZYNQ

ZYNQ:

- 4 GTX RX from MiniPODs
- 4 GTX RX from MicroPODs
- 2 GTX RX from Processor FPGA A
- 1 GTX RX from HUB
- 4 GTX TX to MiniPODs
- 4 GTX TX to MicroPODs
- 2 GTX TX to Processor FPGA A
- 2 GTX TX to HUB
- 2 GTX TX to RX loopback (with ac coupling capacitors or not)
- I2C/SD/Ethernet/DDR3/QSPI interface

gFEX Pre-prototype Test Bench



Performance of gFEX Pre-prototype

- JTAG, SD card and QSPI boot modes for ZYNQ √
- JTAG, SPI and Multi-boot modes for processor FPGA √
- I2C, SPI, SD and DDR3 √
- Power sequence controlled by two ADM1066 √
- With the power load resistors, the power module LTM4630 can drive about 34 A. √

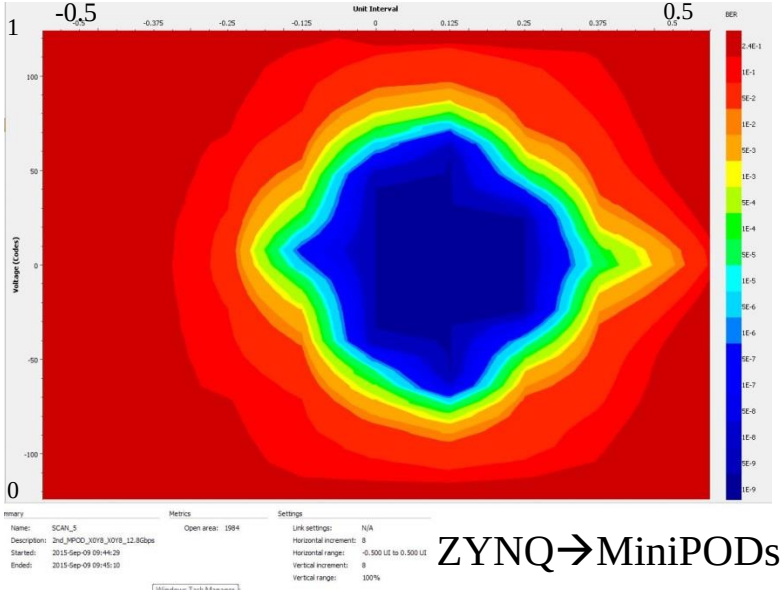
High Speed Parallel Bus

- Three 50-b parallel buses
- Clock delay adjusted with IDELAY in firmware
  - IDELAY step resolution is ≈ 78 ps
  - 32 TAPs, so total length is 2.5 ns
- pFPGA→8 inch LVDS trace→pFPGA @ 480 MHz (960 Mb/s)
  - Stable region is 10 TAPs (~ 0.78 ns); 75% of half cycle (1.0417 ns)
- pFPGA→2.6 inch HSTL trace→pFPGA @ 480 MHz (960 Mb/s)
  - stable region is 10 TAPs (~ 0.78 ns); 75% of half cycle (1.0417 ns)
- pFPGA→4.7 inch LVDS trace→Zynq @ 480 MHz (960 Mb/s)
  - stable region is 9 TAPs (~ 0.702 ns); 67% of half cycle (1.0417 ns)

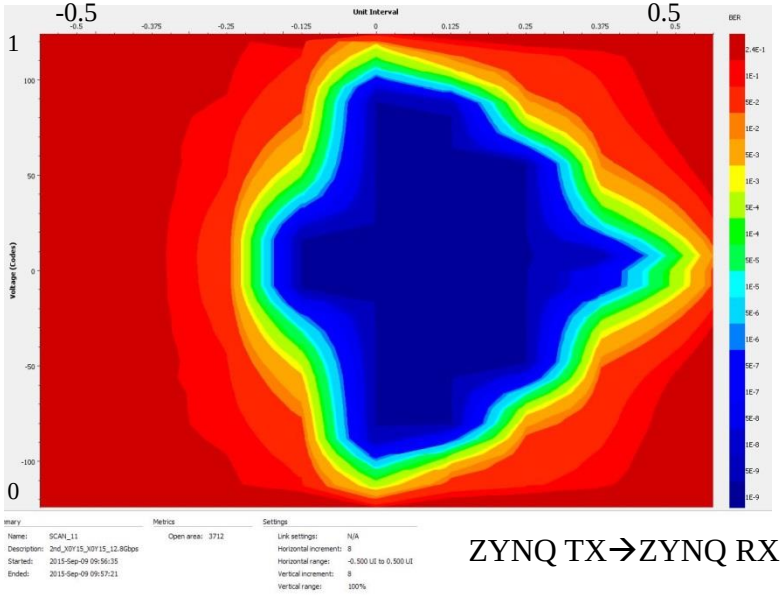
Link Speed Test

- All the links between Processor FPGA, ZYNQ, MiniPODs, and MicroPODs are stable at 12.8 Gb/s with the BER <10E-15, when all the 80 channels GTH of pFPGA and 16 channels GTX of ZYNQ are turned on.
- The links to the backplane, which are tested with backplane test board and VC707 development board, are stable at 10.24 Gb/s.
- The eye diagrams are shown in following slides.

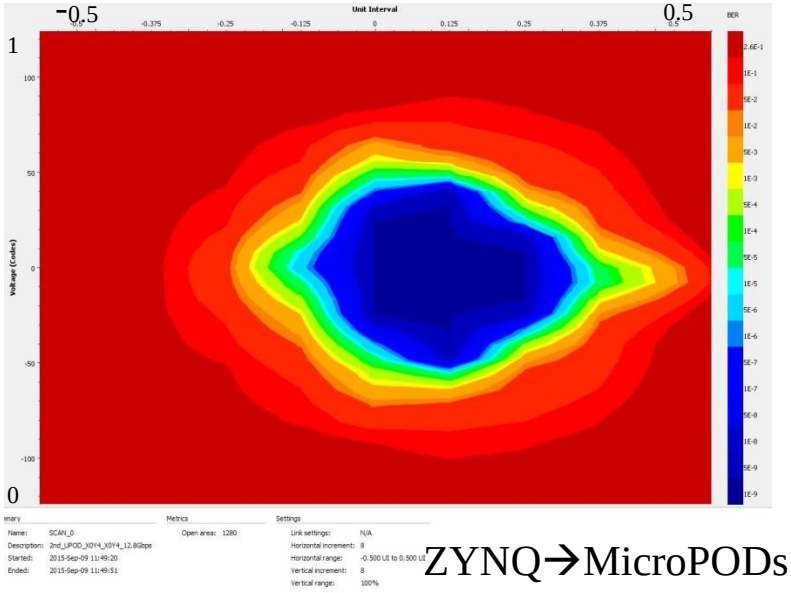
Eye Diagram at 12.8Gb/s (ZYNQ)



ZYNQ→MiniPODs



ZYNQ TX→ZYNQ RX



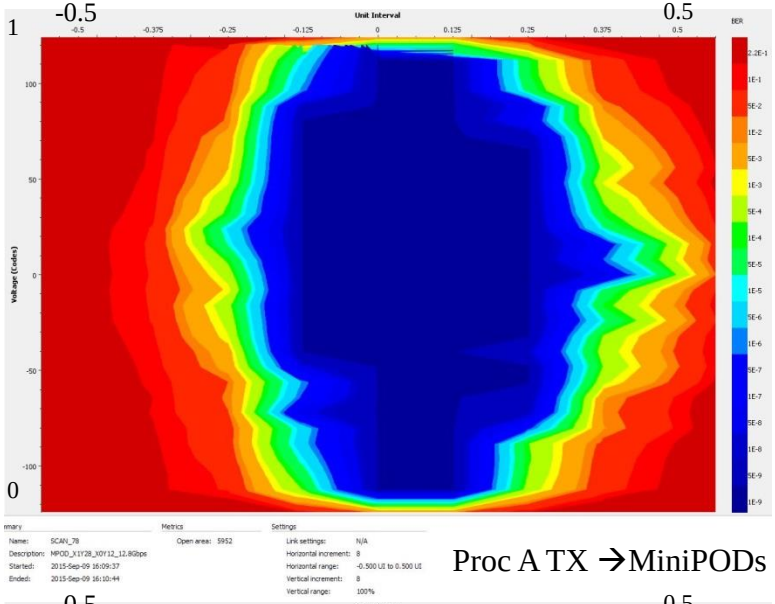
ZYNQ→MicroPODs

The link speed test was done with IBERT, it includes

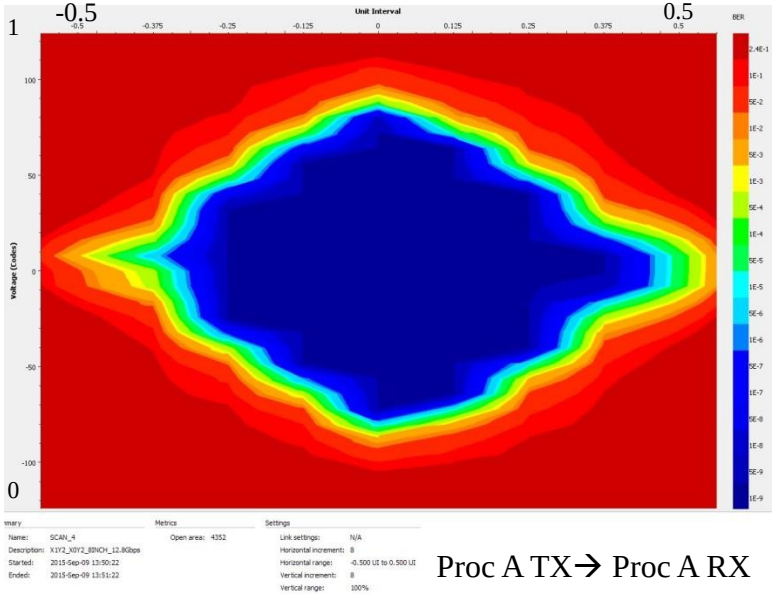
- ZYNQ TX → ZYNQ RX loopback
- ZYNQ TX → MiniPOD TX→Fiber →MiniPOD RX→ZYNQ RX loopback
- ZYNQ TX → MicroPOD TX→Fiber →MicroPOD RX→ZYNQ RX loopback.

- *All the links are stable at 12.8Gb/s when all 16 channels are turned on.*
- *The ZYNQ assembled on this board is XC7Z045-2FFG900.*

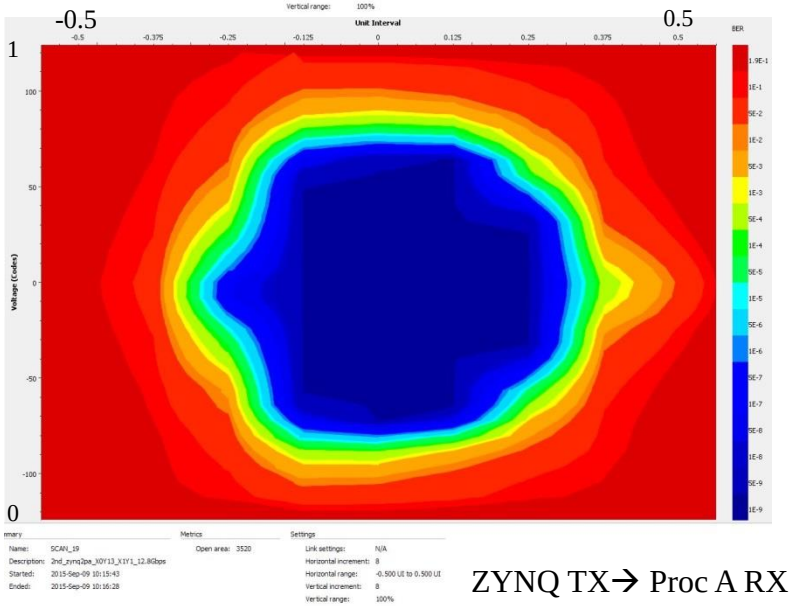
Eye Diagram at 12.8Gb/s (Processor FPGA)



Proc A TX →MiniPODs



Proc A TX→ Proc A RX

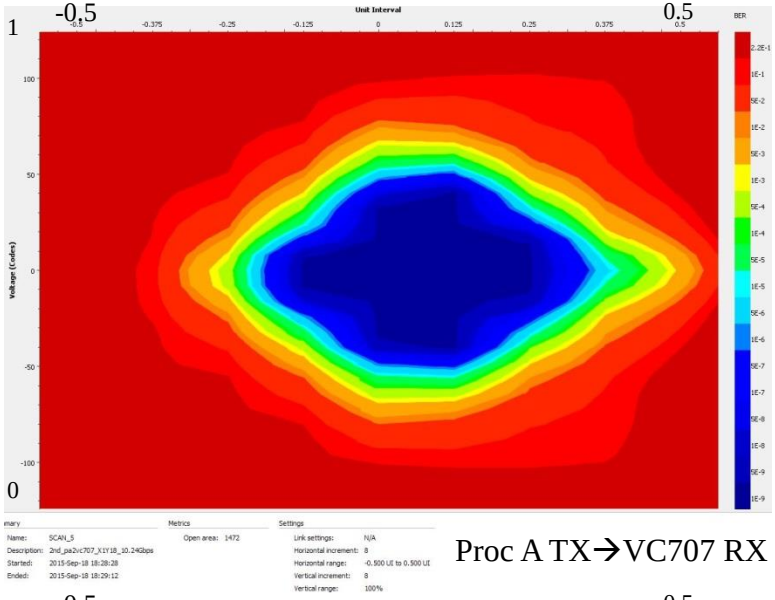


ZYNQ TX→ Proc A RX

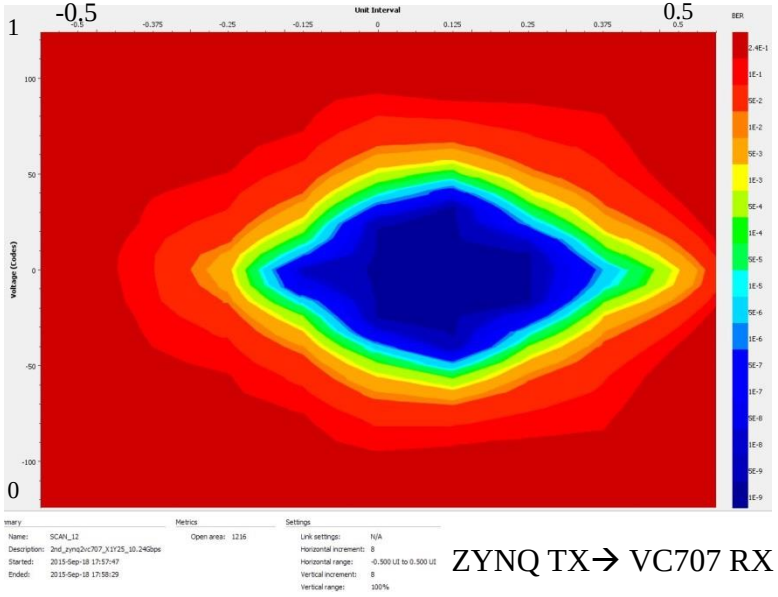
The link speed test was done with IBERT, it includes

- ❑ Proc FPGA TX → Proc FPGA RX (8 inch)
- ❑ Proc FPGA TX → MiniPOD TX→Fiber →MiniPOD RX→ Proc FPGA RX
- ❑ ZYNQ TX → Proc FPGA RX
- ❖ *All the links are stable at 12.8Gb/s when all 80 channels GTH of pFPGA and 16 channels GTX of ZYNQ are turned on.*

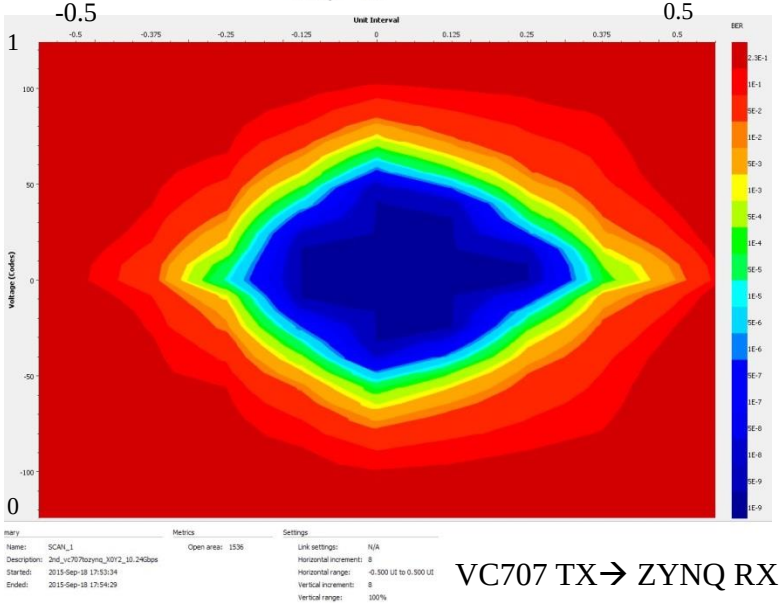
Eye Diagram at 10.24Gb/s (Backplane)



Proc A TX→VC707 RX



ZYNQ TX→ VC707 RX



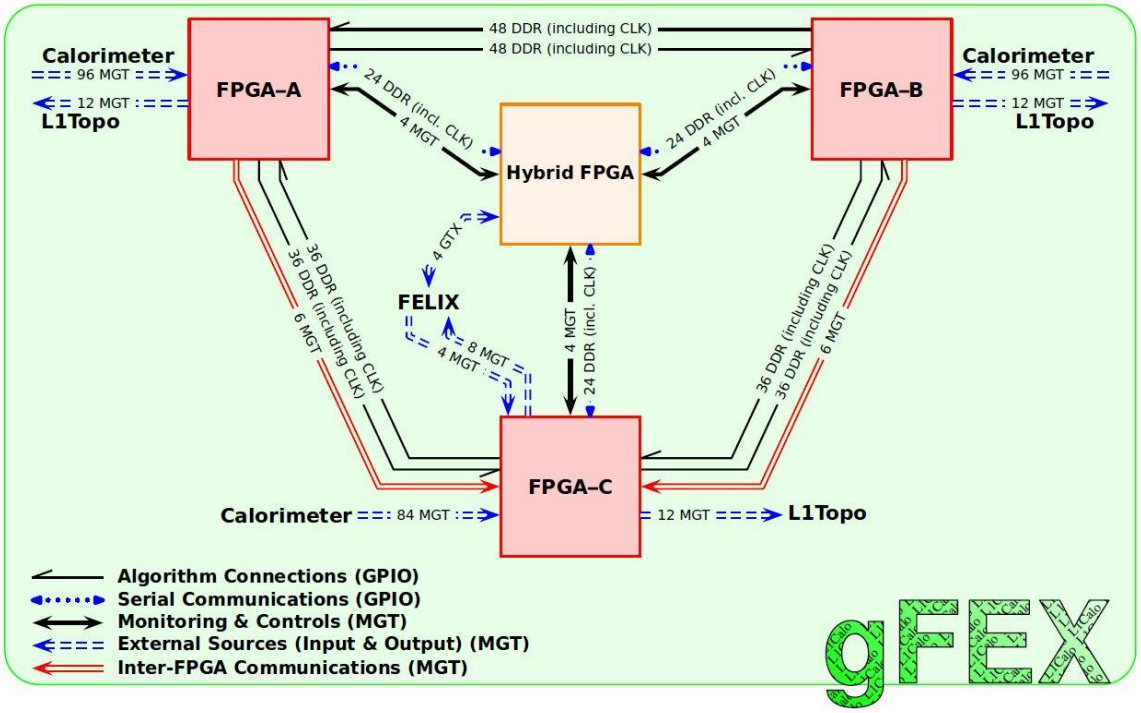
VC707 TX→ ZYNQ RX

The link speed test was done with IBERT, it includes

- Proc FPGA TX → Backplane → VC707 RX (25 inch and 19 inch trace)
- ZYNQ TX → Backplane → VC707 RX (25 inch)
- VC707 TX → Backplane → ZYNQ RX (18 inch)
- All the links are stable at 10.24Gb/s.
- *one channel had a bit error at 11.2 Gb/s due to VC707 (speed grade -2)*
- *VC707 MGT needs slightly higher voltage to further open eye*

Prototype Block Diagram

After the elementary technologies verified in the pre-prototype, a more advanced prototype is designed. The block diagram is shown below.



Processor FPGA A & B:

- 96 RX Calo (12-b ET to eta<2.4)
- 6 TX FPGA C (for read out)
- 12 TX L1Topo
- 4 TX ZYNQ (monitoring data)

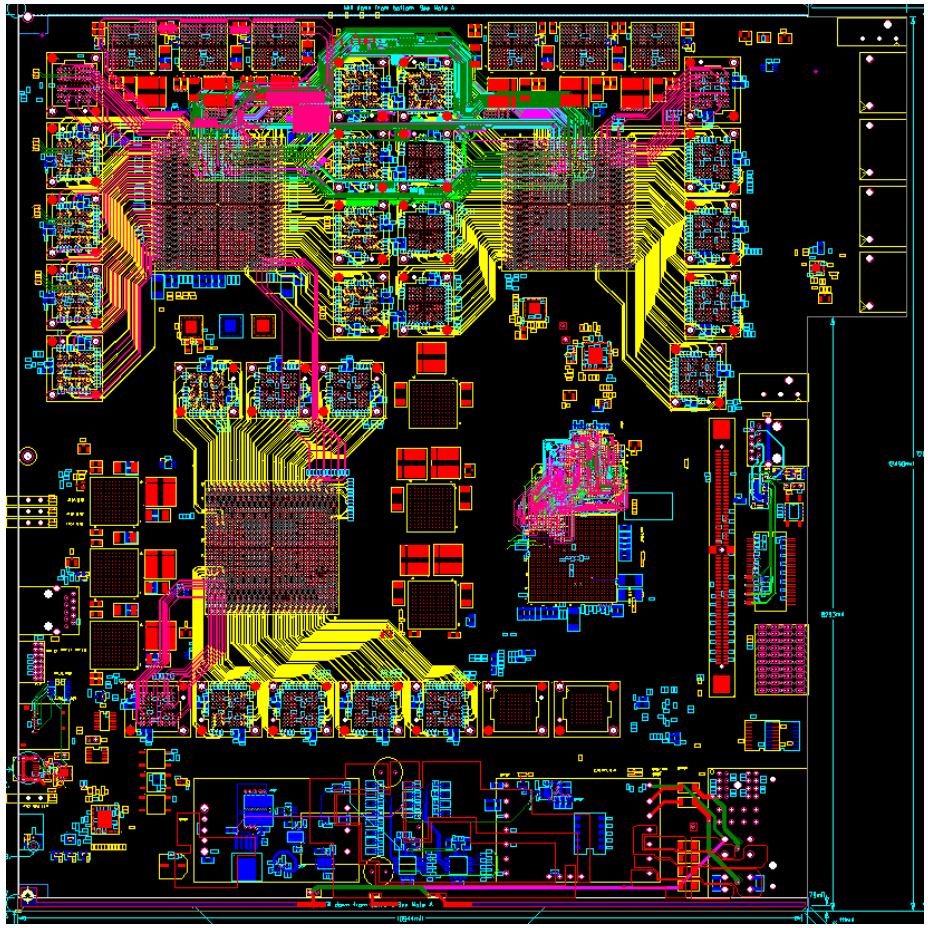
Processor FPGA C:

- 48 RX HEC & EM/IW (9-b ET 2.4<eta<3.2)
- 22 RX FCAL (9-b ET)
- 18 RX Phase-II Upgrades
- 12 RX FPGA A+B (for read out)
- 4 RX FELIX (busies)
- 12 TX L1Topo
- 4 TX ZYNQ (monitoring data)
- 8 TX FELIX (read out & busies)
- 12 TX to HUB1 and HUB2

ZYNQ:

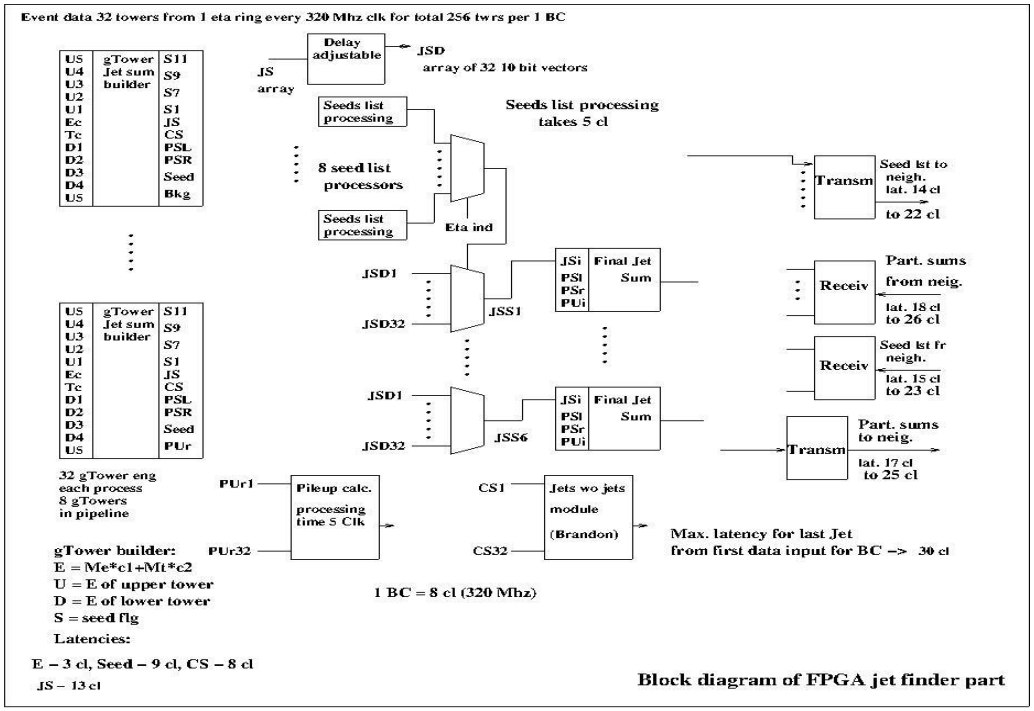
- 4 RX FPGA A
- 4 RX FPGA B
- 4 RX FPGA C
- 4 RX FELIX
- 4 TX FELIX

Prototype implementation



gFEX Firmware Status

- Vivado simulation established
- Detailed C++ register-level emulation of FPGA to aid development
- Integrated large-R jet finding and jets-without-jets algorithms
  - 32 parallel gTower builders/jet sum engines
  - simultaneously calculates jwj observables
  - no structural changes for Ultrascale FPGA but still developing as Virtex-7 architecture
- Initial implementation of Playback Memories in place
- IPBus on Zynq operational



Summary

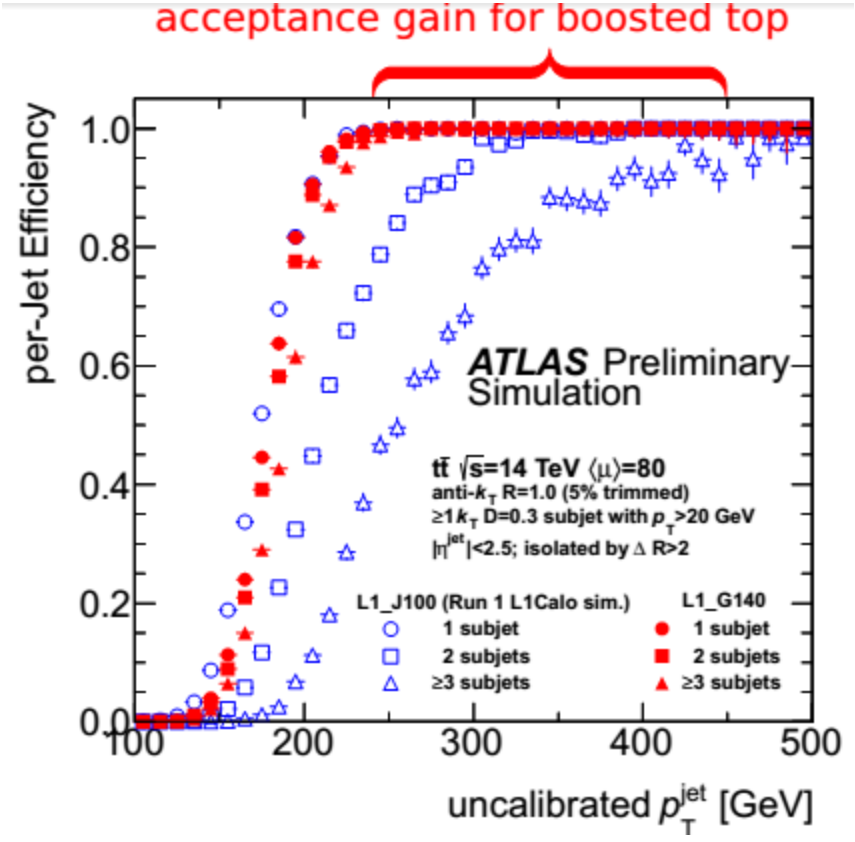
- gFEX Pre-Prototype :
  - power, clocks, infrastructure, etc working mostly as expected
  - MGT IBERT at 12.8 Gb/s with < 1.2 × 10− 15 BER with all 80 Virtex-7 GTH and all 16 Zynq GTX running simultaneously!
  - backplane connections support up to 10.24 Gb/s
  - 50-b parallel buses operate at 960 Mb/s (480 MHz) without issue. It is 50% better than proposed in PDR for the most limited on-board resource!
- Zynq SoC
  - IPBus implementation functions well
  - controls firmware in progress
- gFEX Firmware
  - initial simulations of large-R jet-finding and jets-without-jets algorithm firmware
  - C++ register-level emulation of firmware
  - gTower & jTower object definition
  - supercell-to-gTower mappings
- gFEX Prototype
  - The layout and routing is finished about 40%.

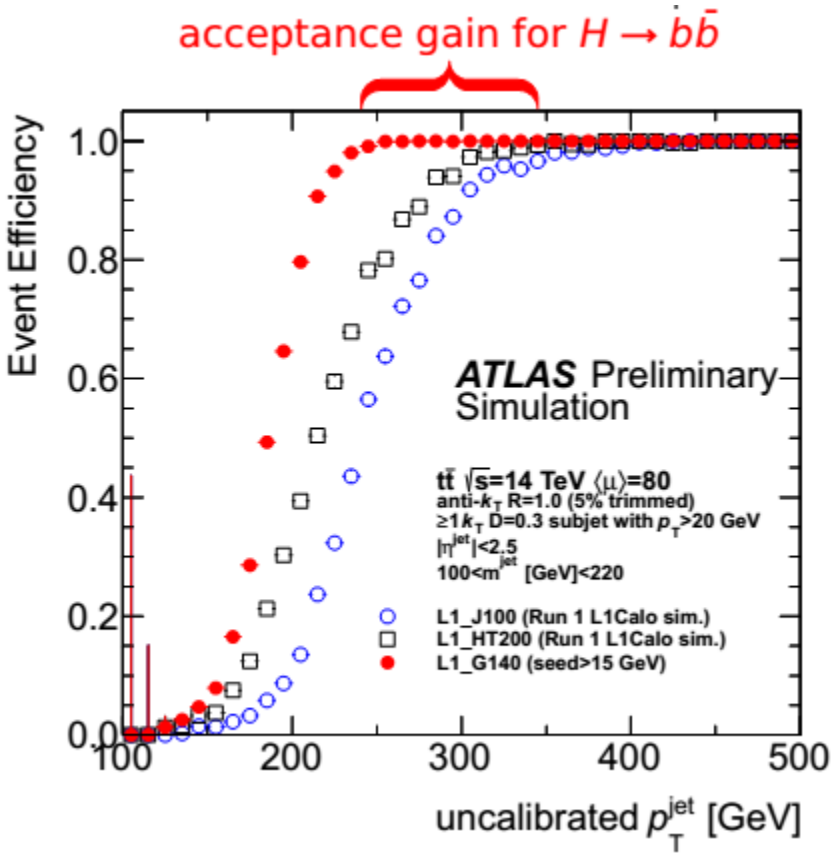
Backup Slides

Abbreviation

- LAr - Liquid Argon
- LTDB - Liquid Argon Trigger Digital Board
- DPS - Digital Processor System
- TBB - Tower Build Board
- L1Calo - L1 Calorimeter
- L1Topo - L1 Topological Trigger
- L1CTP - L1 Center Trigger Processor

Simulation Studies





gFEX Firmware Block Diagram