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Progress on the Upgrade of the CMS Hadron Calorimeter Front-End Electronics

Jake Anderson^a, Jim Freeman^a, Juliana Whitmore^{a,*} for the CMS HCAL Collaboration
^a *Fermi National Accelerator Laboratory, P.O. Box 500, Batavia, IL 60510, USA.*

Abstract

We present a scheme to upgrade the CMS HCAL front-end electronics in the second long shutdown to upgrade the LHC (LS2), which is expected to occur around 2018. The HCAL electronics upgrade is required to handle the major instantaneous luminosity increase (up to $5 * 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$) and an expected integrated luminosity of $\sim 3000 \text{ fb}^{-1}$. A key aspect of the HCAL upgrade is to read out longitudinal segmentation information to improve background rejection, energy resolution, and electron isolation at the L1 trigger. This paper focuses on the requirements for the new electronics and on the proposed solutions. The requirements include increased channel count, additional timing capabilities, and additional redundancy. The electronics are required to operate in a high radiation/high magnetic field environment and are constrained by the existing infrastructure (existing on-detector custom crates, legacy optical fiber, existing water cooling plant, tight trigger latency requirement). The proposed solutions span from chip level to system level. They include the development of a new ASIC ADC, the design and testing of higher speed transmitters to handle the increased data volume, the evaluation and use of circuits from other developments, evaluation of commercial FPGAs, better thermal design, and improvements in the overall readout architecture. We will report on the progress of the designs for these upgraded systems, along with performance requirements and initial design studies.

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1. Introduction

The CMS Hadron Calorimeter [1] is comprised of four distinct subdetectors: the Barrel (HB), the Endcap (HE), the Outer Barrel (HO), and the Forward (HF). The HB, HE, and HO subdetectors are scintillator sampling calorimeters with embedded wavelength shifting fibers (WLS). The fibers from the sampling layers are optically ganged together to form towers whose light is detected by photo-sensors. The HCAL front-end electronics sits on the detector and must operate in a 4-tesla field (for HB/HE). Hybrid photodiodes (HPDs) were initially used as the photo-sensors. The electrical current from a photo-sensor is digitized with a dead-timeless, multi-range custom ADC (QIE) operating at 40 MHz.

* Corresponding author. Tel: +1-630-840-5042; Fax: +1-630-840-2197 *Email address:* jaws@fnal.gov

The QIE currently on the detector has a 5-bit piece-wise linear mantissa and 4 ranges (2-bit), with a dynamic range of 10,000 (1 fC sensitivity up to a maximum input charge of 10 pC). Digital data from several channels are serialized by the Gigabit Optical Link (GOL) at 1.6 Gbps and sent off the detector via Vertical Cavity Surface Emitting Laser Diodes (VCSELs) onto optical fibers. [1,2] The data are sent approximately 100 meters to the HCAL Trigger Cards (HTR), where thresholds are applied, channels are summed to form towers, and trigger primitives are formed. The data are collected in the Data Concentrator Cards (DCC) and sent to the Data Acquisition (DAQ). Figure 1 shows the HCAL readout scheme for the electronics that is currently installed in the CMS detector.

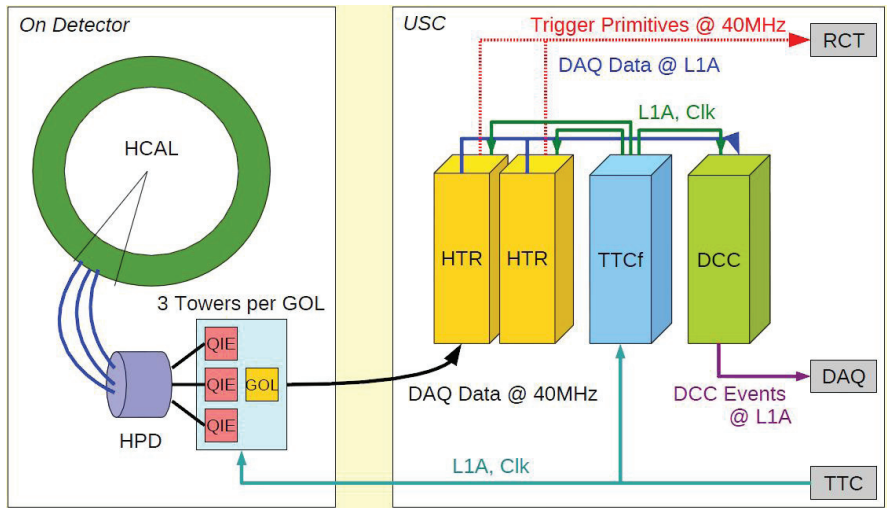


Figure 1: Current readout scheme for the HCAL. The on-detector front-end and off-detector back-end electronics are shown.

The upgrade plan includes replacing HPDs with multi-pixel avalanche photo-diode arrays (also called Silicon PMTs or SiPMs). The ADC also will be redesigned in order to accommodate a wider dynamic range and to provide timing information. The current readout configuration has 5184 channels in HB and HE. The upgrade design allows for longitudinal segmentation of HCAL towers, requiring the number of ADC channels to increase by roughly a factor of 3. The transmission speed for the upgraded electronics will increase from 1.6 Gbps to 4.8 Gbps to deal with the higher data volumes from the increased channel count. The backend will be based on a new readout architecture (μ -TCA [3]) that allows for high-speed data transmission and greater flexibility in data processing and filtering. This article will focus on an upgrade scenario to the HB and HE front-end and back-end readout electronics (see Fig. 2).

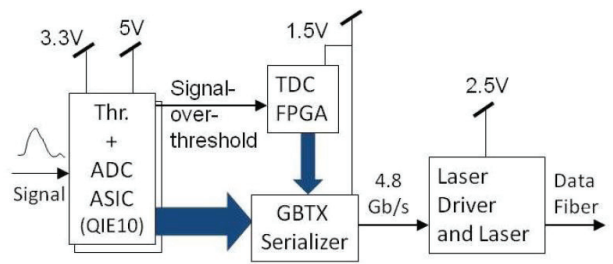


Figure 2: Block diagram of the HCAL front-end electronics upgrade that will include a new Silicon PMT photo-sensor, a new ADC (QIE10), a radiation tolerant FPGA to form TDC information, a new Gigabit transceiver (GBTX), and a new high speed laser driver/laser.

2. Upgraded LHC Environment

The luminosity upgrades for the Large Hadron Collider (LHC) accelerator at CERN will be done in stages. The long shutdowns, (LS1, LS2, and LS3), allow incremental upgrades to the accelerator complex that result in peak luminosities of up to $5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ with an expected total integrated luminosity delivered of $\sim 3000 \text{ fb}^{-1}$. The shutdowns are expected to last from 8 months to 2 years and are currently scheduled to occur periodically after 2-3 years of full-time physics running. LS1 is scheduled for 2013-14, LS2 in 2018-19, and LS3 for sometime after 2021. Financial limitations and tight installation schedules require most of the HCAL infrastructure (mechanical readout boxes/custom crates, cooling pipes, optical fiber plant, etc.) to remain the same. This provides a constraint on the upgraded system in terms of the mechanics, the power dissipation, and the readout bandwidth.

The HCAL upgraded front-end electronics will be installed in LS2. Before accelerator upgrades, the HCAL electronics were expected to see radiation levels of $1.3 \text{E}11 \text{ n/cm}^2$ and 330 rads. The electronics was tested to roughly 3-4 times expected levels, to $5 \text{E}11 \text{ n/cm}^2$ and 1 krad. The corresponding radiation exposure for the HCAL electronics in the upgraded LHC environment is expected to be a factor of 10 more than the current electronics was tested to survive. With a more conservative safety margin, the upgraded electronics are required to be radiation hard to the $1 \text{E}13 \text{ n/cm}^2$ and 10-30 krad levels. [4]

3. Physics Motivation

High luminosity conditions require improvements to the HCAL detector in order to maintain performance. Pile-up conditions will make out-of-time energy rejection algorithms that rely on timing from pulse-shape discrimination to become less efficient. In the current detector, most regions of HB have towers with a single longitudinal depth segmentation. Energy leaking from the electromagnetic calorimeter will damage the inner layers of the HCAL decreasing its response. Adding depth segmentation to the calorimeter towers, at minimum a “Layer 0” forward compartment and a rear compartment, will help improve the energy resolution of the detector as will additional information from longitudinal shower shape. It also will allow the low E_T energy leakage from ECAL to be separated from the high E_T particle flow from jets.

Lepton isolation triggering will be very challenging in LHC high luminosity conditions. At a luminosity of $10^{35} \text{ cm}^{-2}\text{s}^{-1}$ with the current HCAL detector design, isolation criteria are insufficient to reduce the Level 1 single electron trigger rate. Current estimates are a 5kHz rate at an E_T trigger threshold of 20 GeV. Simulations have shown that by removing “Layer 0” from the HCAL tower sum, the background rejection is improved. Placing “Layer 0” in a separate depth segment will allow this possibility.

Higher luminosity will cause severe pile-up conditions. An estimated 200 minimum bias events per crossing (25ns) are expected. In order to reject this out-of-time energy, improved timing and pulse shape information is required. The time resolution for the current detector is determined by looking at the shape of the pulse integrated over a 25ns time sample. Pile-up will severely limit this timing technique. The minimum requirement for the new electronics is to include TDC information to reject out-of-time events.

4. The HCAL Front-end Upgrade Design

One goal of upgrading the HCAL sub-detector is to add longitudinal depth segmentation information to achieve better lepton isolation and to improve background rejection. Figure 3 shows

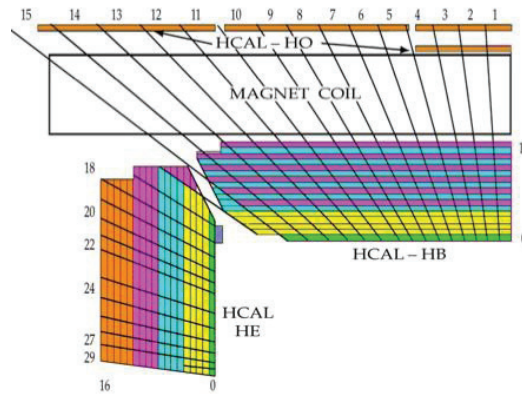


Figure 3: A possible depth segmentation scenario for an upgraded HCAL detector. Colors indicate optical summing for the longitudinal depth segmentations: Layer 0 is depth-1, layers 1-4 are depth-2, odd layers 5-10 are depth-3, and even layers 6-16 are depth-4. The two SiPM analog signals from the interleaved back compartments are then electrically summed to go to a single QIE.

one possible layering scenario for HCAL. The colors indicate the depths for the HCAL towers; in this design, HB has 3 depth segmentations, with interleaved layers for the rear compartment that go to 2 SiPMs that are electrically summed together into a single readout channel. This design adds redundancy in case of a SiPM failure, reduces the required dynamic range of the SiPM, and requires only 3 times the number of front-end channels. A design that had all 4 depth-segmentations being digitized was rejected due to the challenging board layout and increased power from the additional QIEs (estimated to be 350-500 mW), and the bandwidth limitations from the GBT (5 Gbps) and existing fiber plant. Schedule and fiscal constraints limit the upgrade design to reusing much of the existing infrastructure (readout boxes (RBX), digital data fibers, water cooling pipes). Space and electronics cooling constraints restrict the increase in channel count to no more than 3 or 4 times the current number. Current readout boxes dissipate roughly 100W of power. The power budget goal for the upgraded electronics is ~200W. Chips with higher power consumption (e.g. FPGAs and transmitter chips) will be put on boards that will have better thermal coupling to the existing RBX cooling plate.

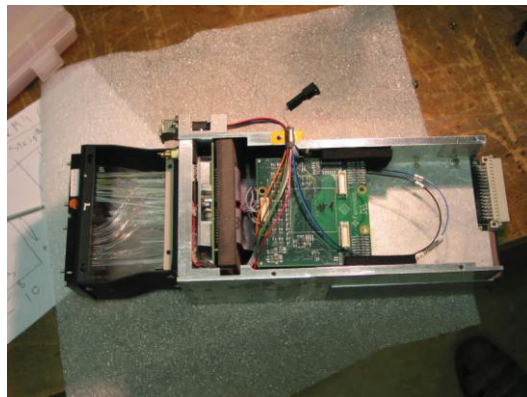


Figure 4: A prototype EODU that was used in a beam test in 2011.

The upgrade designs being investigated form HCAL towers in several different concepts: 1) optically ganging together fibers from the tile layers to form tower depths (ODU – optical decoder unit), 2) presenting individual fibers from a layer to a photo-sensor and electrically ganging the signal to form towers (EDU – electrical decoder unit), or 3) presenting a partial set of fibers from a depth segment to a photo-sensor and electrically summing several photo-sensors to form the complete depth segment (EODU – electrical optical decoder unit). Figure 4 shows the prototype design of the EODU.

The photo-sensor technology that is being studied to replace the Hybrid Photodiode in the HCAL is the Silicon PMT (SiPM). These solid-state devices are basically micro-pixelated Geiger mode Avalanche Photo-Diodes (APDs). They have high gain (10^6), high quantum efficiency ($\sim 20\%$), excellent time resolution, small form factor, can operate in a high magnetic field, can work at room temperature, and can function with a relatively low bias voltage (50-90 V). There are several candidate devices that are promising. For the EDU concept, the Hamamatsu 4.5k cells/mm² pixel Multi-Pixel Photon Counter (MPPC) [5], the Zecotek 15k cells/mm² Micro-Pixel Avalanche Photo Diodes (MAPD) [6], and the KETEK 4.5k cells/mm² device [7] look promising. Although none currently meet all of the requirements of the large dynamic range, the fast pixel recovery time, and radiation hardness, vendors are working to tune the processes and designs to meet the specifications. For the ODUs, Zecotek and Hamamatsu have candidate devices as do FBK-IRST (2.5k cells/mm²) [8], KETEK (2.5k cells/mm²) [7], CPTA (7k cells/mm²) [9], and NDL (10k cells/mm²) [10]. Figure 5 shows a readout module that was used in a beam test at CERN in July, 2011. Each SiPM sees 4 fibers that are mapped according to the optical decoder unit section (the black unit being held on the left side of figure 5a).

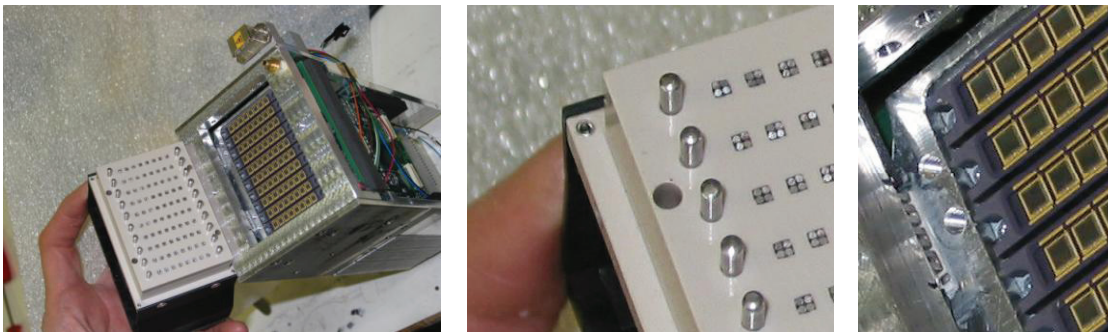


Figure 5(a): A readout module used in a 2011 beam test. The SiPMs are arranged in strips. The optical decoder unit in the left of the figure maps the fibers onto the SiPMs; Figure 5(b) shows a close-up of the 4-fiber bundles that form the 4-layer depths; Figure 5(c) shows a close-up of the SiPM array.

Radiation studies have been performed on the SiPMs under consideration. The apparent decrease in gain as a function of accumulated dose radiation effects seen in earlier studies has been attributed to changes in the over-voltage operating point of the device. Re-calibrating the device should reduce this problem. In addition to total dose effects, which show up as an increase in noise counts, the nuclear counter effect has been studied. But unlike an APD nuclear counter event that affects the entire device, a single-pixel hit on a SiPM with 10k pixels is not as serious an issue. One contribution seems to come from the epoxy potting of the devices, with bare dice being less susceptible to neutron interaction events. An R&D project is underway to develop a thin optical window in place of the standard epoxy encapsulation to protect the SiPM. [11]

SiPM gains vary with temperature on the order of 4%-8% per °C. Peltier coolers that are mounted on the SiPM mounting cards in each readout module will be used to maintain thermal stability

of the system. The readout module Peltier system with a slow control feedback loop has been used in a beam test and has been shown to be stable to within 0.1°C.

The current from the SiPMs is then sent to a custom ADC. One ADC option that is being investigated is an upgraded version of the Charge Integrating and Encoding (QIE) [12] ASIC that is currently used for HCAL. The upgraded QIE is a piece-wise linear, dead-timeless ADC that covers an effective dynamic range of 100,000 (16-17 bits) with only 4 range scales (2-bits) for the current-splitter and a 6-bit 5-sensitivity scale FADC. It achieves this large dynamic range while requiring few output bits by use of a nonlinear response function that is tuned to the calorimeter response. There are 4 ranges with a factor of 8 difference in sensitivity between ranges. The upgraded chip has more than a factor of 10 more dynamic range and 1-bit more sensitivity than the current QIE. The corresponding charge sensitivity is 3fC with a maximum input charge of 330 pC. An additional 2-bits are used to identify the integration capacitor in the 4-stage pipeline. In addition to ADC information, the QIE will generate 5-6 bits of TDC providing 1-2ns timing resolution. The current system uses pulse shape as a timing discriminator, which will degrade as the pile-up increases. Also the chip will provide a level to indicate when the input pulse goes above a programmable threshold. This level will be sent to an FPGA to provide pulse arrival time and pulse width information. The QIE will have a programmable adjustment for the phase of its integration clock and will synchronize and re-phase the digital data going to the FPGA. The QIE will be fabricated in the AMS 0.35 μm SiGe bi-CMOS process. [13] The advantage of the SiGe processes is the higher radiation tolerance of the bipolar transistors. [14] The QIE is currently being developed as a single channel device, although the option of putting four channels into a single chip package or four channels into a single chip is being investigated.

The QIE data can either go directly to the serializer or to an FPGA before going to the serializer. The FPGA can collect, re-phase, reduce redundant data from multiple QIEs, and do simple error checking. It also can be programmed to provide additional information, such as the pulse width. The data then will be sent to the Gigabit Bi-directional Transceiver (GBT) chips [15] that will drive 82 HCAL user bits every 25 ns on a 4.8 Gb/s serial link. Since the number of installed optical links is limited, the majority of fibers will be used as up-links. A dual optical transmitter using VCSELs that is being developed for LHCb [16] is ideal for the HCAL needs for the Versatile Link Project. [17]

Slow controls will also be done via GBT opto-links, with 1 uplink and 1 downlink for front-end communication. The clock, SiPM bias voltages, Peltier Cooler voltages, front-end board voltages, and QIE integration phase adjustment will be downloaded. SiPM leakage current, front-end board voltage read-back, SiPM board and front-end card temperatures will be sent on the uplink.

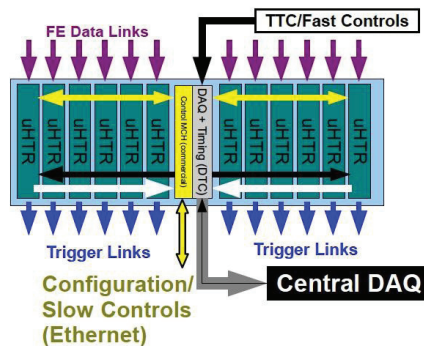


Figure 6: The data flow of the HCAL micro-TCA Back-End electronics.

The back-end data collection will be done with a μ TCA based system (Fig. 6), which will receive 4.8 Gbps data, apply thresholds and sum energies, generate crate trigger primitives that are passed to the Level-1 trigger, and hold the pipelined data for possible read-out by the DAQ. New μ TCA data/trigger boards and data hubs have already been developed [18,19]. Parasitic operation with the new backend readout electronics will be exercised during physics running in 2012.

4. Upgrade Timeline

The upgrade to the HCAL electronics will be staged. During the LS1 shutdown, the backend μ TCA readout will be installed. This will allow full commissioning of the back-end well in advance of any front-end changes. The HB/HE frontend upgrade will occur in LS2, although some electronics may be installed earlier if there is a shutdown opportunity. HCAL has already gained operational experience with SiPMs in some RBXs that were installed in May 2009 in the HO region. The entire HO will be upgraded to SiPMs in LS1 [20], so there will be extensive operational experience before the HB/HE SiPM upgrade.

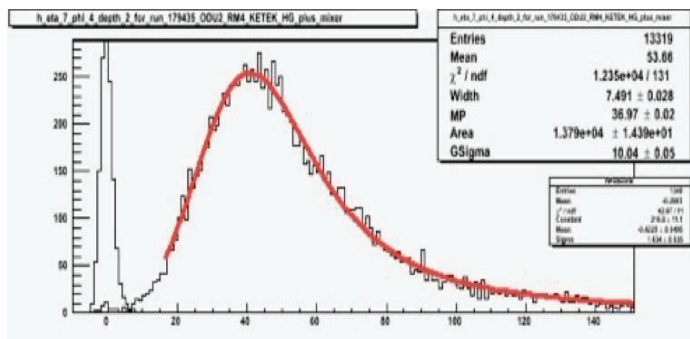


Figure 7: Minimum ionizing particle response in linear ADC counts (sum of 4 time slices) from HB with a KETEK device during the 2011 beam test.

CERN beam tests in July and October 2011 have given very promising results, with a signal to noise of 20/1 for minimum ionizing particles (see Fig. 7). Additional studies of single layer readout are providing information for simulations to better understand the electrical ganging to optimize the energy resolution. It is expected that by the end of 2011, at least one candidate device which satisfies the HCAL requirements will be identified.

5. Summary

An electronics upgrade of the CMS HCAL detector that replaces HPDs with SiPMs is being studied. This upgrade will provide additional depth segmentation information and will improve the detector performance at high luminosity. SiPMs in beam tests and in the HO region of the CMS detector have shown promising results. A planned μ TCA backend upgrade will be installed and commissioned in LS1. The front-end electronics upgrade R&D path is on track for installation during the LS2 shutdown.

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