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Results from the NA62 Gigatracker prototype: a low-mass and sub-ns time resolution silicon pixel detector

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Abstract

The Gigatracker (GTK) is a hybrid silicon pixel detector developed for NA62, the experiment aimed at studying ultra-rare kaon decays at the CERN SPS. Three GTK stations will provide precise momentum and angular measurements on every track of the high intensity NA62 hadron beam with a time-tagging resolution of 150 ps. Multiple scattering and hadronic interactions of beam particles in the GTK have to be minimized to keep background events at acceptable levels, hence the total material budget is fixed to 0.5% X_0 per station. In addition the calculated fluence for 100 days of running is 2×10^{14} 1 MeV n_{eq}/cm^2, comparable to the one expected for the inner trackers of LHC detectors in 10 years of operation. These requirements pose challenges for the development of an efficient and low-mass cooling system, to be operated in vacuum, and on the thinning of read-out chips to 100 μm or less. The most challenging requirement is represented by the time resolution, which can be achieved by carefully compensating for the discriminator time-walk. For this purpose, two complementary read-out architectures have been designed and produced as small-scale prototypes: the first is based on the use of a Time-over-Threshold circuit followed by a TDC shared by a group of pixels, while the other uses a constant-fraction discriminator followed by an on-pixel TDC. The readout pixel ASICs are produced in 130 nm IBM CMOS technology and bump-bonded to 200 μm thick silicon sensors. The Gigatracker detector system is described with particular emphasis on recent experimental results obtained from laboratory and beam tests of prototype bump-bonded assemblies, which show a time resolution of less than 200 ps for single hits.

Keywords: Solid-state detectors, Tracking and position-sensitive detectors, Silicon pixel ASIC, Time-to-Digital Converter

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1. The NA62 experiment

NA62 is a fixed target experiment at the CERN SPS, specifically designed to measure $O(100)$ events of the ultra-rare decay $K^+ \rightarrow \pi^+\nu\bar{\nu}$ with low background (~10%) in about two years of data taking [1]. This decay mode has a branching ratio of $(7.8 \pm 0.8) \times 10^{-11}$, predicted with high accuracy in the Standard Model with a theoretical error of a few percent [2].

This measurement is extremely challenging from the experimental point of view due to the large backgrounds coming from the other decay channels, primarily $K^+ \rightarrow \mu^+\nu$ and $K^+ \rightarrow \pi^+\pi^0$ that have branching ratios of ~64% and ~21% respectively. NA62 will study $K^+ \rightarrow \pi^+\nu\bar{\nu}$ using kaon decaying in-flight. This technique makes use of an un-separated 75 GeV/c kaon beam (the kaon fraction is ~6% of the total) and essentially allows to reduce inefficiency problems for vetoing low energy particles. A schematic layout of the experiment is shown in Fig 1.
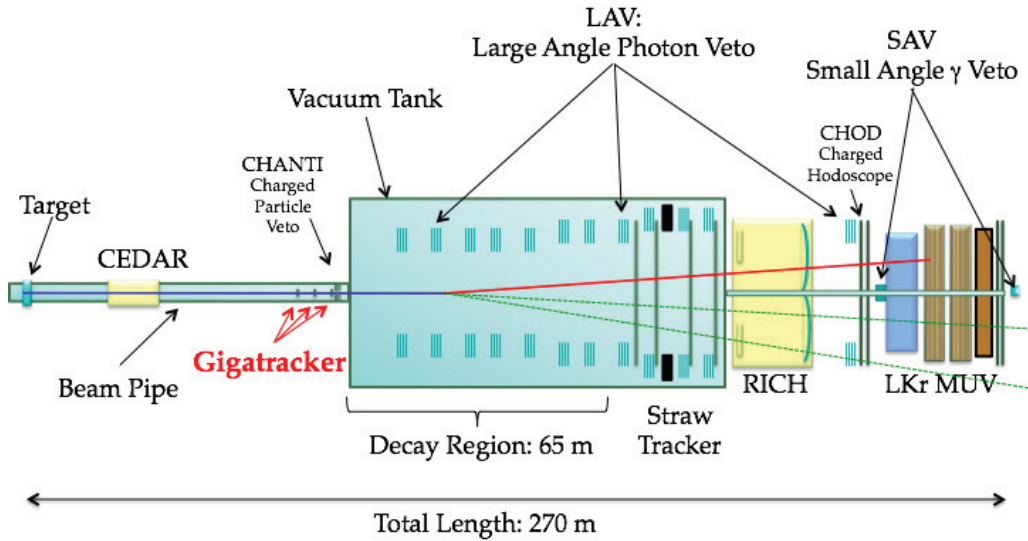

Fig. 1. Schematic drawing of the NA62 experiment.

Background reduction will be achieved by means of highly efficient photon vetoes (LAV, LKr - Liquid Krypton calorimeter - and SAV) and particle identification detectors, together with kinematical cuts on the missing mass variable:

$$m_{miss}^2 \simeq m_K^2 \cdot (1 - \frac{|p_\pi|}{|p_K|}) + m_\pi^2 \cdot (1 - \frac{|p_K|}{|p_\pi|}) - |p_K| \cdot |p_\pi| \cdot \theta_{\pi K}^2$$

where p_K (p_π) and m_K (m_π) are the kaon (pion) momentum and mass, respectively, and $\theta_{\pi K}$ is the angle between the two tracks. The experiment is equipped with two spectrometers: a first one to measure the kaon track upstream of the decay region (Gigatracker) and a second one with large acceptance (Straw Tracker) to measure the momentum of kaon charged decay products. The setup also includes particle identification detectors (CEDAR and RICH), a charged hodoscope (CHOD), a charged particle veto following the Gigatracker (CHANTI) and a muon detection system (MUV).

2. The Gigatracker

The beam spectrometer of the experiment consists of three Gigatracker (GTK) stations installed in vacuum together with a series of dipole magnets, as indicated in Fig 2. This detector system has to provide precise momentum, time and angular measurements on all beam tracks and has to sustain high and non-uniform particles rate (~1.5 MHz/mm² in the center, 0.8-1.0 GHz in total). The total material budget per
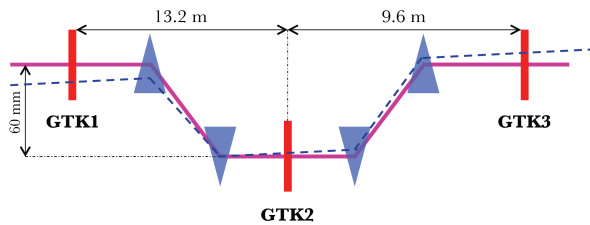
Fig. 2. Basic elements of the NA62 beam spectrometer. The three Gigatracker (GTK) stations are represented by red rectangles, while bending dipole magnets are drawn as blue triangles.
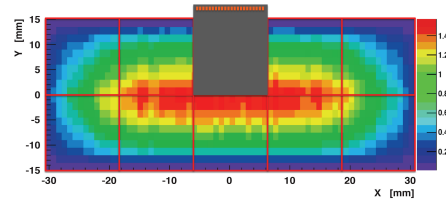

Fig. 3. Beam intensity distribution on a single GTK station (units are MHz/mm^2). A schematic drawing of one read-out chip is shown.

station has been fixed to 0.5% X_0 in order to reduce multiple scattering and hadronic interactions of the beam particles. The most challenging requirement on this detector is the time resolution of 150 ps for a single track, that will allow to associate the daughter pion track to the correct parent kaon [3].

A single Gigatracker station consists of one silicon sensor (60×27 mm^2) bump-bonded to ten read-out chips, as shown schematically in Fig 3. A pixel size of 300 μm $\times$ 300 μm, together with the proper spectrometer lever arm, is sufficient to achieve the required momentum ($\sigma(p_K)/p_K \sim 0.2\%$) and angular ($\sigma(\theta_K) \sim 16$ μrad) resolutions.

Sensor thickness has been fixed to 200 μm as a trade-off between material budget requirements and the signal-to-noise ratio needed to achieve the target time resolution. Wafer processing (p-in-n) has been performed at FBK (Trento, Italy). Sensor operation at 300 V over-bias is needed to achieve the required time resolution, thanks to the shorter charge collection time. Flip-chip bonding for prototype sensors has been done at IZM (Berlin, Germany). In order to match the severe material budget requirements, the read-out chips in the final full-size version will be thinned down to 100 μm or less.

A fluence of up to 2×10^{14} 1 MeV n eq. cm^{-2} is expected in the central region of the sensor during one year of operation. Irradiations of p-in-n diodes with fast neutrons and protons have been performed, in addition to annealing measurements (I-V and C-V curves) following the expected run scenario, in order to characterize the sensor operation in a high radiation environment. Results show that the most critical parameter in operating the Gigatracker is the radiation induced leakage current, which can be kept to an acceptable value if the sensor temperature can be maintained below 5°C. Irradiations of prototype Gigatracker bump-bonded assemblies will also be done in order to evaluate the sensor and read-out chip performances (especially time resolution) as a function of the accumulated dose.

3. Cooling options

An efficient cooling system is necessary for stable detector operation. In addition, to comply with the stringent material budget requirements, the cooling and support system must be of very low mass ($\sim$0.15% X_0) in the active beam area. Two cooling options are under study, that should dissipate the total power produced by the read-out chips ($\sim$32 W per station) and keep the sensor at a temperature of $\sim$-20°C.

One solution is based on convective cooling inside a vessel. As shown in Fig. 4, the detector is mounted on a printed circuit board (PCB) and housed inside a cylindrical aluminum vessel, and the GTK assembly is separated from the vacuum by two thin (50 μm) kapton walls in the beam region. Cooling is achieved through a flow of cold gaseous nitrogen ($\sim$100 K at the inlet). A full size prototype has been built and optimizations are ongoing to improve uniformity of temperature distribution across sensor area.

The other option exploits conduction between the Gigatracker assembly and a micro-channel cooling plate, connected to it through a high thermal conductivity adhesive material. The cooling plate is composed of two silicon wafers (150 μm thickness in total in the active beam area) bonded to each other, as shown in Fig. 5. Micro-channels, in addition to the openings for inlet and outlet manifolds, are etched in one wafer while the other is used as a cover exploiting the silicon fusion-bonding technique. Cooling is achieved by flowing a rad-hard coolant (C_6F_{14}) inside the micro-channels. A full-scale prototype and a vacuum test stand
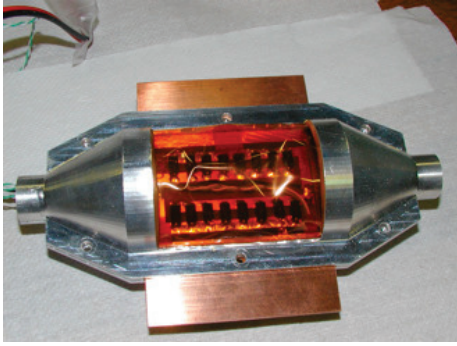
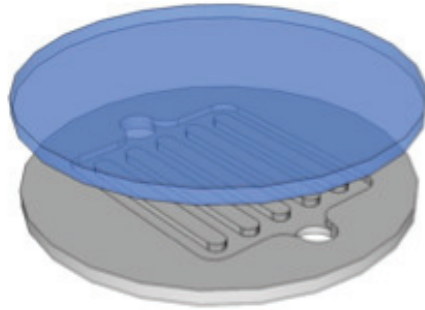Fig. 4. Picture of a prototype vessel cooling system.

Fig. 5. Schematic drawing of a micro-channel cooling plate, before bonding of the two wafers.

have been built, and work is ongoing to optimize the manifold geometry for pressure reduction and to thin down the wafer in the active area.

4. Read-out chip architectures

A careful compensation of the time-walk is necessary in order to achieve the required timing resolution, due to the high dynamic range (3600 to 60000 electrons). Two complementary read-out architectures have been implemented for the Gigatracker [4, 5].

The first one, named "End of Column" TDC option, is based on a Time-over-Threshold (ToT) discriminator placed in each pixel cell and connected to a Delay-Locked Loop (DLL) based TDC at the end of a pixel column. In this approach the analog front-end signals are discriminated inside the pixel cell and sent to the periphery of the pixel matrix, where the End-of-Column (EoC) circuitry performs the time measurement.

Time measurements of the leading and trailing edges are performed for each hit and the ToT of the signal is used offline to correct for the time-walk. Hit arrival time is measured using a DLL based TDC, operated at a base frequency of 320 MHz (32 buffers divide the period of 3.125 ns in bins of 98 ps). Groups of 5 pixels are multiplexed in a single hit register, leading to a global dead-time of less than 0.5%. A digital arbiter circuitry has been designed to send hit pulses to the TDC banks and block signals from the same group of 5 pixels in case they would overlap in time. These overlaps are flagged and the information is added to the output data stream. A schematic diagram of this architecture is shown in Fig 6.
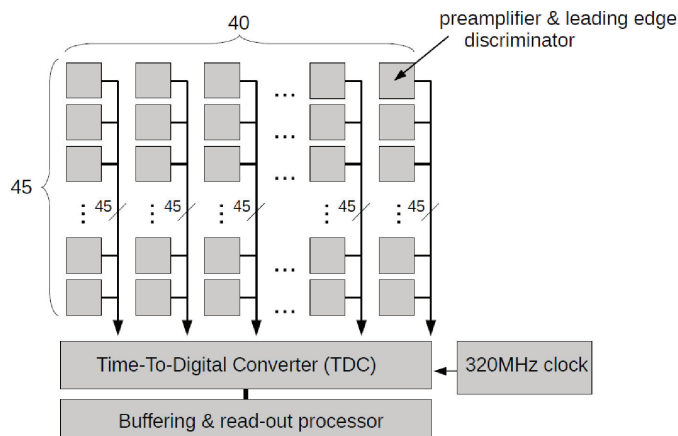

Fig. 6. Schematic diagram of the end-of-column TDC architecture.

The second architecture, called "On-pixel" TDC option, is based on a Constant Fraction Discriminator (CFD) in addition to a Time-to-Digital Converter (TDC), based on a Time-to-Amplitude Converter (TAC), implemented in each pixel cell. Correction of the time-walk is achieved through the CFD, which measures the zero crossing time of the difference between the original input signal and a delayed and attenuated copy of the same signal. When a hit is detected a coarse time measurement is latched into a digital buffer. In parallel the hit initiates a fine time measurement by triggering a ramp generator to charge a capacitor until the next clock trailing edge. The capacitor voltage corresponds to the fine time measurement and is converted to a digital value. The hit information (coarse time, fine time and pixel address) is stored into the output buffer before being transferred to the end-of-column logic at the periphery of the chip. A schematic drawing of this architecture is shown in Fig. 7.
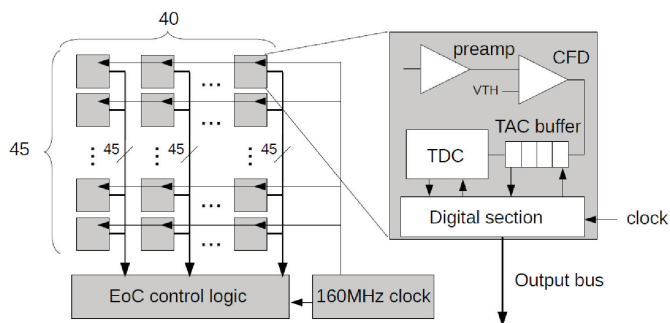
Fig. 7. Schematic pixel cell diagram for the on-pixel TDC option.

Small area prototype chips (for both architectures) have been produced in 0.13 μm IBM CMOS technology in 2009 and then bump-bonded and tested in 2010. After a careful design review, the NA62 Collaboration decided to adopt the "End of column" architecture as the baseline option. The decision has been based on the performance of the available prototype assemblies and also on the tight time schedule of the experiment (the start of the data taking is expected for 2014).

In the final version, the read-out chips will comprise 40 columns of 45 pixels each (1800 pixels per chip in total) and are designed for a maximum rate of 140 kHz per pixel. Key challenges for the chip design are the time resolution (200 ps per single hit), the fast on-pixel analog pulse shaping (5 ns peaking time) and the high data rate per chip (up to 8 Gb/s). A list of specifications for the final chip is shown in Table 1 and more detailed information on its design and implementation can be found in Ref. [6].

Pixel Matrix	40 columns × 45
Pixels per chip	1800
Chip size	12 mm × 19 mm
Dissipated power	~2 W/cm^2
Dynamic range	3600 - 60000 e- (0.6 - 10 fC)
Time resolution	< 200 ps
Peaking time	5 ns
Maximum rate per pixel	140 kHz
Maximum data bandwidth	8 Gb/s

Table 1. Gigatracker chip specifications.

5. Test of prototype assemblies

A systematic characterization of the prototype bump-bonded assemblies has been performed in 2010 and 2011. In this section only results that concern the EoC prototype option will be presented.
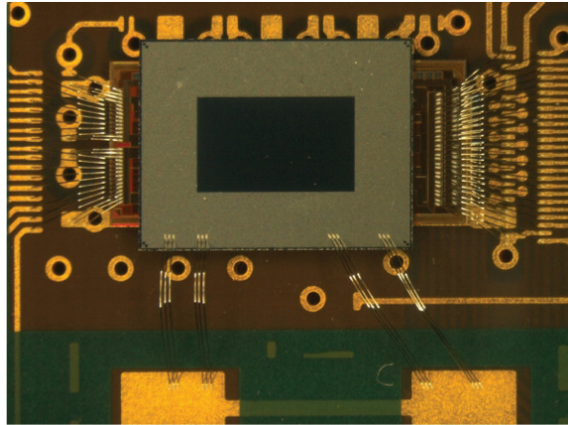

Fig. 8. Picture of one EoC prototype bump-bonded assembly, connected to the carrier read-out board. The rectangular opening in the back-side sensor metallization is clearly visible.

Extensive electrical characterizations on these prototypes (Fig. 8) have shown very low noise levels (~180 electrons) with the sensor bump-bonded to the chip [7].

A dedicated laser test setup has been built in order to characterize Gigatracker bump-bonded assemblies on a laboratory bench and in a repeatable way. Infra-red light (1060 nm wavelength) was used to illuminate the back-side of the sensor to emulate minimum ionizing particles. This system is characterized by a 5 ps global time precision, and hence represents an ideal tool to characterize fast detectors. Absolute calibration of the injected charge has been achieved using radioactive sources (e.g. ^{241}Am, ^{109}Cd).
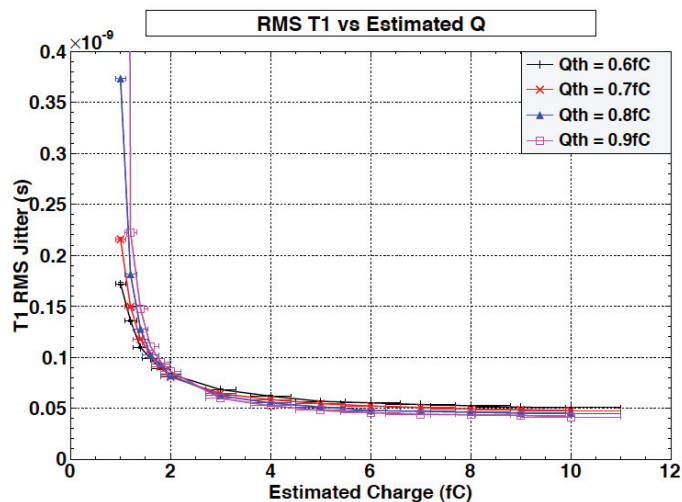

Fig. 9. Time resolution (jitter) as a function of the estimated injected charge (infra-red laser injection in the pixel center) for different pixel thresholds (the nominal one is 0.7 fC) .

One of the most important results obtained with the laser setup can be seen in Fig 9. A time resolution (jitter) of ~75 ps has been measured for an injected charge of 3 fC, which is the average charge generated by a minimum ionizing particle in 200 μm thick silicon. This value refers to a charge injection done at the pixel

center and for a sensor bias voltage of 300 V. In addition the laser system is installed on a X-Y-Z linear stage system with a few microns precision, that allows to measure the behavior of digitized time as a function of the impact position inside pixel (geometrical effect due to weighting field variations).

A test-beam was performed at CERN using 4 consecutive Gigatracker prototype assemblies aligned on the beam. Fast scintillators were used to provide an ultra-precise timing reference and a pixel-by-pixel Time-over-Threshold correction was applied offline to the GTK data. The main result of the test-beam is the measurement of a time resolution of ~175 ps for 300 V sensor bias voltage. The dependence of the time resolution on the sensor bias voltage has been investigated as well. Results (Fig 10) show a clear dependence and indicate that sensor operation at high over-depletion is mandatory.
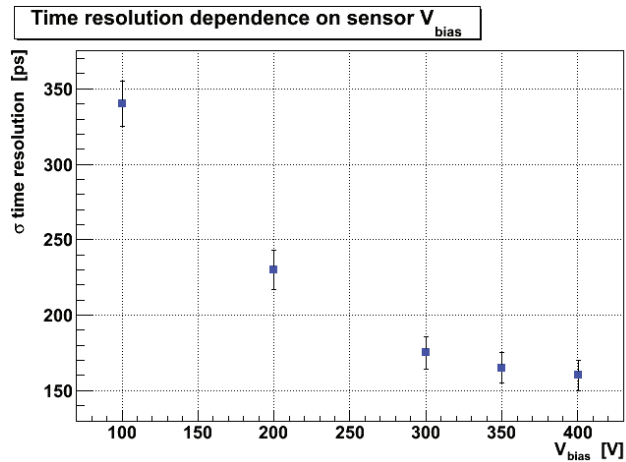

Fig. 10. Time resolution dependence on the sensor bias voltage.

At a first glance it might seem that the results on the time resolution coming from the laser test (~75 ps) and the test-beam (~175 ps) are fully incompatible. However, those numbers cannot be directly compared, because there are many different effects that enters in the beam measurement and not in the laser one.

A common effect in the laser and beam measurements of the time resolution is the one coming from the electronic noise of the front-end chip and from the sensor bias voltage, that has a direct effect on the variation of the charge collection time and thus on the signal slope. During the test-beam, the particle illumination of the pixel cell was rather uniform, while for the initial tests with the laser the light has been shone only on the pixel center. However, particles arriving at the same time and with different impact positions on the pixel will produce different measured times, due to the weighting field variation. In addition, for beam particles, energy straggling in the sensor bulk produces a non-uniform energy release along the sensor thickness plus delta rays departing from the main ionization trail, while for the laser a rather uniform (along the thickness) and constant (pulse-by-pulse) energy release is expected. A detailed study of the different contributions to the total detector time resolution is ongoing, including a complete scan of the detector surface with the laser and simulations of signal generation for laser and particle beams.

Conclusions

The NA62 Gigatracker detector system and a summary of the main results of the prototype bump-bonded assembly test have been presented. Extensive measurements, based on electrical and laser tests plus a dedicated test-beam, have been performed on EoC prototype assemblies. A time resolution of ~175 ps has been measured with minimum ionizing particles impinging on the sensor operated at 300 V bias voltage. The different contributions to the total time resolution are being quantified with specific simulations and measurements. Two very-low mass cooling systems (<0.15% X_0) are being developed in parallel. The first results on prototype versions are encouraging and a baseline cooling option for NA62 will be selected in the coming months.

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