Highly-Parallelized Pattern Matching Execution for the ATLAS Experiment

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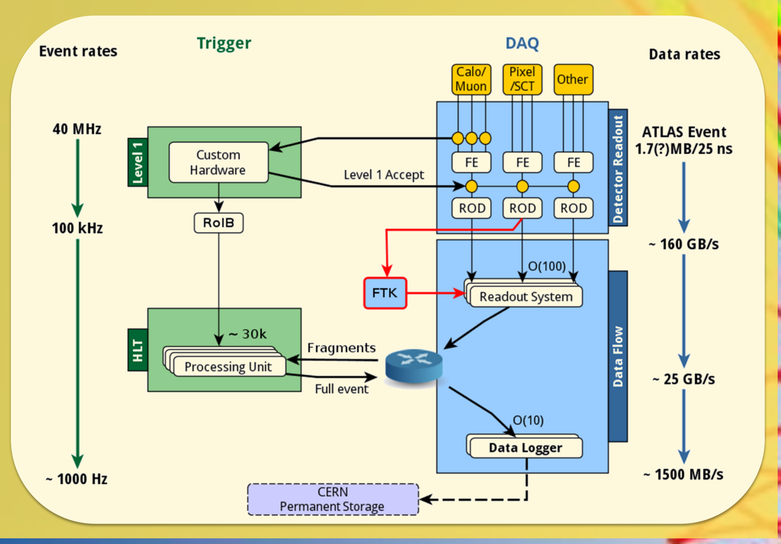
Abstract

The trigger system of the ATLAS experiment at LHC will improve the capability of the detectors to select the events with the greatest scientific potential. During operations in 2015-2018 will be introduced the Fast TracKer system (FTK). FTK is a hardware based system capable of finding charged particle tracks by analyzing hits in silicon detectors at the rate of 10^5 events per second. The core of track reconstruction is performed into two pipelined steps. At first step the candidate tracks are found by matching combination of low resolution hits to predefined patterns; then they are used in the second step to seed a more precise track fitting algorithm. The key FTK component is an Associative Memory (AM) system that is used to perform pattern matching with high degree of parallelism. The AM system implementation, the AM Serial Link Processor (SLP), is based on a powerful network of 2Gb/s serial links to sustain a huge traffic of data. The design of the AM SLP is reported. The AM SLP consists of two types of boards: the Little Associative Memory Board (LAMB), a mezzanine where the AM chips are mounted, and the Associative Memory Board (AMB), a 9U VME motherboard which hosts four LAMB daughterboards. We also report on the performance of the prototypes produced and tested in the global FTK integration, an important milestone to be satisfied before the construction of the final FTK system.

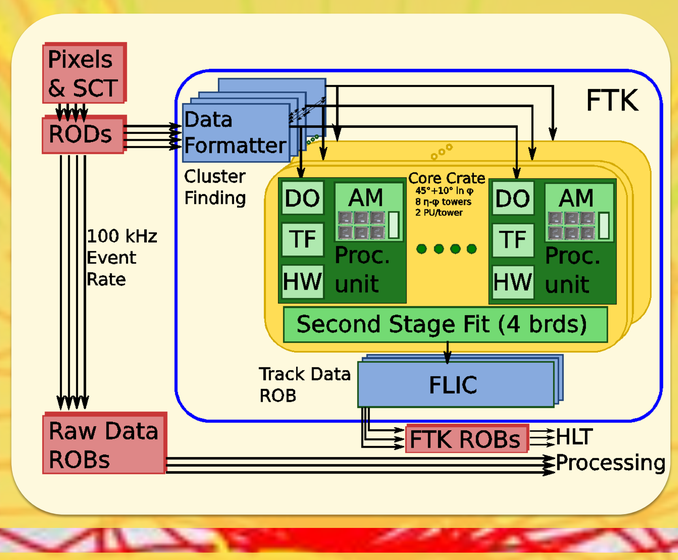
FTK in the ATLAS Trigger

The Fast Tracker processor [1] will receives data from pixel and microstrip ATLAS detectors for all events (bunch crossings with multi p – p collisions) accepted by the Level 1 trigger at 100kHz event rate **(~100GB/s**). It will reconstruct all events to provide in **~50 microseconds** all the tracks with transverse momentum above 1 GeV/c to the High-Level Trigger (HLT).



FTK Architecture

The FTK core is made of 128 Processing Units (PUs). The PU is composed of an Associative Memory board (AM) and an Auxiliary Card where the functions of the second step are executed: the Track Fitting (TF), the Data Organizer (DO), an interface between AM and TF, and the Hit Warrior (HW) able to remove the duplicated tracks found by the TF.

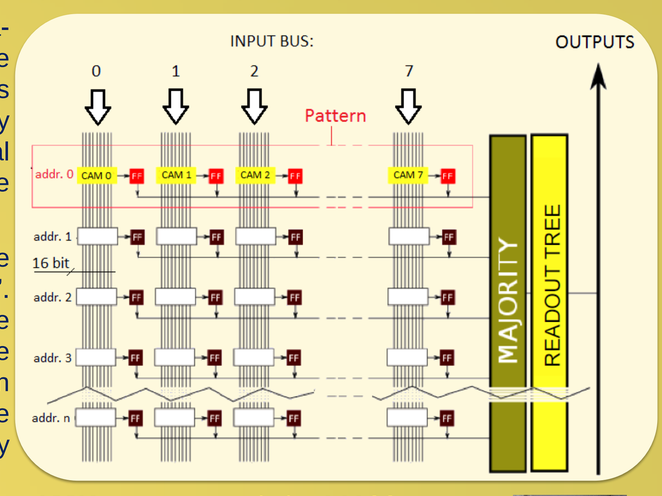


Associative Memory (AM) Chip

The AMchip[3] is composed of a matrix of Custom Content addressable memory cells. Pre-computed patterns are stored in the AM chips. Pattern is made by 8 data-word each one referred to one silicon layer (5 SCT and 3 Pixel). The 8 channels are compared in parallel and independently in each clock cycle

If the 8 received data-words match with the pattern, its address is readout. The majority logic allows partial matches to increase the efficiency.

Pattern layers have "variable resolution". "Don't care bits" can be set to decrease in the layer word resolution, in order to decrease the amount of unnecessary stored data.



- The AMchip 06 will store **128K patterns** made by **144 bits**
- One AMchip 06 will perform **~2 *10^{18} bit match** per second
- The Energy for a bit match is **~1.5 fJ/bit/search**

AM boards

The AM system is made by 128 AM Serial Link Processors (AMBSLPs). The AMBSLP is composed of a motherboard (VME 9U) with 4 daughterboards, that holds 64 AMchips.

The main purpose of the AMBSLP is to distribute the inputs to all the **64 AMchips** (blue arrows). This data distribution is controlled by an FPGA (blue square).

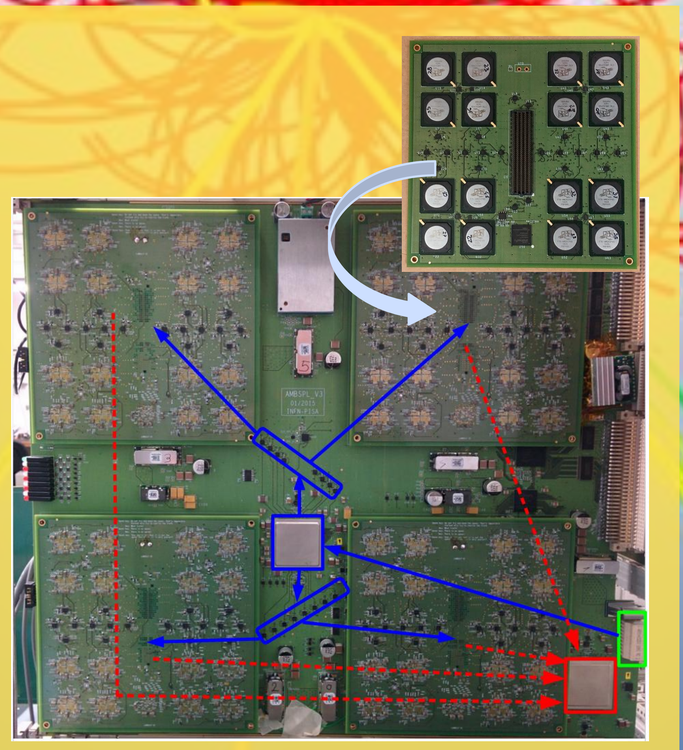
The patterns are collected and sent to the AMBSLP output by another FPGA (red square and red arrows).

Both the large FPGAs execute monitoring and error detection functions. Monitor data and error flags are also added to the output stream.

Input and output data are transmitted on 2Gb/s serial links.

The AMBSLP has **~850 serial links**, with **~1 Tb/s** of global data traffic.

- The AM system will perform **120 Peta bit match per second**
- Power consumption is **250 W**
- In the AM system ~**2.07fJ/bit/search** are needed

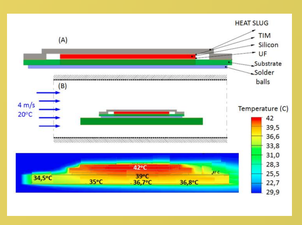


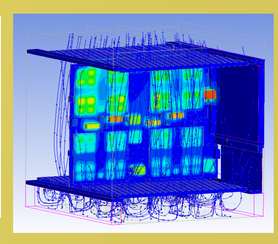
Temperature Simulation and Test

Crate and AMchip die Temperature (T) simulations done with IMEC.

The AMchip package and board design **have been optimized** in order to increase dissipating heat **with the PCB** and the air. From the simulation the highest T in the PCBs is expected **~90°C and the T of the AM die is few degree more than the PCB T.**

Temperature measurements were done in USA15 (Electronic cavern of ATLAS) with old AM chips dissipating more than the new ones.





The USA15 setup was a realistic reproduction of the final environment of the system.

In the measurement we added a second fan placed above the crate. We obtained in this final condition **~10°C less** than the simulation reports.

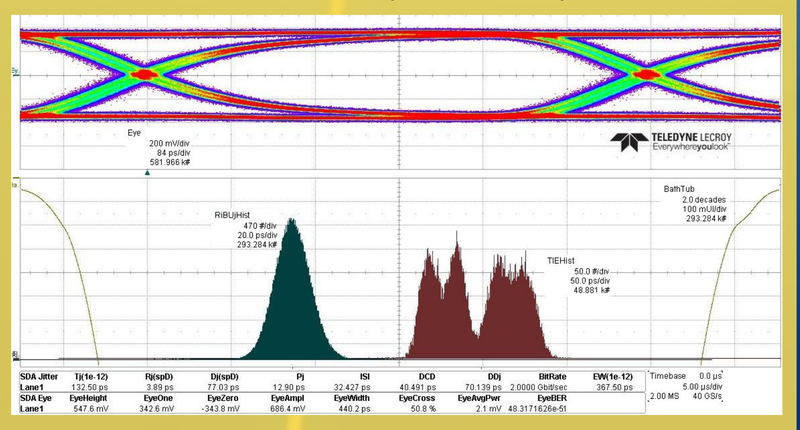
Test and measurements on AM boards

In order to validate the AM system, functional tests were performed using **random data**. With a computer simulation, patterns to store in the AM chips and the input data to send are created. At the end of the process a comparison is made between the output of the simulation and the real output.

In addiction, a quality investigation was performed on all the serial links on the boards. Pseudorandom binary sequence (**PRBS**) was sent on all links and with each receiver were checked the number of errors.

This test was run for 3 days continuously and the Bit Error Rate (**BER)** found is **≤ 2 * 10^{-15}** It is limited by the running time of the measurements.

A quality analysis is also made with an oscilloscope, and the estimated **BER ≤ 48 * 10^{-51}**



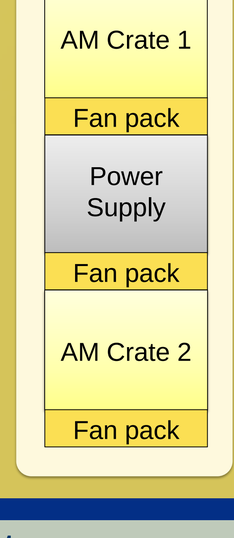
Power Supply

In one rack will be installed 32 AM board spitted in two crates. These means ~ 5kW per crate, so in one rack we will need **10kW**.

In order to meet this constraint a **16kW** custom power supply is designed:

- **48 V** **300 A**
- **5 V** **240 A**
- **24 V** **60 A**

The Power supply is also connected to the Detector Control System, in order to monitor and control it from the control room.



Results

We designed a massive pattern matching computing unit, paying attention on power consumption and signal integrity. We tested systematically all the serial links internal to the AM board, reaching very low rate of BER. To test the global functionality of the system we use a "Random Test" that generates events containing random input data in order to test rare conditions that could escape standard specific systematic tests. After these tests the board has been integrated in the FTK Global Integration test at CERN. Production has to be installed in the experiment to take data for the first time at the end of 2015.

References

[1] Andreani et al., The FastTracker Real Time Processor and Its Impact on Muon Isolation, Tau and b-Jet Online Selections at ATLAS, 2012 TNS Vol.: 59 , Issue:2, pp, 348 – 357

[2] The FTK collaboration, "Technical Design Report Fast TracKer (FTK)" CERN-LHCC-2013-007 ATLAS-TDR-021 available online: https://cds.cern.ch/record/1552953/files/ATLAS-TDR-021.pdf

[3] A. Annovi, et al., "Associative memory design for the Fast TracK processor (FTK) at Atlas," in IEEE NSS/MIC, 2009, Orlando, pp. 1866 – 1867.

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