The Evolution of the Region of Interest Builder in the ATLAS Experiment at CERN

Othmane Rifki (University of Oklahoma),
R. Blair, G. Crone, B. Green, J. Love, J. Proudfoot, W. P. Vazquez, W. Vandelli, J. Zhang

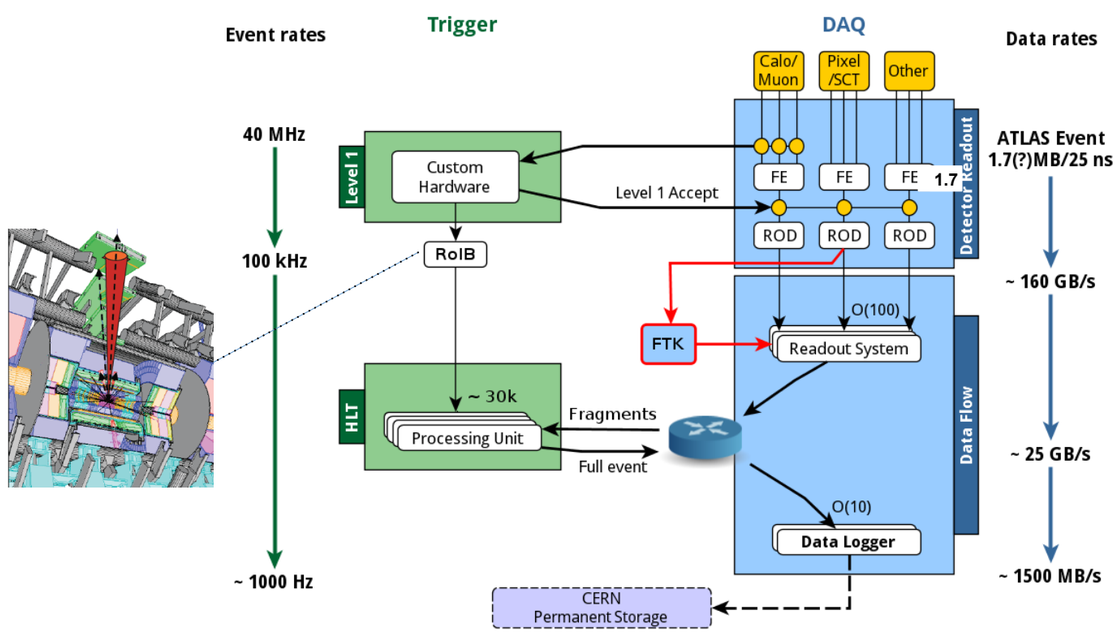
Abstract

The ATLAS detector at CERN employs a combination of hardware and software triggers to select interesting collisions for physics analysis. The Region of Interest Builder (RoIB) [1] is part of the ATLAS Trigger and Data Acquisition (TDAQ) system where it collects coordinates of the regions of interest (RoIs) identified by the first level trigger (L1) and pass them to the High Level Trigger (HLT) to make a decision. Due to the increase in luminosity and complexity of L1 triggers, the custom VME based RoIB was replaced with a single PCI-Express card in a commodity PC. In the ATLAS TDAQ testbed at CERN, the HLT is reading out 12 channels with fragment size of 100 32 bit words at a rate above 100 kHz.

Challenges of TDAQ System

- **Short bunch-crossing period** (25ns): It is shorter than the time it takes particles travelling at the speed of light to traverse the detector;
- **High rate of interactions per bunch crossing** (pile-up): The pile-up events add to the volume of data to be read out and complicate the task of recognizing signatures of interesting interactions;
- **Very high trigger selectivity**: The interaction rate of 10^9 Hz (bunch crossing rate of 40 MHz) has to be reduced to 10^3 Hz for recording on permanent storage;
- **Rare physics processes**: The interesting events should be selected with high efficiency. For example, only about 1 interaction in 10^{13} would give rise to a Higgs boson decaying into four leptons.

TDAQ System Architecture



The RoIB guides the HLT by building an event fragment with the RoIs used by the HLT to retrieve partial information from the Readout System (ROS) and thus eliminating the need to make a trigger decision based on the full detector readout which will be technically challenging and expensive at high rates.

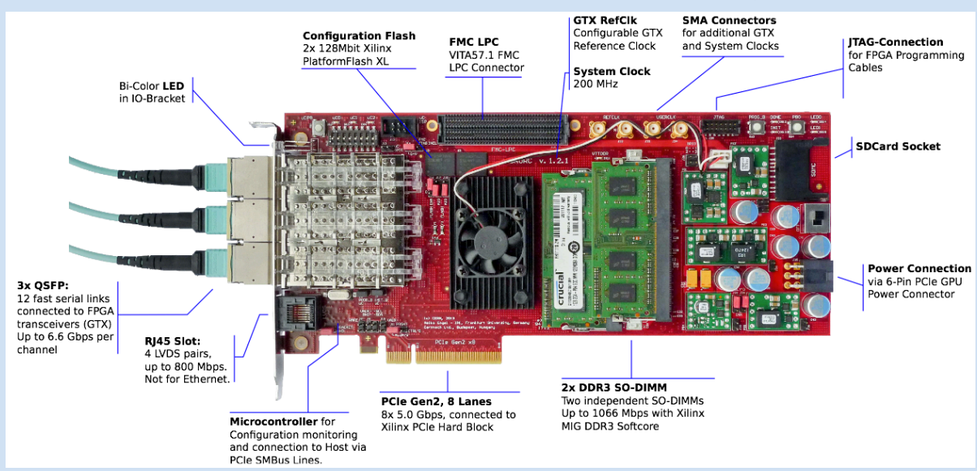
Current RoIB

- Uses custom electronics on a VME architecture;
- Backplane operates at 20 MHz and transfers 16 data bits per clock cycle for up to 12 inputs;
- Maximum data throughput: 40 MB/s per link;
- For 100 32 bit words and 8 channels, the current RoIB rate is around 60 kHz. The current system does not satisfy the required 100 kHz.

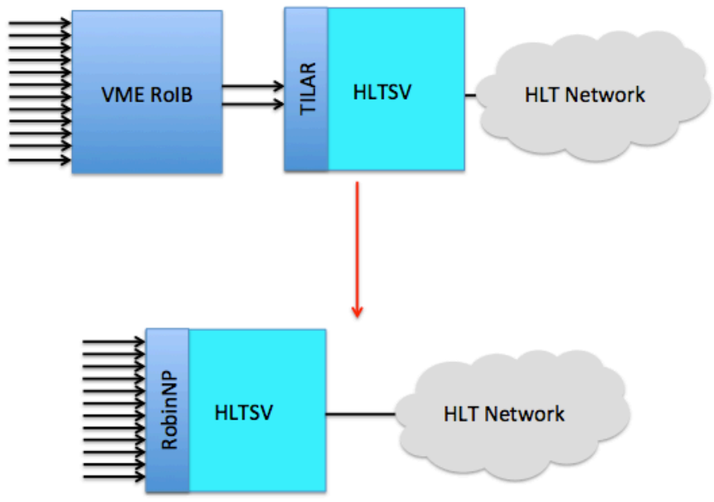
New RoIB

The new RoIB is based on a custom board, the C-RORC [2], developed by the ALICE collaboration that uses the ATLAS readout buffer software and firmware, called the RobinNP, and which has the following characteristics

- PCI Express 8 x lanes card with up to 200MB/s per link;
- FPGA: Xilinx Virtex-6 @ 125MHz;
- Buffer memory: DDR3-1600 SO-DIMM RAM 2x4GB;
- 3 QSFPs: optical patch cords with 4 fiber pairs in each using the S-Link protocol.



RoIB Evolution



HLT Supervisor (HLTSV):

- Manages the HLT processing farm;
- Receives L1 results from the RoIB;
- Assigns events to HLT nodes and handles bookkeeping;
- Runs on a host PC.

Goals:

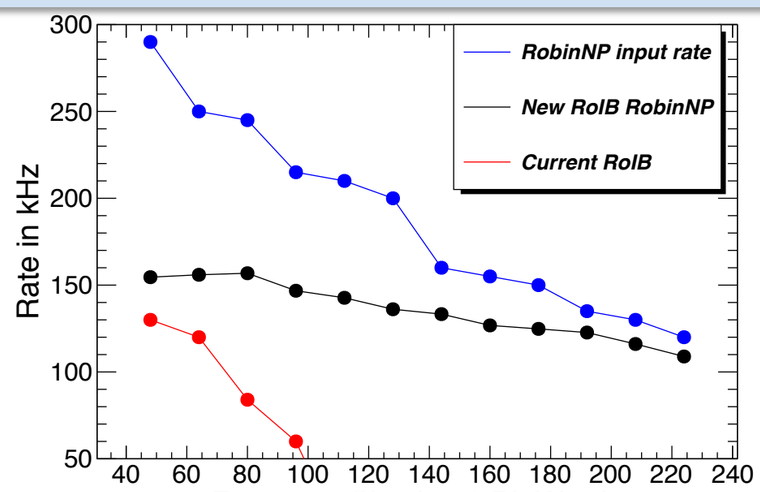
- Absorb the RoIB function in the HLTSV;
- Replace the custom made VME bus system of the RoIB with the RobinNP PCIe card in the HLTSV;
- Achieve over 100 kHz readout rate with the full ATLAS TDAQ system;

Tools:

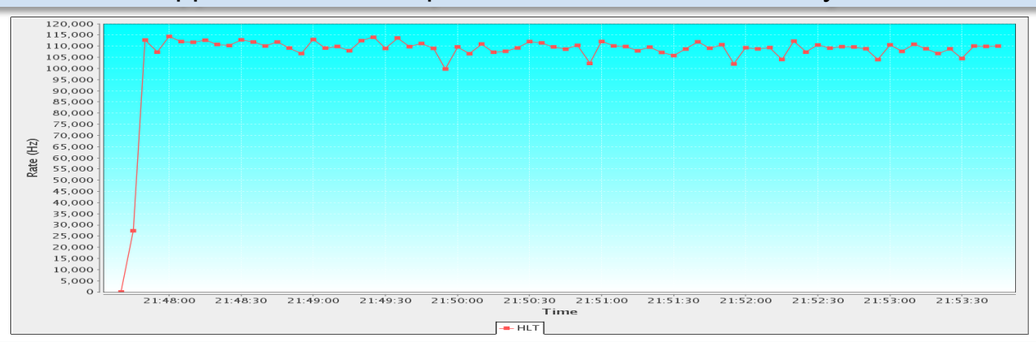
- Intel(R) Xeon(R) CPU E5-1650 v2 @ 3.5 GHz with 6 cores;
- Intel threading building block (TBB) library for concurrent event building.

Performance

The performance is tested using a standalone RobinNP application and an external source that emulates L1 trigger decisions in form of RoIs of 32 bit words with 12 channels.



We have seen an event building rate of over 100 kHz with 100 32 bit word fragments with the HLTSV application in a setup close to the ATLAS TDAQ system.



Outlook

The new RobinNP based RoIB will add stability and flexibility to the ATLAS TDAQ system where cards can be replaced or added to increase the number of channels while maintaining high readout rates.
A full integration test of the readout performance of the ATLAS TDAQ with the RobinNP RoIB will be performed during the end of this year's LHC shutdown.

References

[1] The ATLAS High Level Trigger Region of Interest Builder, arXiv:0711.3217
[2] The C-RORC PCIe Card and its Application in the ALICE and ATLAS Experiments, ATL-DAQ-PROC-2014-039