QIE12: A New High-Performance ASIC For the ATLAS TileCal Upgrade

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On Behalf of the ATLAS Tile Calorimeter System

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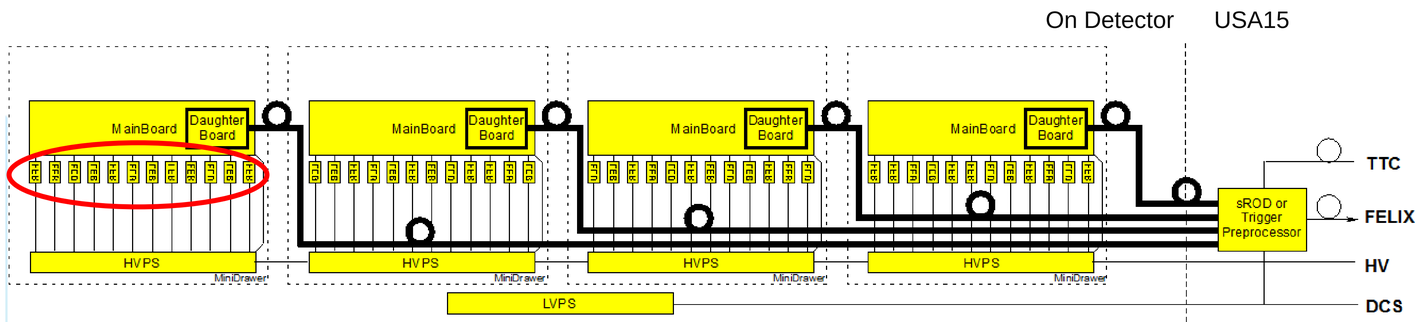
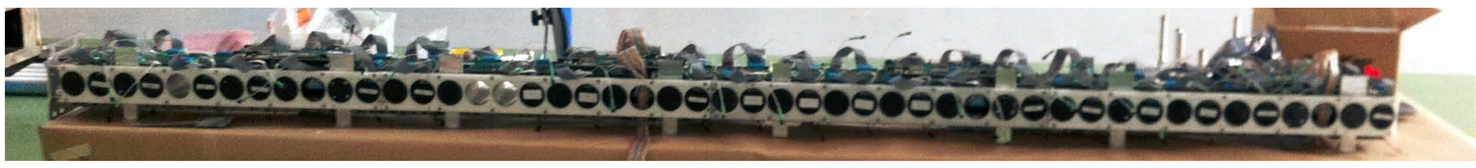
The TileCal Upgrade Readout Architecture

- **Prototype Development Program for the Phase 2 Upgrade**
- **Replacement of All Front-End & Back-End Electronics**
- **3 Front-End Technologies being Considered for PMT Readout :**
  - **3-in-1 (Discrete Design)**
  - **FATALIC (Custom ASIC)**
  - ***QIE: Charge Integrator and Encoder***
    - ***Custom ASIC, 350 nm SiGe***

⇨ ***Designs in Progress***
⇨ ***Test Beam Starting***
⇨ ***Technology Decision: Summer, 2016***



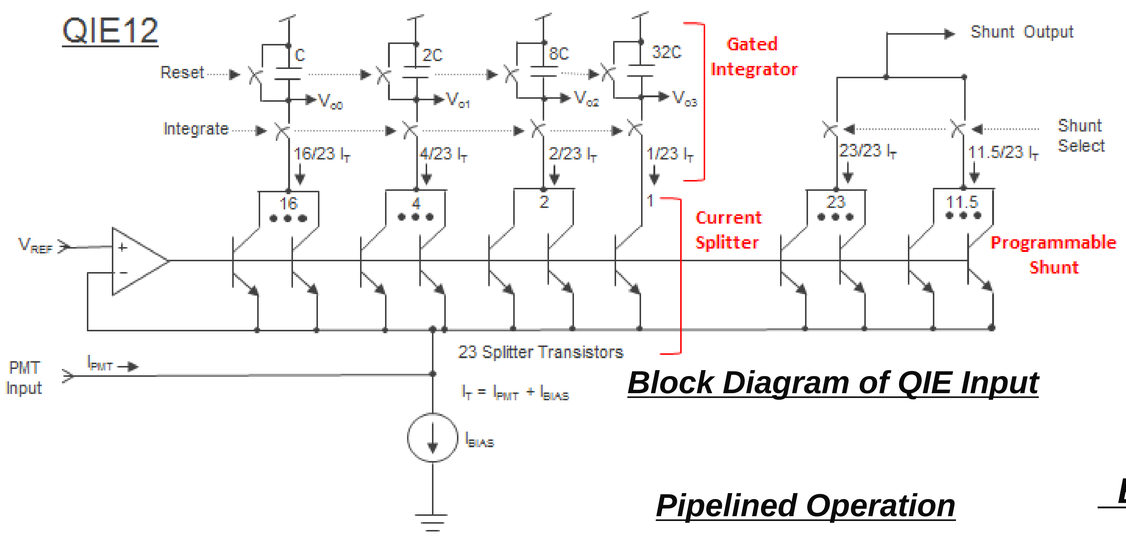


Front-End Components

- **Front-End Main Board**
  - **Analog & Digital**
- **Front-End Board**
  - **Analog & Digital**
- **Daughter Board**
  - **Kintex-7 FPGA**
- **Optical Link (Luxtera)**
  - **Analog & Digital**
- **HV Control Board**
  - **Analog & Digital**
- **Low Voltage Power**
  - **Analog & Digital**
- **COTS POL Regulators**
  - **Analog & Digital**

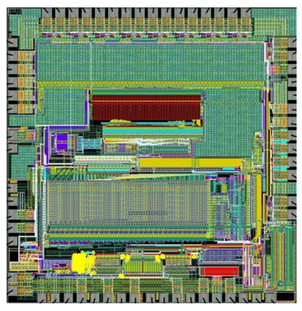
Overview of the QIE12

- **General Features of the QIE12**
  - **"Current Splitter" with Gated Integrator**
    - *No Pulse Shaping*
    - *Pseudo-Logarithmic Response*
  - **Pipelined Operation; Dead-timeless at 40 MHz**
  - **18-bits Dynamic Range**
  - **1.5 - 3 fC Least Count**
  - **Internal TDC → 1 nS resolution**
  - **Internal Shunt for External Current Integrator**
  - **Internal Charge Injection**
  - **Low Power – 360 mW/ch (Chip Only)**
  - **Highly Integrated; Simple Interface & Support Circuitry → High Reliability**
  - **Radiation Tolerant (SiGe Process for TID; SEU-Tolerant Design)**
  - **50 Ohm Input, Incorporate SPI for Slow Control**
    - Allows for one data bus for all slow control functions: Integrator ADC; Q Inj DAC, QIE

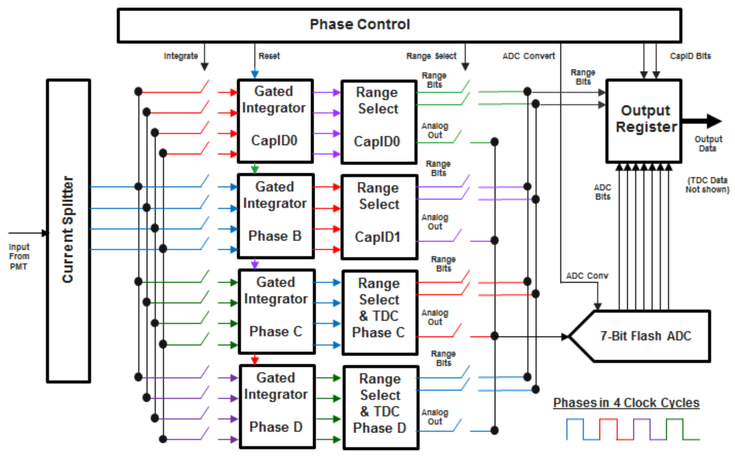


Block Diagram of QIE Input

QIE12 Chip layout

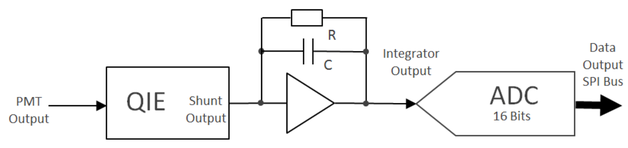


Pipelined Operation

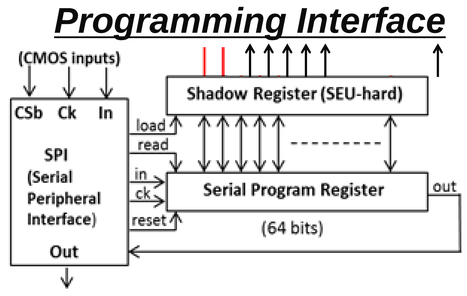


Current Integrator Implementation

(External to Chip)

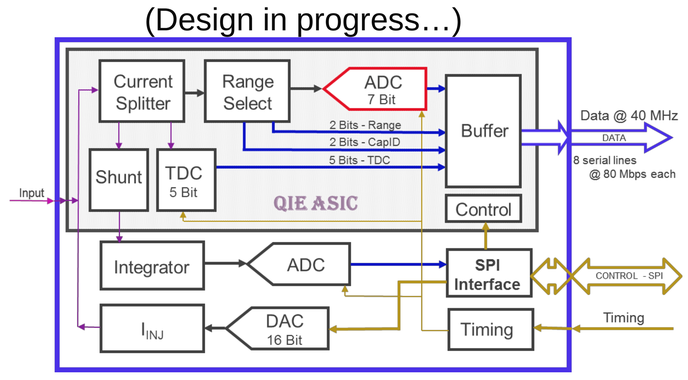


Programming Interface



Block Diagram of QIE Front-End Board

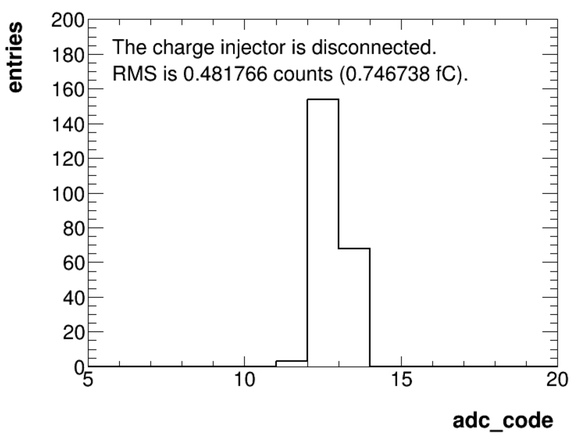
(Design in progress…)



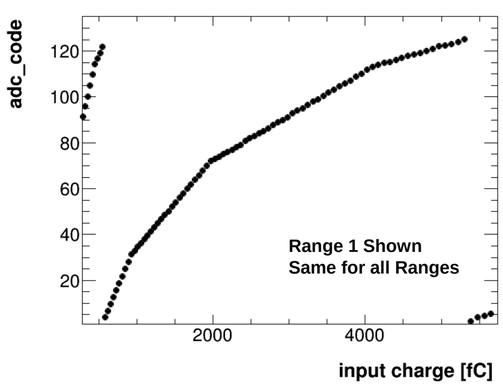
⇨ ***Simple Front-End***
⇨ ***Goal: Robust; High Reliability***

A Few Measurements & Results on Prototype Chips

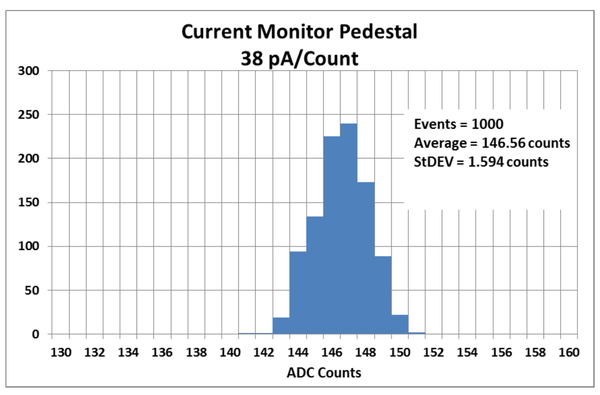
Pedestal Noise



ADC Transfer Function

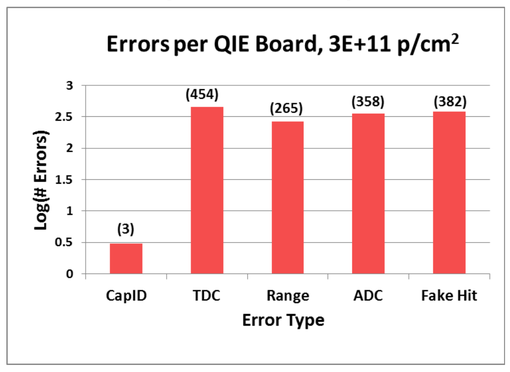


DC Current Monitor

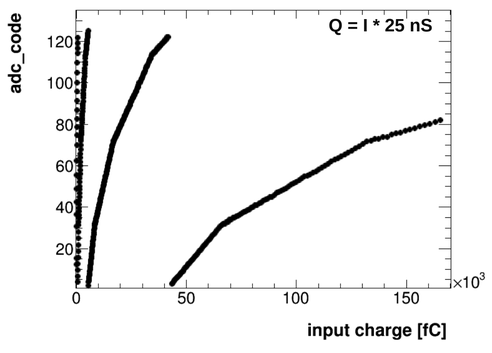


Current SEE Performance

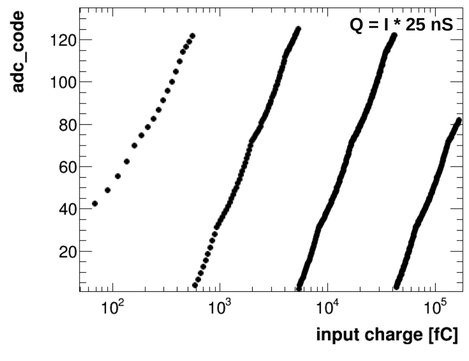
~ 1 SEU Error per 3E+8 p/cm² per chip
~1 Fake Hit per 1E+9 p/cm² per chip
No Errors in Shadow Register (SEU-Hard)
Est 10 yr Dose: ~4E+9 p/cm²



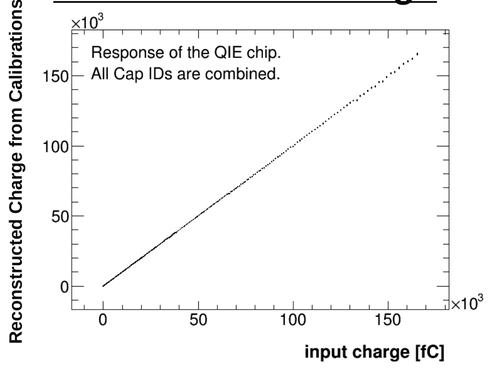
Current Injection – Linear scale



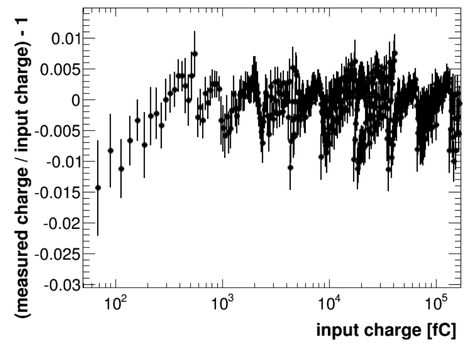
Current Injection – Log scale



Reconstructed Charge



Linearity Residuals



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