FATALIC:

A Dedicated Front-End ASIC

for the ATLAS TileCal Upgrade

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(on behalf of the ATLAS Tile Calorimeter system)

TWEPP 2015

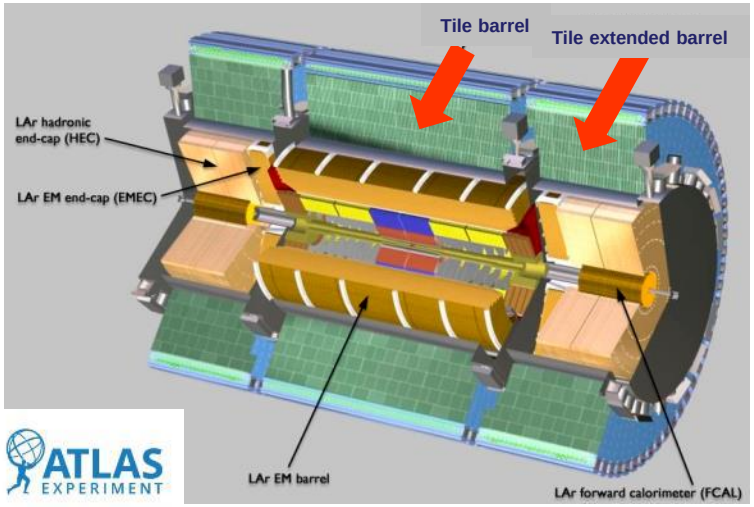
Topical Workshop on Electronics for Particle Physics

28 September - 02 October 2015
IST - Lisbon - Portugal

Outline

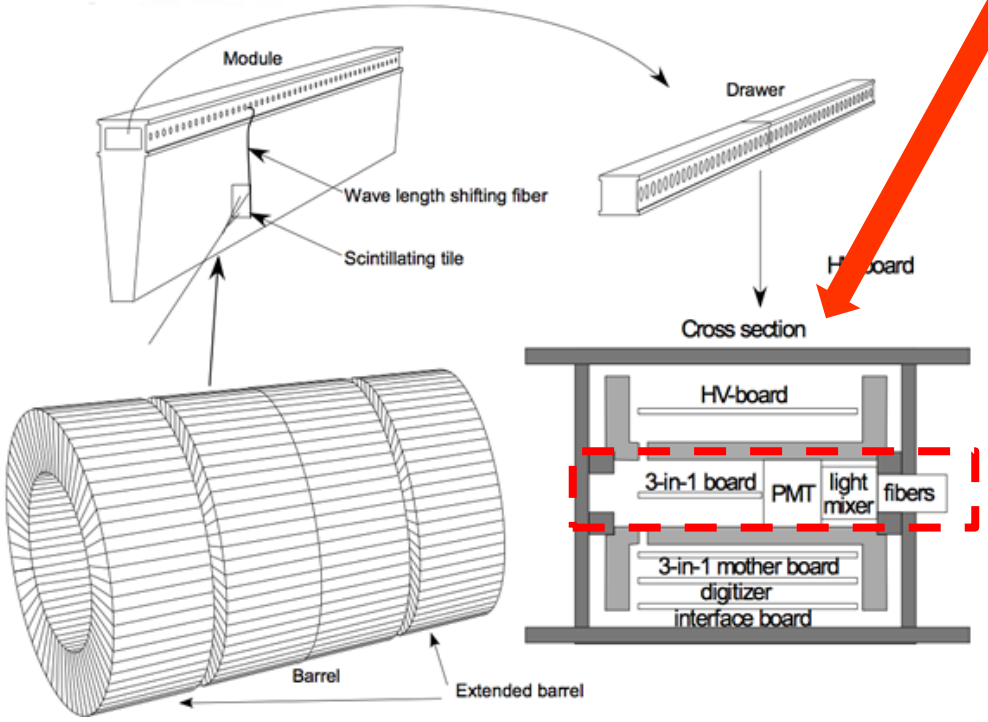
1. **Readout electronics of the Tile Calorimeter of Atlas**
2. The FATALIC ASIC
3. Performance of FATALIC
4. Summary and Outlooks

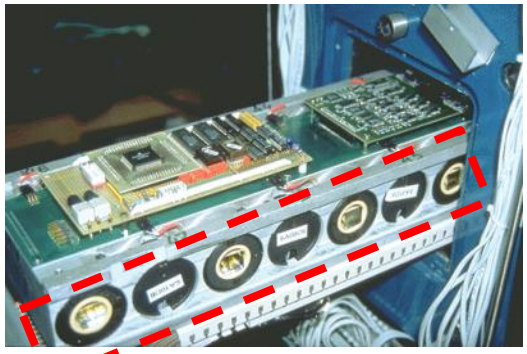
The ATLAS Tile Calorimeter



- The TileCal in a few words:
  - the **central hadronic calorimeter** of the ATLAS experiment;
  - segmentation: modules grouped in **barrels**,
  - active sensors: **plastic scintillator tiles** embedded in a steel absorber structure;
  - readout chain located in **drawers**:

    fibers → PMTs → readout electronics
  - about 16-bit dynamic range (single PMT):
    - 16 MeV (1pe) → few TeV
    - 24 fC → few nC





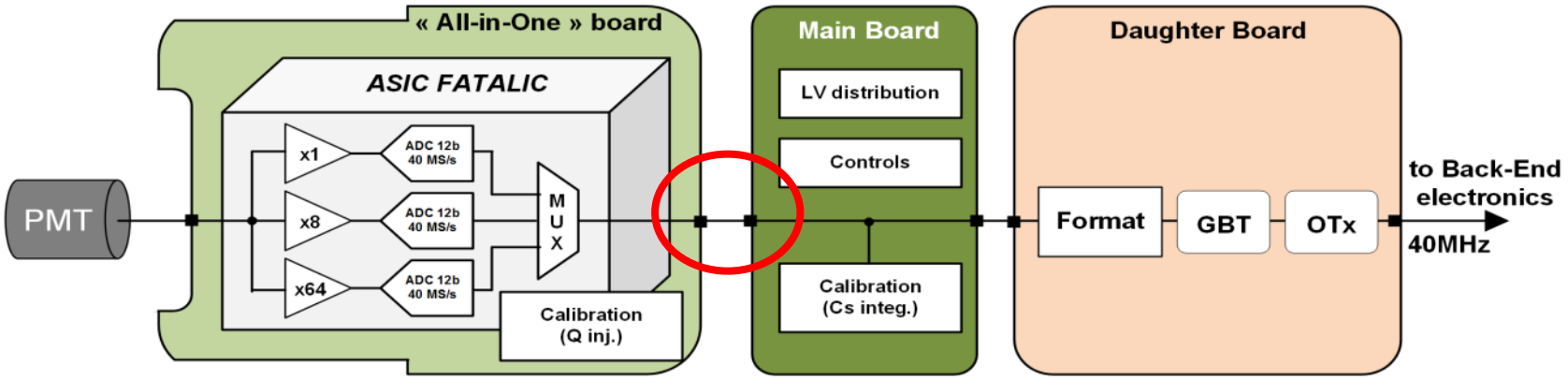
Motivations for the Tile upgrade

Two key issues:

- to cope with **HiLumi-LHC** constraints expected in 2023:
  - **2023: end-of-life** of the current system (obsolescence of electronics)
  - A better **radiation tolerance** (≈ TID of 50 krad at the barrel level)
  - A more **powerful trigger** across whole ATLAS detector
- to **improve** the current system:
  - **simplify** the **operation** of the detector
  - **improve** the **reliability**: maintenance more difficult due to higher radiation level
  - **facilitate** the operation of **maintenance**, increase serviceability
  - **increase** the **dynamic range** to be able to observe very high energy events in each cell

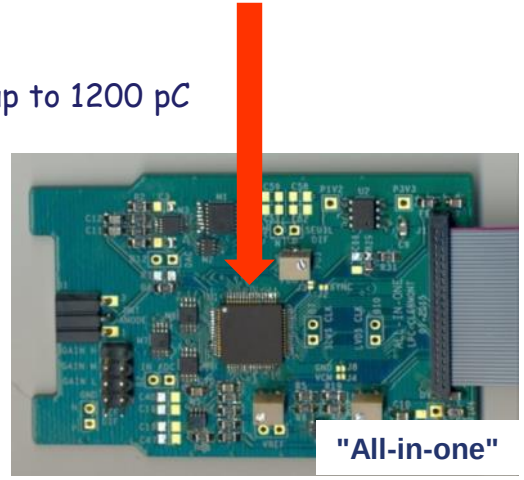
The Read-out electronics upgrade

Simplified view of the proposed upgraded readout electronics



Readout electronics composed of 3 boards: "**All-in-One**" → Main B. → Daughter B.

- "**All-in-One**" board: **PMT signal processing** thanks to a **Tile-Specific Integrated Circuit: FATALIC**
  - → **key issues**: performance, reliability, rad-tolerance, energy-efficiency
  - → 3 gain-channels with at least 10-bit precision ADC to extend the dynamic range up to 1200 pC
  - → early embedded digitization reduce constraints **on cabling** and on MB
- **Main Board**: data coding + LV distribution + controls + Cs calibration
  - → "pure" digital board: no transmission and "handling" of analog **sensitive** signal
  - → simplified design, reduced cost, increased robustness
- **Daughter board** (C.Bohm's talk):
  - → high speed optical communication for transmission of full data at 40 Mbps out of the detector



This system allows a digital triggering and a digital integration for Cs calibration

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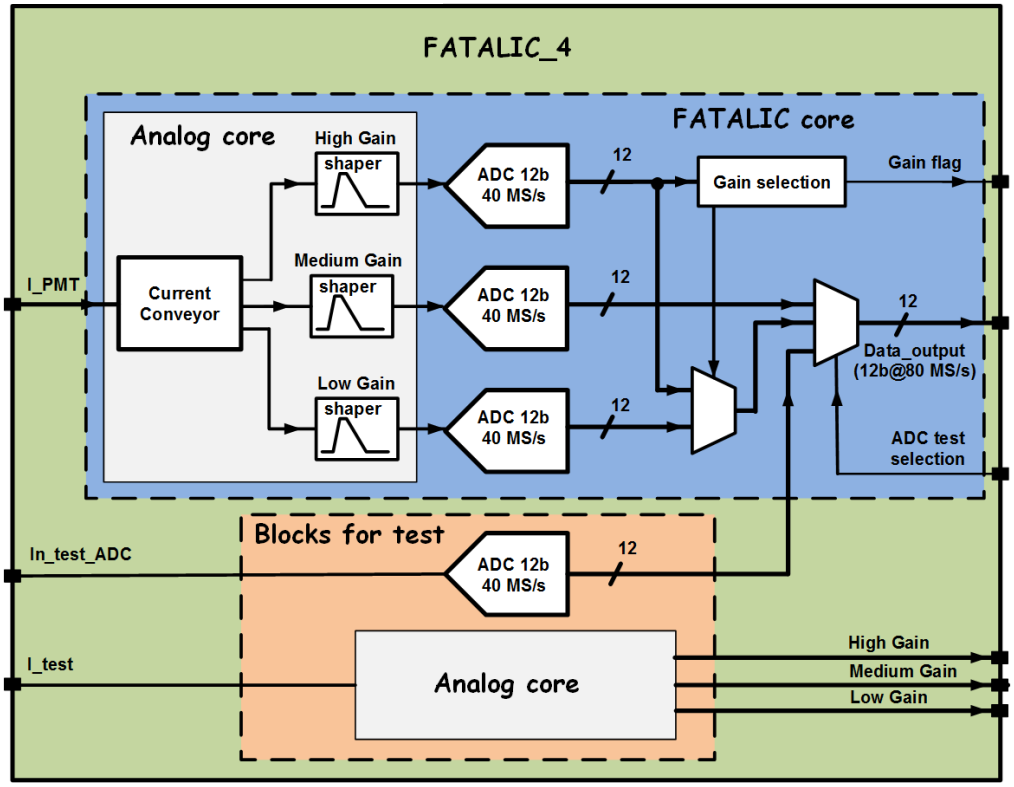
The FATALIC ASIC

The FATALIC chip embeds:

- An **analog-processing** block with:
  - a current conveyor which "reads" and "duplicates" the PMT current pulse to cover the dynamic range with 3 gain-channels
  - 3x RC-shapers (one per channel)
- An **analog-to-digital conversion**
  - 12-bit 40 MS/s ADC
  - one single ADC per channel
- A **digital processing**
  - Pipeline ADC data processing (1.5bit/stage algo.)
  - An auto-selection of the data to be transmitted
    → Medium gain AND (Low OR High gain) data
  - 80Mb/s output data multiplexing

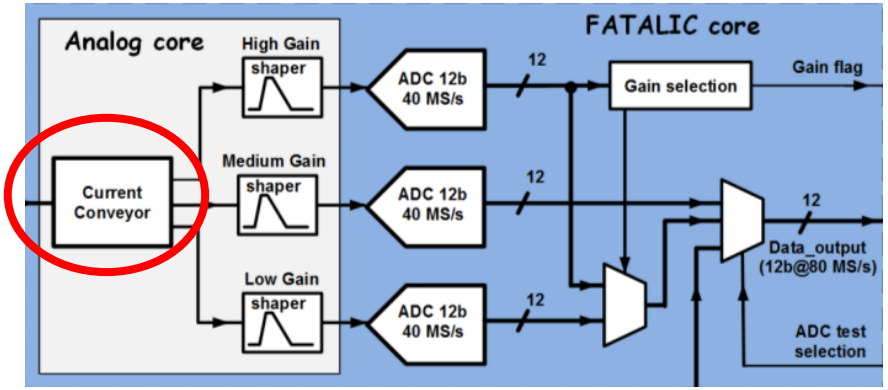


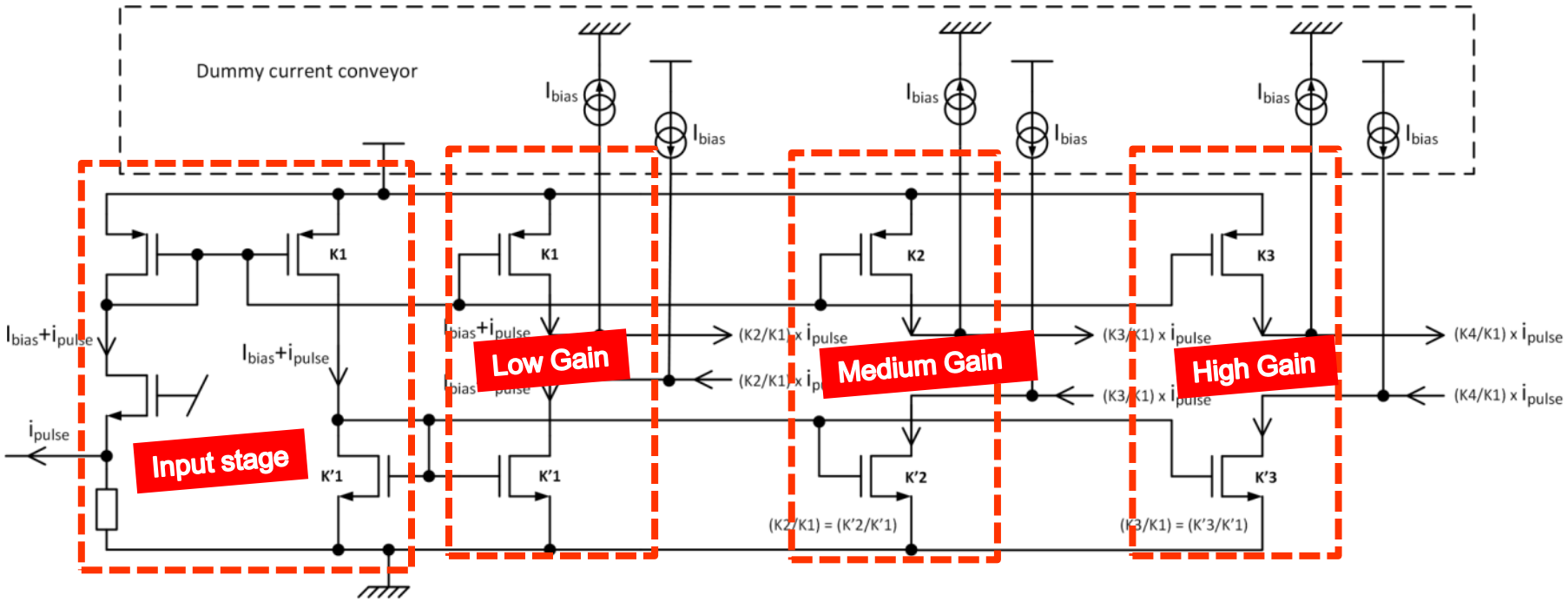
- Two replica blocks for test purpose: analog core and one ADC
- Power consumption limited to **205mW** with a **single power voltage** (1.6V)
- FATALIC has been designed with the IBM CMOS 130nm, characterized for his rad-tolerance by Cern

Radiation tolerance of the 130nm technology CMRF8SF
Results from TID2 test vector
15 September 2006
F.Faccio, L.Gonella
CERN/PH dept, MIC group

The current conveyor

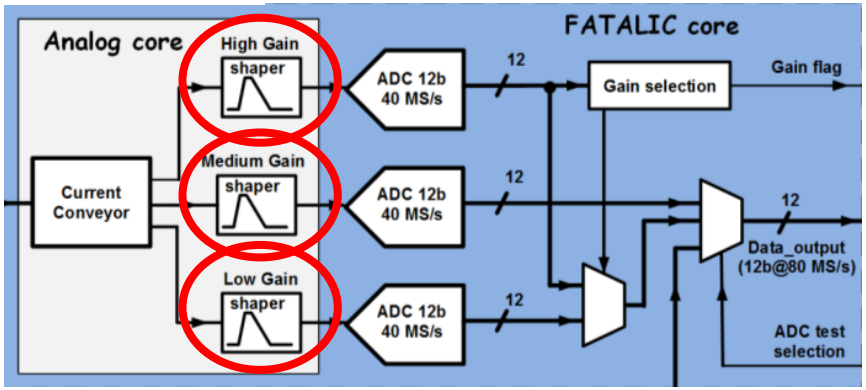
- The input stage:
  - a low impedance common-gate input (<20Ω)
  - A copy of the current to the amplifying stages
- 3 current-amplification stages:
  - factor of amplification given by the size ratio between master and slave transistors (Kx/K1)
  - differential output
- A dummy structure of the current conveyor is used to remove the biasing current

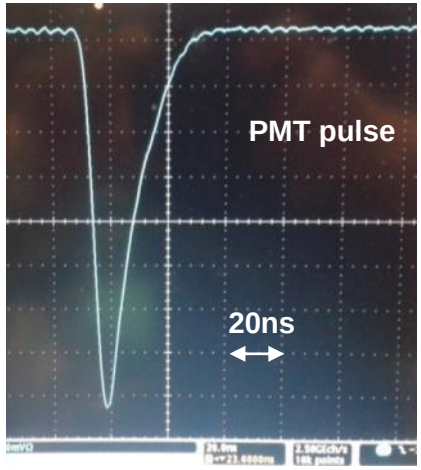


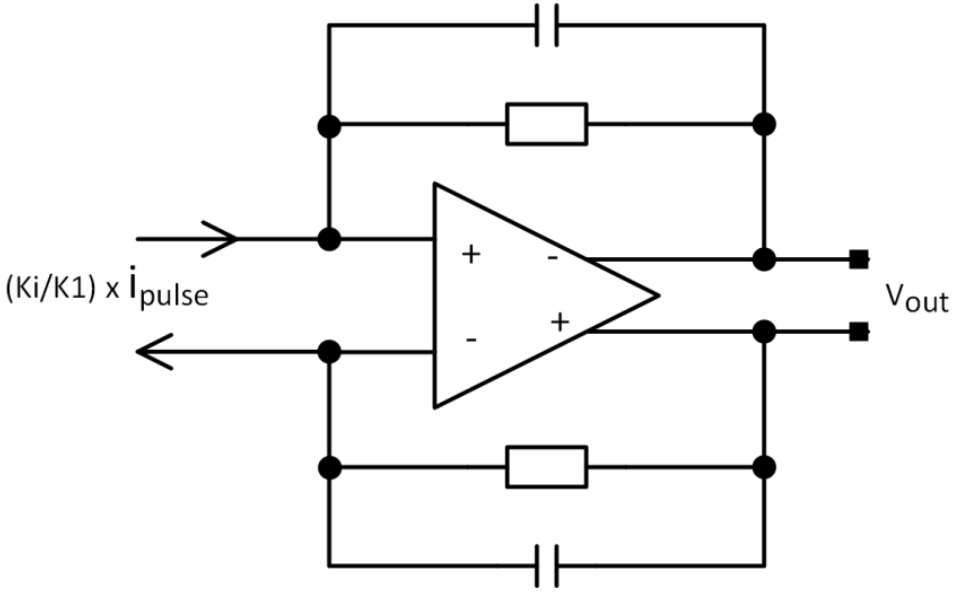


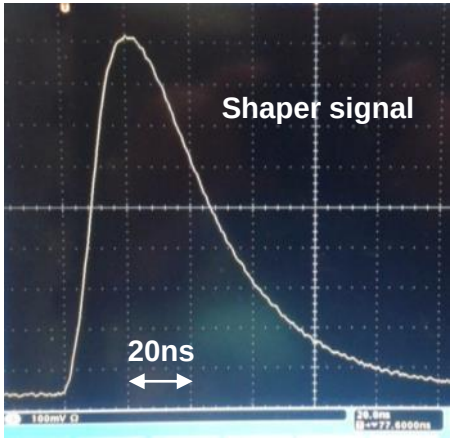
The shaper

- The shaper has a dual function:
  - Transimpedance amplifier
  - Integration of the PMT-pulse
- Peaking time (with typ. PMT pulse): ≈ 22ns
- Identical shaper for the 3 gain-channels
- Noise (Current-Conveyor + Shaper): < 500µV rms (7 fC rms)



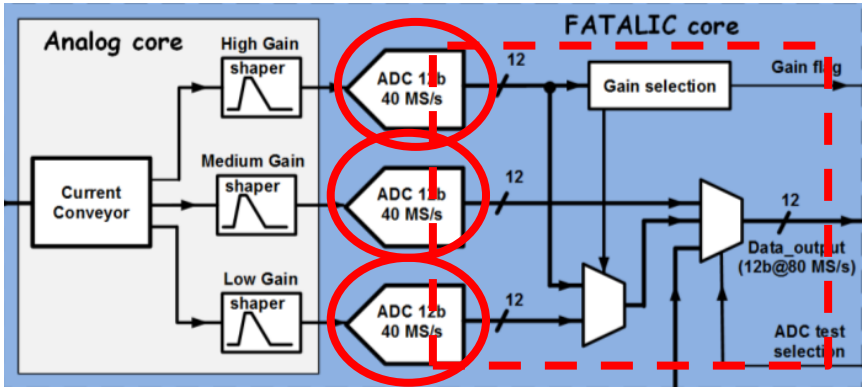




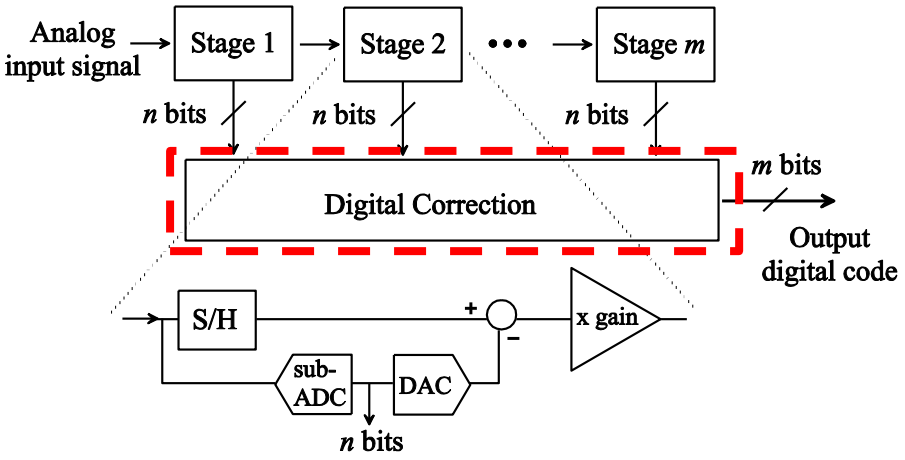


The Analog-to-Digital Converter
and the digital block

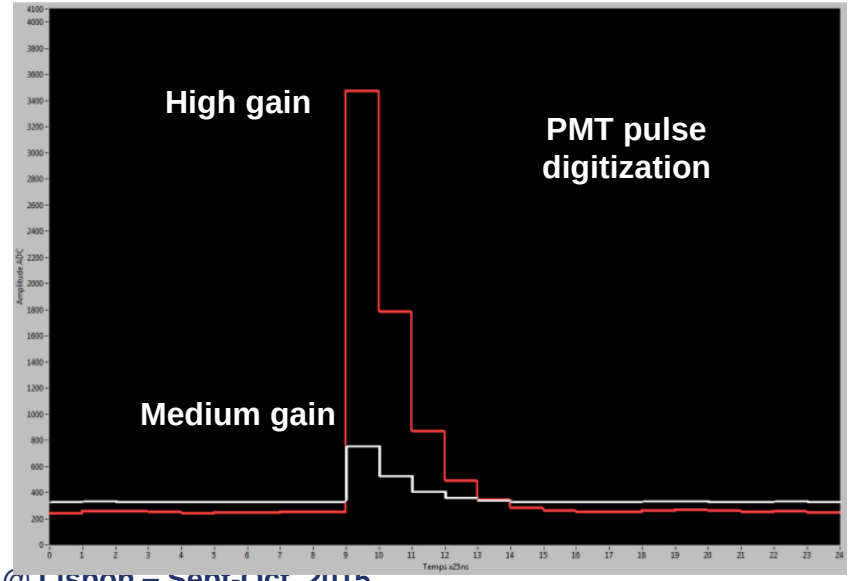
- A "classical" 1.5bit/stage pipeline ADC architecture
  - 12-bit resolution @ 40MS/s
  - < 0.1% error amplification (x2) precision required:
    - high performance OTA
    - good capacitor matching



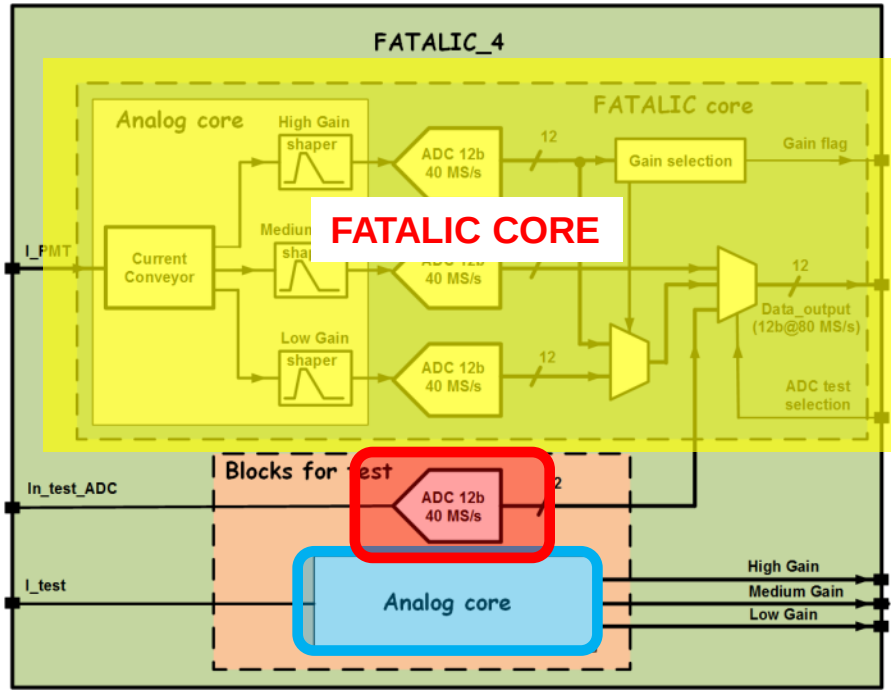
- A Digital block:
  - digital correction of the digital code (1.5bit/stage algorithm)
  - selection of the data to be outputted between high-gain and low-gain channels

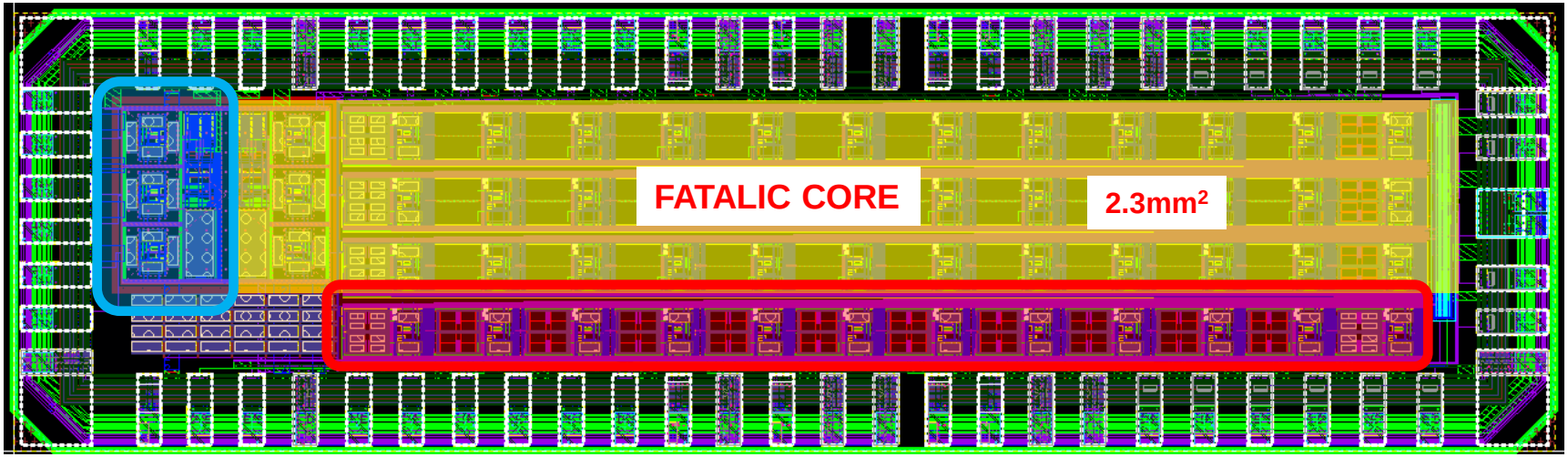


Pipeline ADC architecture



The floorplan





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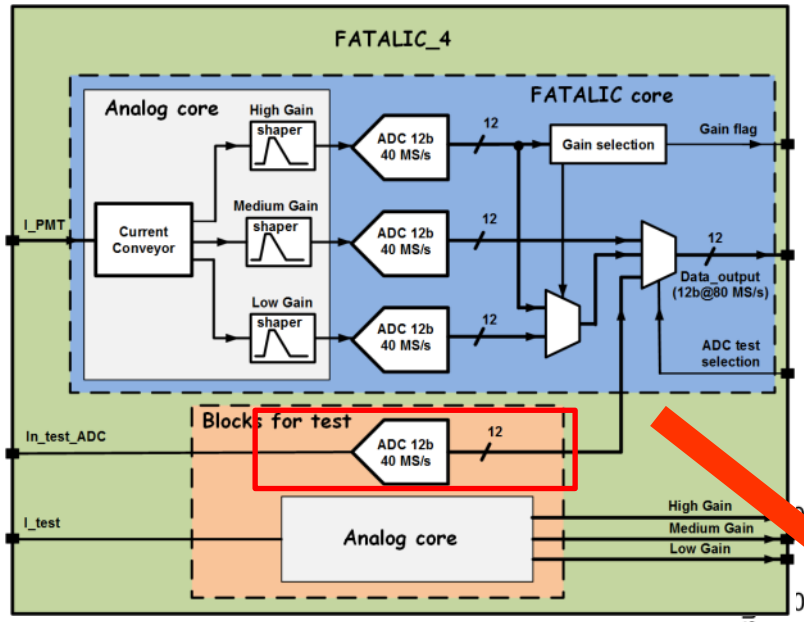
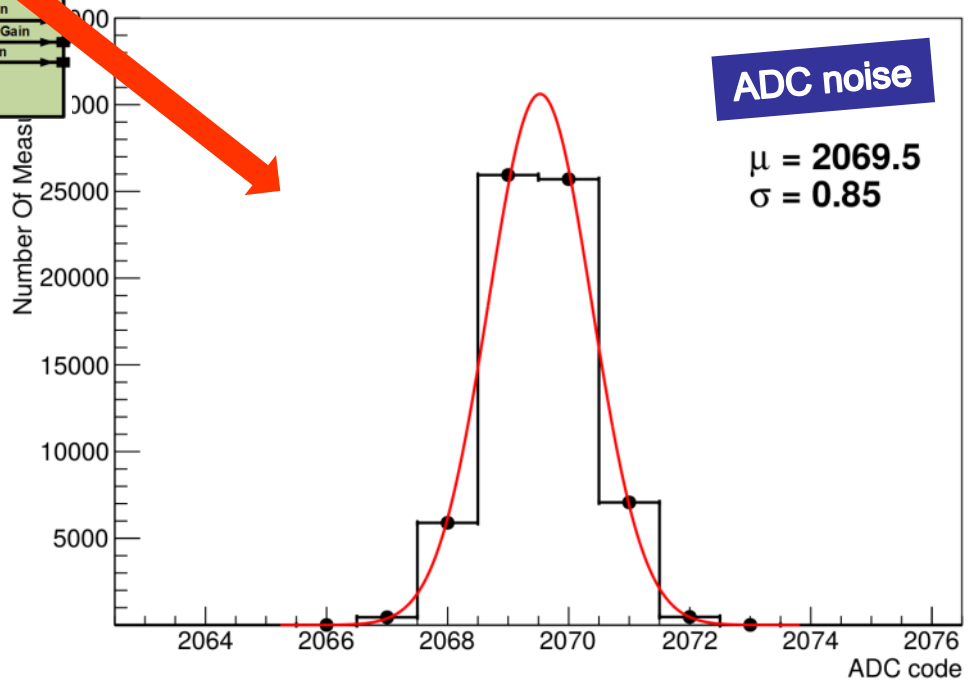
Performance: noise
Noise of the ADC



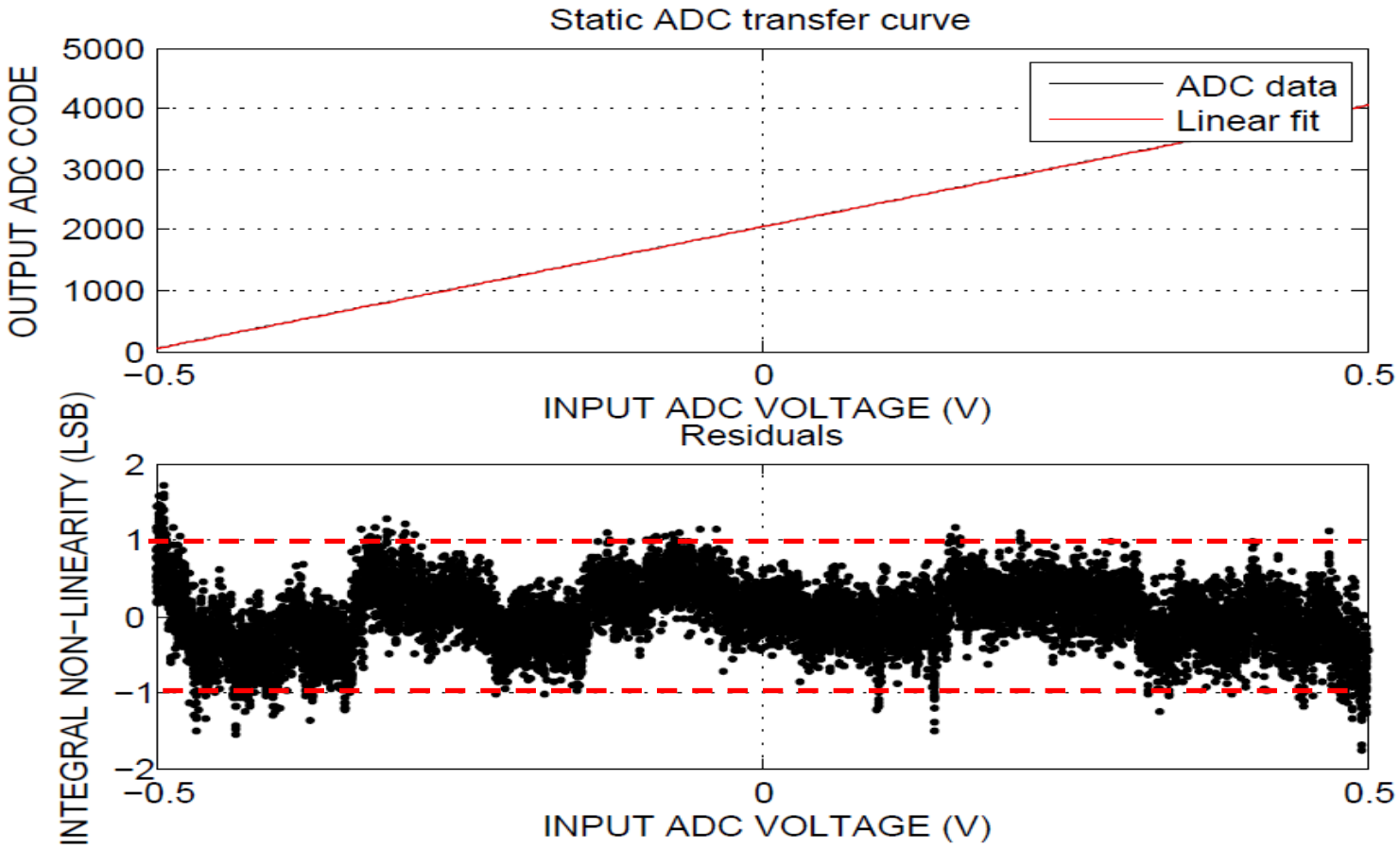
- Measurements on the extra-ADC; same environment as the 3 other ADC (clock, power supplies)
- Histograms of **output code** fluctuation (no input signal):
  - Mean Value = 2069.5
  - Std Deviation = 0.85 LSB



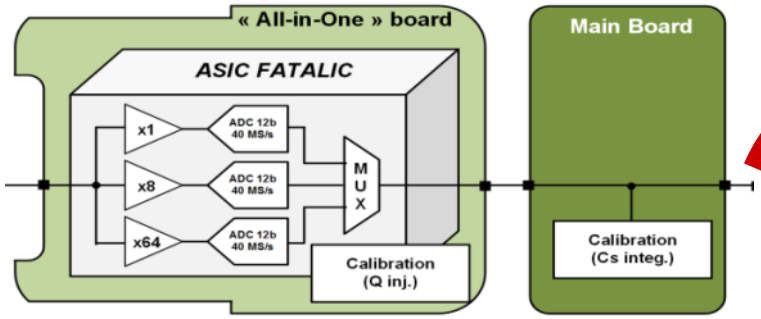
Performance: linearity

Integral Non-Linearity of the ADC

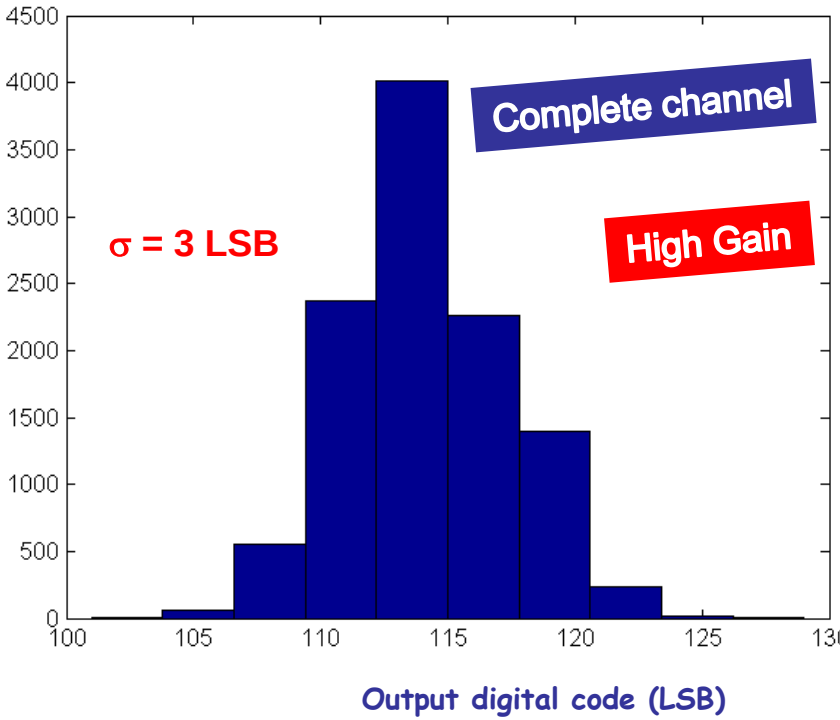
- Integral Non-Linearity (measurement with ramping generator):
  - INL= ± 1 LSB → 11-bit precision ADC → 10-bit required



Performance: noise
Complete channel



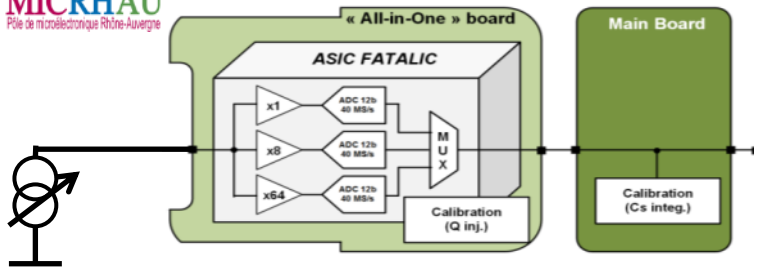
Noise Requirement: "The intrinsic noise of the electronics, as measured through the digitization path, expressed in terms of equivalent input charge, shall not be greater than **12 fC rms** at pedestal. "

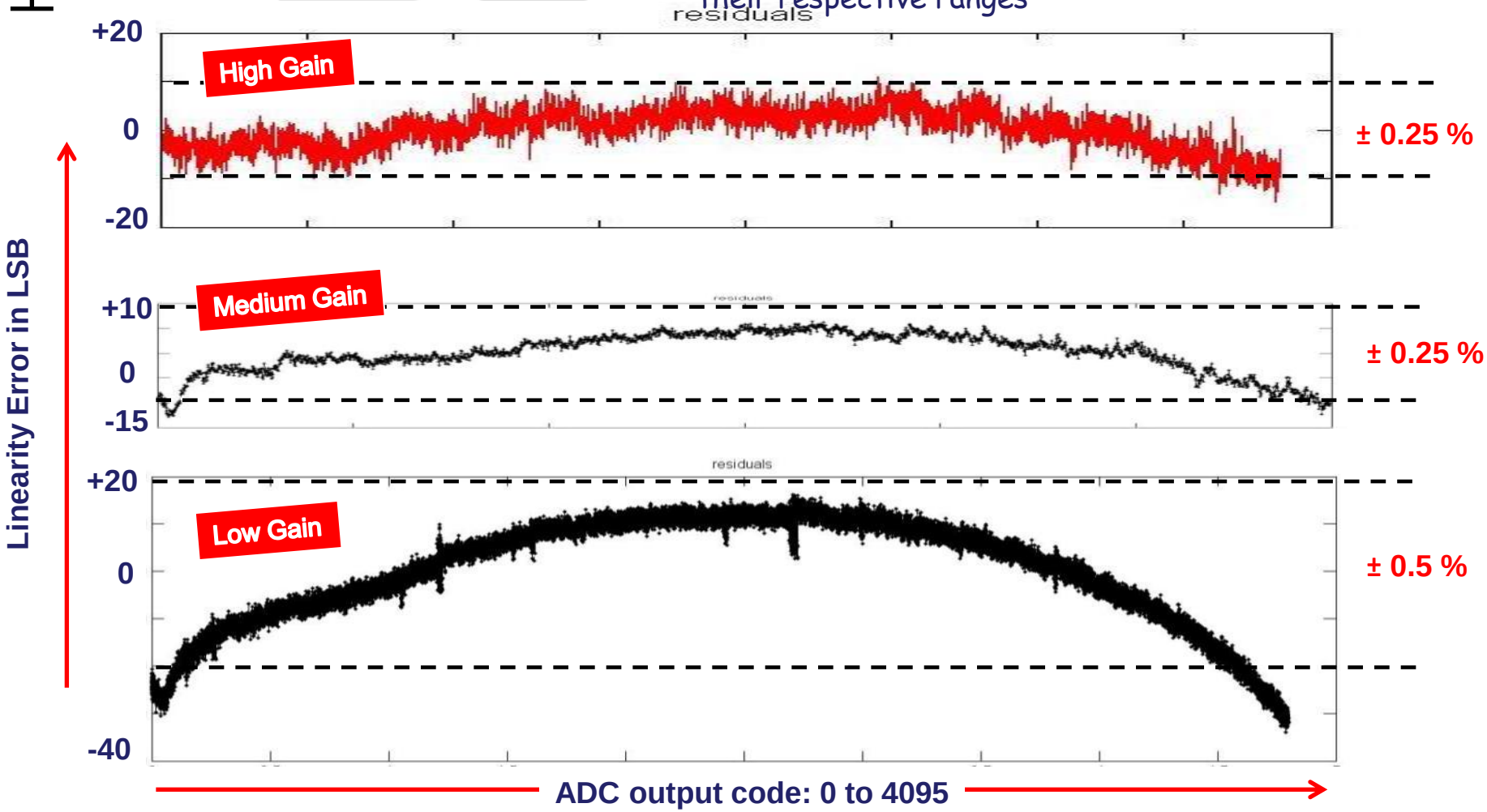


- Measurements on the high sensitive channel (High gain)
- Histograms of **output code** fluctuation (no input signal):
  - **Std Deviation = 3 LSB → σ= 10 fC rms**
- Thanks to the early digitization, noise performance guaranteed at the MB output

Performance: linearity of complete channel

- Test with slow (static) ramping current signal
- Readout of the 3 gain-channels (digital data) over their respective ranges



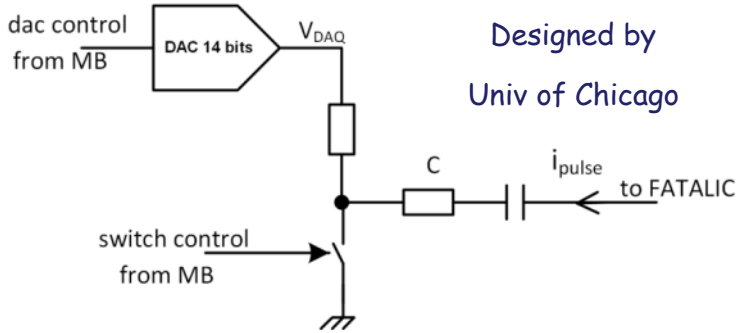


Performance: dynamic range

- Test with the **charge injection system**

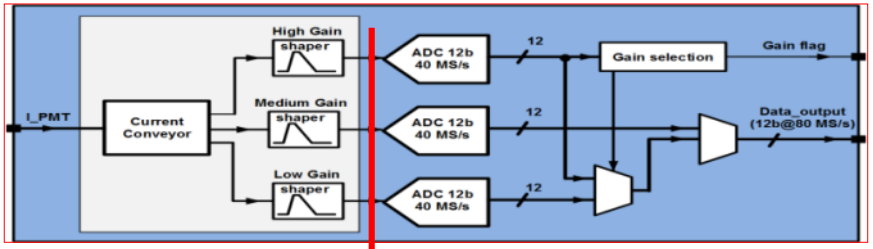
  → PMT-like pulses

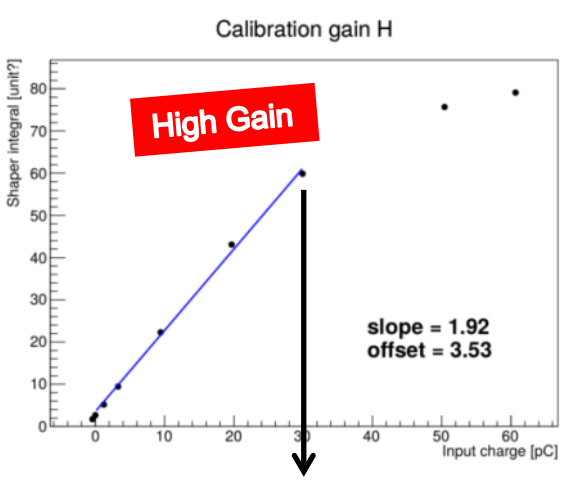
- Integral of the signals at the **shaper outputs**
- **Preliminary results:** few points and no precise calibration of the injector, but:
  - ➔ working quite well in each validity range
  - ➔ dynamic range limited to **800pC** (1200pC expected)
- Gain ratio: **H/M = 8.3 , M/L = 7.6 → OK with simulations**



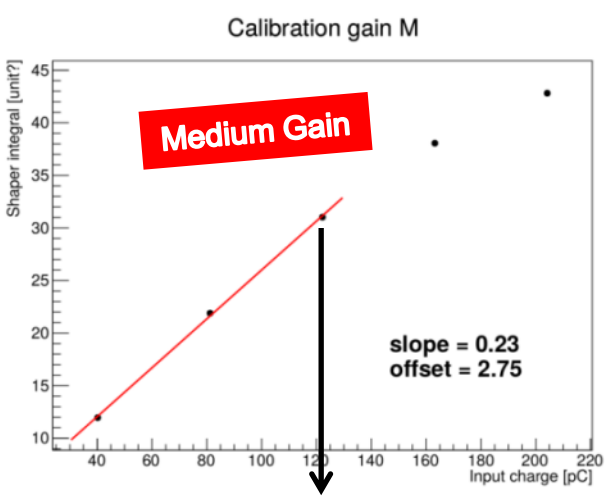
Designed by

Univ of Chicago

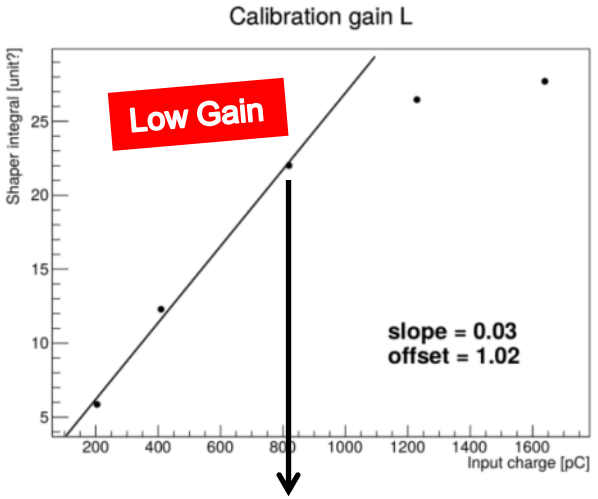




30pC



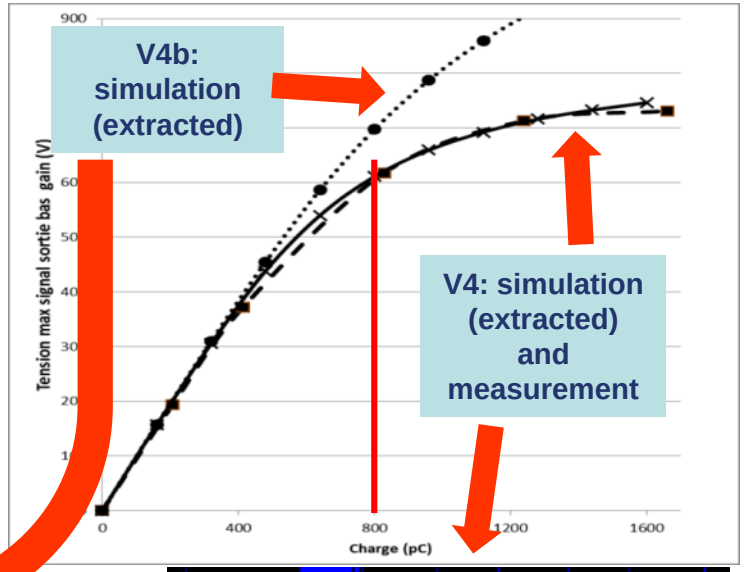
120pC

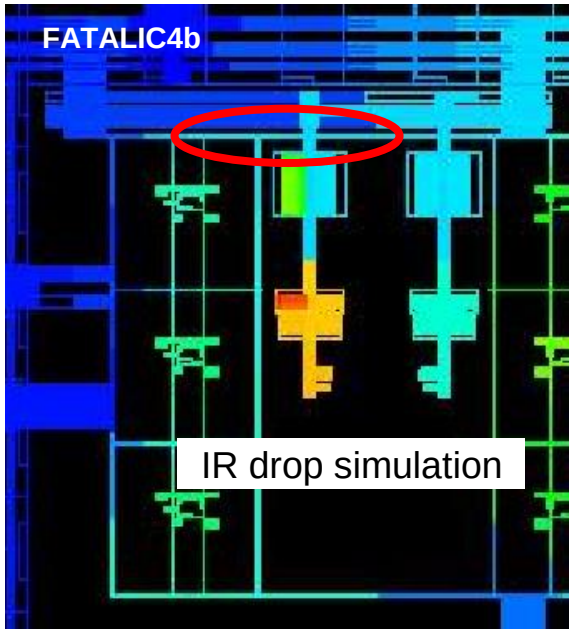


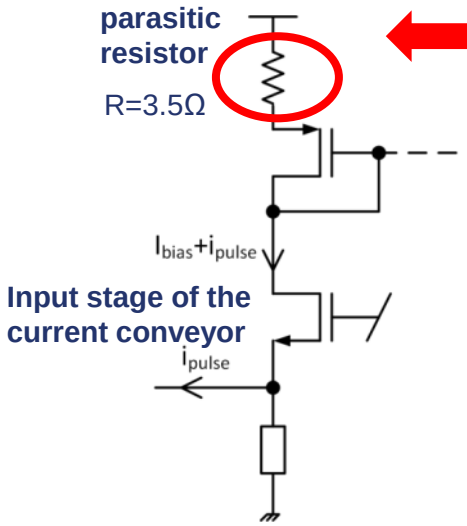
800pC

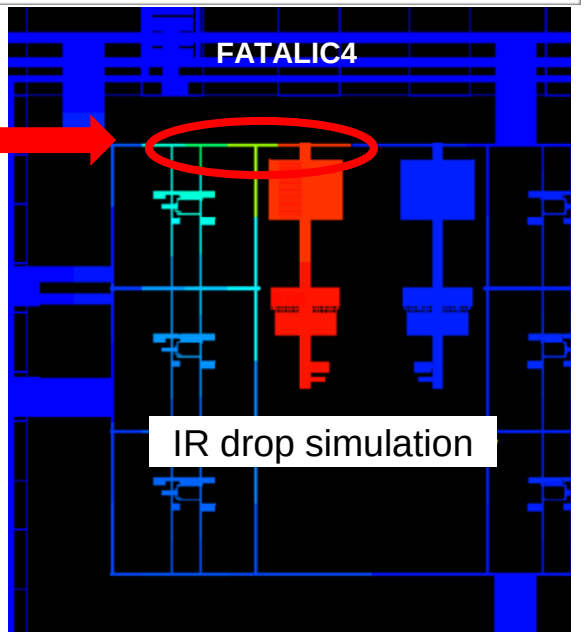
FATALIC: improvements (v4b)

- With PMT-like pulses, FATALIC-v4 exhibits a compression of its response over ≈ 800pC.
  - current conveyor: 3.5Ω parasitic resistor on a power rail
  - up to **200mV** voltage drop for high peak input current (tens of mA) (measurements fit with parasitic simulations).
  - → corrected in FATALIC-v4b
- New feature in V4b:
  - extra pin (input) to force the **low-gain** data as output information
- Chip delivered last week, tests in progress …









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Summary and Outlooks

- The FATALIC ASIC is **one** of the **three** options dedicated to the upgrade of the **VFE electronics** of the ATLAS-TileCal.
- It performs the **full processing** of the PMT signal, including the **analog-to-digital conversion**.
- FATALIC fulfills the **requirements** in terms of **noise**, and the embedded digitization guarantees an optimal signal-to-noise ratio all along the readout chain.
- The linearity is validated up to a **dynamic range of 800 pC**. It is extended to **1200 pC** with FATALIC-v4b (to be measured).
- More exhaustive measurements in **physic conditions** (PMT-like pulses) will be carried out thanks to:
  - the **charge injector** system embedded in the "All-in-One" board
  - a dedicated **LED+PMT** system
- Performance of FATALIC, as the two other options, will be evaluated on a demonstrator during test beams in 2015-2016 (1st period next week).

THANK YOU !