A 12bits 40MSPS SAR ADC with a redundancy algorithm and digital calibration for the ATLAS LAr calorimeter readout

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Summary

✓This SAR ADC is developed in the context of the ATLAS experiment's Liquid Argon Calorimeter (LAr) readout upgrade for Phase-II of the LHC.
✓With a resolution of **12 bits, it reaches 40MS/s with a power** consumption of only **11mW** in **CMOS 130nm 1P8M** process.
✓A generalized algorithm is used with a **redundancy** in **14 steps**, allowing a **digital correction** of the mismatch effects in the capacitor array.
✓The architecture of the capacitor array is differential within one segment but a reduced size of **only 2^{11} unit capacitors** is used.

The redundancy

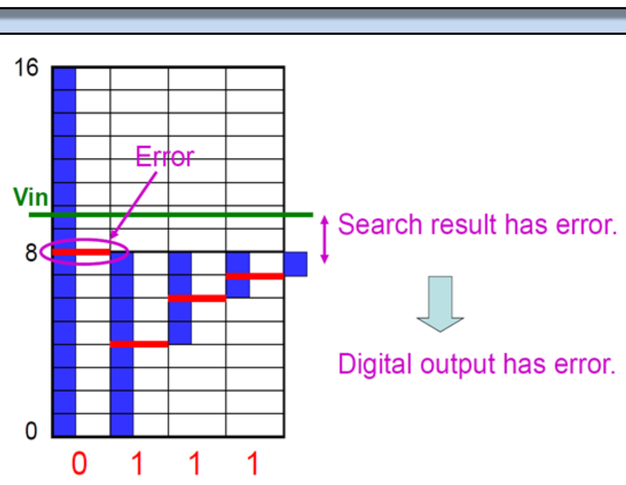


Fig 1: Example of decision error due to incomplete DAC settling.

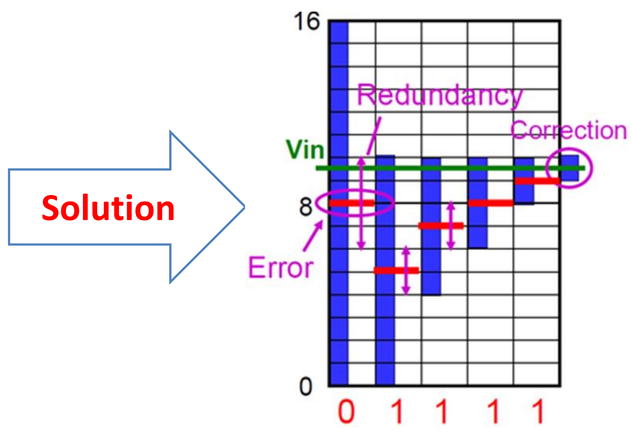


Fig 2: Operation of a redundant search algorithm of a 4-bit 5-step SAR ADC.

	Generalized non-binary search algorithm	
Step k	p(k)	q(k)
1	2048	24
2	1012	124
3	456	76
4	252	40
5	144	24
6	80	12
7	46	6
8	26	4
9	14	2
10	8	2
11	4	2
12	2	0
13	2	0
14	1	0

Table 1. A 12-BIT 14-STEP SAR ADC P(K) AND Q(K) VALUES

✓ Redundancy ➔ Robust toward incomplete DAC settling time issues.
➔ Possibility to calibrate the capacitors mismatch.
✓ During each conversion step (*k*), and to set the corresponding bit, the analog input voltage is compared to a reference voltage generated according to a redundancy vector ***p***.
✓ The vector ***q*** represents the settling error range which can be corrected by the redundancy in each step.

The architecture of the developed SAR ADC

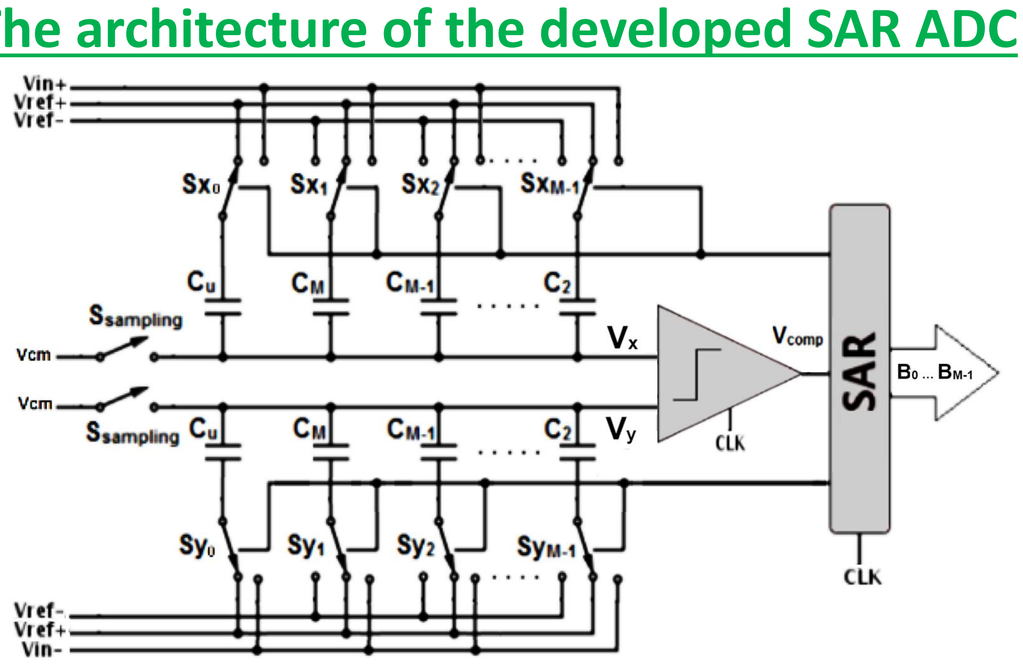


Fig 3: The proposed N-bit M-step SAR ADC architecture (where $C_k=p(k)*C_u$ and $k = 2, 3 \ldots M$).

✓ The redundancy algorithm **(14 steps)** is implemented in the analog part of the SAR ADC **(12bits, 40MS/s)**.

✓ The capacitive DAC is composed of only **2^{11} unit capacitors**

➔ Reduced dynamic power consumption.

➔ Total capacitors area divided by 2.

✓ The capacitors switching algorithm is :

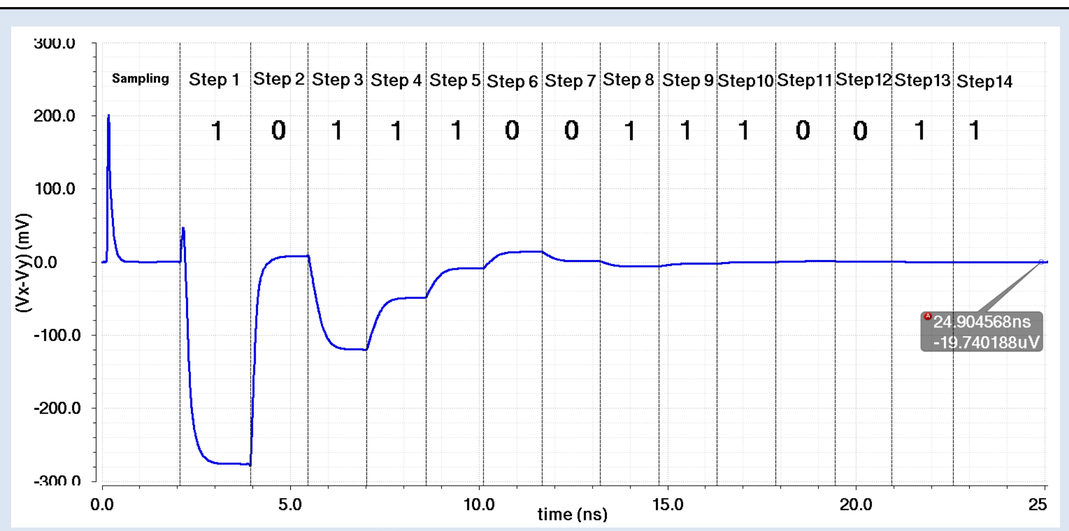
❑ Monotonous

➔ Saving extra dynamic power consumption.

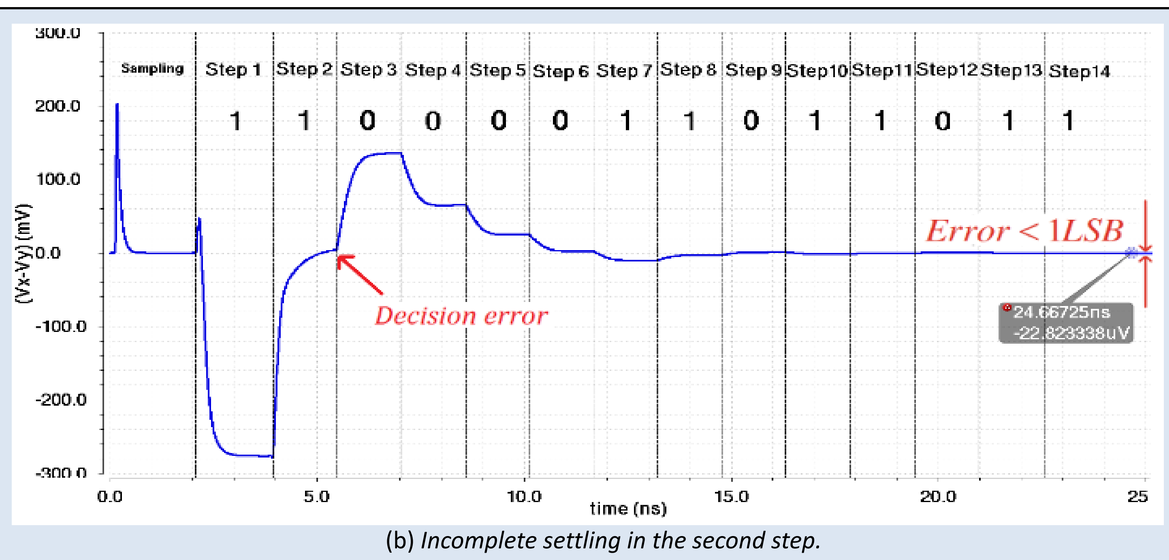
❑ Only one capacitor switched per conversion step

➔ Inherent immunity to the skew of the switch signals.

Simulation results



(a) Complete settling



(b) *Incomplete settling in the second step.*

Fig 4: Simulations of the DAC outputs voltage difference (***Vx-Vy***) of the proposed redundant architecture.

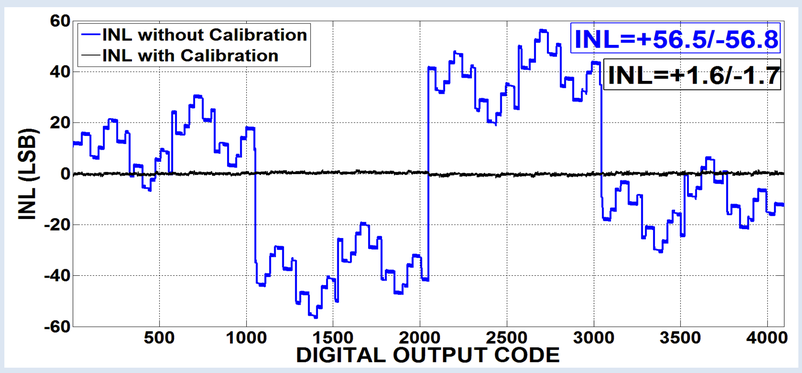


Fig 5: The simulated **INL** without and with digital calibration.

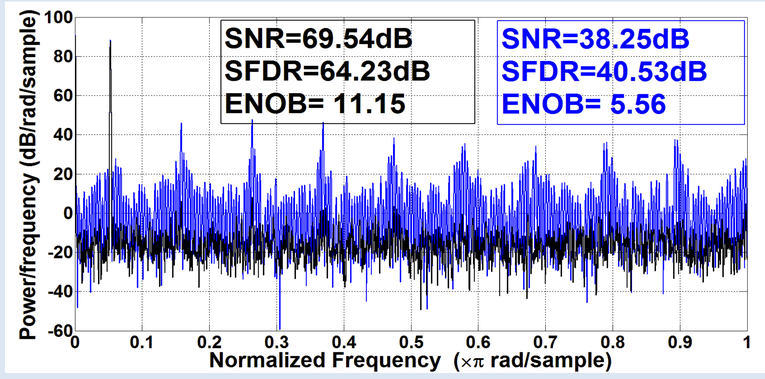


Fig 6: The simulated FFT **spectrum** without and with digital calibration.

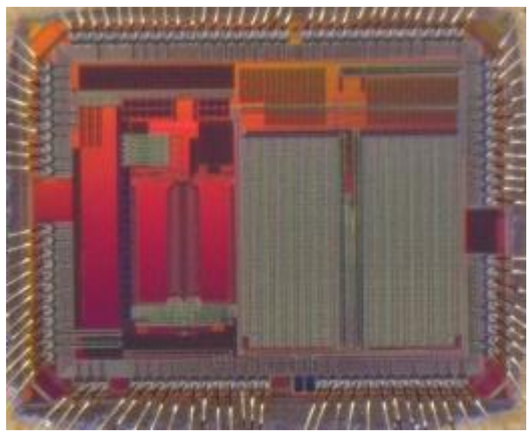


Fig 7: Chip die photograph to be tested