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Capacitively coupled hybrid pixel assemblies for the CLIC vertex detector

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Abstract

The vertex detector at the proposed CLIC multi-TeV linear e^+e^- collider must have minimal material content and high spatial resolution, combined with accurate time-stamping to cope with the expected high rate of beam-induced backgrounds. One of the options being considered is the use of active sensors implemented in a commercial high-voltage CMOS process, capacitively coupled to hybrid pixel ASICs. A prototype of such an assembly, using two custom designed chips (CCPDv3 as active sensor glued to a CLICpix readout chip), has been characterised both in the lab and in beam tests at the CERN SPS using 120 GeV/c positively charged hadrons. Results of these characterisation studies are presented both for single and dual amplification stages in the active sensor. Pixel cross-coupling results are also presented, showing the sensitivity to placement precision and planarity of the glue layer.

This work was carried out in the framework of the CLICdp collaboration

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1 Introduction

The demands for precision physics in combination with the challenging experimental conditions at the proposed electron-positron Compact Linear Collider (CLIC) have inspired a broad detector R&D program [1]. In particular the vertex-detector systems have to fulfil unprecedented requirements in terms of material budget (0.2% of a radiation length, X_0 , per layer) and spatial resolution (3 μm single-point resolution) in a location close to the interaction point, where the rates of beam-induced background particles are high. Time slicing of hits with an accuracy of approximately 10 ns will be required to separate such backgrounds from physics events.

The R&D aims at achieving the single-point resolution target with pixels of size $25 \times 25 \mu\text{m}^2$ and analogue readout. Hybrid readout solutions are currently under study, comprised of high-performance readout Application Specific Integrated Circuits (ASICs) coupled to ultra-thin sensors with fast signal collection through drift in the depleted bulk volume. The target thickness for ASICs and sensors is 50 μm each.

Conventional small-pitch solder bump bonding between the readout ASICs and the sensors is costly and reduces the achievable yield for large-area detector systems. Moreover, planar high-resistivity passive sensors require the use of complex and costly custom manufacturing processes. The use of Capacitively Coupled Pixel Detectors (CCPD) has recently been proposed as an alternative [2]. In this approach active sensors with an amplification stage in each pixel are implemented in a commercial High-Voltage Complementary Metal-Oxide-Semiconductor process (HV-CMOS). The sensor substrate is biased, leading to a depletion layer of a few microns. The fast drift signal collected in this depleted layer is transformed to a voltage signal by a transimpedance amplifier and sent to a metal readout pad. This voltage signal is then capacitively coupled through a thin (few microns) layer of glue to the corresponding input pixel pad of the readout ASIC.

In the following we present first laboratory and test-beam measurement results for prototypes of an active HV-CMOS sensor (CCPDv3) capacitively coupled to a readout ASIC (CLICpix).

2 Setup

2.1 The CCPDv3 HV-CMOS sensor

The CCPDv3 is an ASIC implemented in a 180 nm high-voltage CMOS process, designed specifically for use as an active sensor. The chip contains no standalone readout circuitry, save for a single line through which the analogue output of individual pixels may be probed. Each $25 \times 25 \mu\text{m}^2$ pixel contains only analogue circuitry, placed in a deep n-well which acts as the collection electrode (on the p-type substrate) in addition to providing shielding for the electronics and allowing the application of a substrate bias of up to 60 V. This allows the creation of a depletion region around the deep n-well, providing fast carrier collection and increased signal size compared to that available solely through diffusion. Nonetheless, due to the low resistivity of the substrate (10 - 20 Ωcm) the active depth is not expected to exceed 30 μm . The deposited charge is amplified by an integrating amplifier, with an optional second stage voltage amplifier, and the resulting voltage is directed towards an output pad. This pad is then connected to the readout chip by capacitive coupling.

Simplified schematics of the pixel designs for the CCPDv3 and CLICpix (described below) are shown in figure 1. The CCPDv3 pixel contains two amplification stages, and is the default design implemented through most of the chip. A four-column region however contains pixels with a slightly modified architecture, removing this second stage. The resulting voltage pulse is of opposite polarity, and is reduced in magnitude by a factor of approximately 2. This reduction in amplification should result in lower power consumption, of considerable interest for CLIC. The leakage current of the chip versus applied bias voltage is shown in figure 2, where the current is observed to be satisfactory (at the level of tens of nA) until 93 V, well in excess of the maximum rating (60 V).

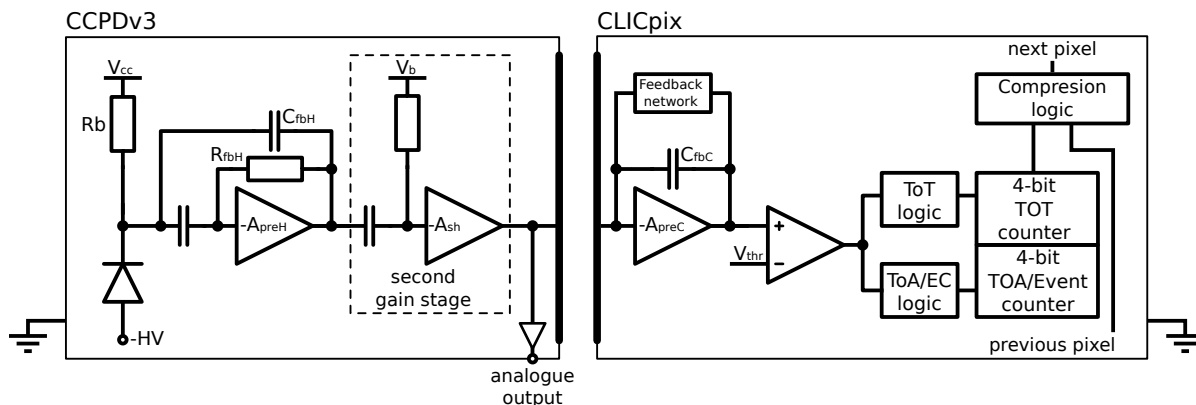


Figure 1: Schematic of the CCPDv3 and CLICpix pixels, with two-stage amplification shown on the CCPDv3.

2.2 The CLICpix readout ASIC

The CLICpix demonstrator hybrid readout chip [3] is a small prototype ASIC targeted to the requirements of the CLIC vertex detector. The chip is implemented in a 65 nm CMOS process. It contains a matrix of 64×64 pixels with $25 \mu\text{m}$ pitch, containing both analogue and digital functionality. Each pixel contains two 4-bit counters, with configurable modes, which operate simultaneously. A Time over Threshold (ToT) measurement of the injected charge amplitude has been implemented, incrementing the counter for each clock cycle during which the discriminator output remains high. A counting mode has also been implemented, incrementing the counter each time the discriminator exceeds the set threshold. Finally, time-stamping of the event is possible by measuring the time between the discriminator crossing threshold and the shutter (described below), to give the particle Time of Arrival (ToA).

The readout architecture of the CLICpix is designed to match the expected beam structure at the CLIC accelerator, involving bunch-train periods of 156 ns with intense activity followed by gaps of 20 ns used for the readout. This is most suited to a shutter-based operation of the chip, whereby all pixels are continuously sensitive while the shutter is open, after which the full matrix is read out. Zero suppression is performed on the ASIC level, and the full chip can be read out in less than $800 \mu\text{s}$ (for 10% occupancy), using a 320 MHz readout clock. A custom readout system, built on a SPARTAN6 FPGA board and modular interface card [4], has been designed for this purpose. Initial testing (without sensor) has shown that the CLICpix is fully functional and that the performance is in agreement with simulations [5]. For

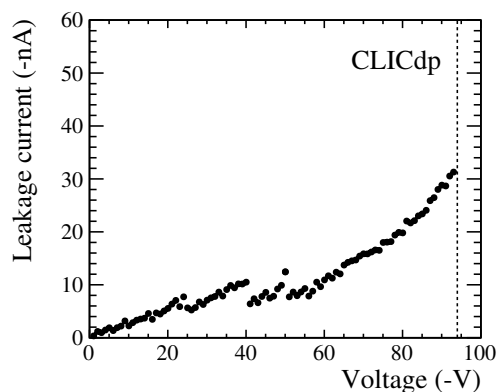


Figure 2: High voltage tolerance of the CCPDv3, showing the leakage current versus bias voltage for the full $1.6 \times 1.6 \text{ mm}^2$ matrix. The breakdown voltage is indicated by the dashed line.

all of the results shown, the ToT measurement of the input charge was performed using a clock frequency of 20 MHz and a constant discharge current.

2.3 Capacitively coupled assemblies

First assemblies of capacitively (or AC) coupled CLICpix ASICs with CCPDv3 active sensors have been produced and tested in October 2014. The output pads of the CCPDv3 are aligned with the CLICpix input pads and connected by a glue layer a few microns thick. This is achieved using a precision flip chip bonder, commonly used for bump bonding, with an epoxy resin [6] for the glue layer. The pad sizes of the CCPDv3 and CLICpix are roughly $20 \times 20 \mu\text{m}^2$ and $14 \times 14 \mu\text{m}^2$ respectively. A cross-section of such a device can be seen in figure 3, where the CLICpix is shown on the top of the figure and the CCPDv3 on the bottom. The high precision of the pad alignment can be seen clearly, in addition to the thin layer separating the pads (roughly $2 \mu\text{m}$), which consists of the polyimide passivation layers of the pads and a very thin layer of glue in between. Neither of the ASICs have been thinned, resulting in an approximate thickness of $280 \mu\text{m}$ for the CLICpix and of $250 \mu\text{m}$ for the CCPDv3.

2.4 Lab setup

Measurements were taken in the lab using ^{55}Fe and ^{90}Sr sources, of activity 6.9 MBq and 29.6 MBq respectively. Due to the penetrating depth of the incident radiation, the spectra were acquired using a bare CCPDv3 device, illuminated from the front (implant) side. Calibrations of the assemblies were carried out using the ^{90}Sr source impinging on the back side of the sensor, by observing the analogue output of a single HV-CMOS pixel on a fast sampling oscilloscope and using this signal as a trigger for the CLICpix readout. The on-pixel event counter is available for use as a veto, in order to avoid events where more than 1 hit occurs during the measurement window.

2.5 Testbeam setup

Testbeam experiments were carried out in November 2014 on the H6 beam line in the CERN SPS North Area, using a beam of positively charged hadrons with momentum 120 GeV/c. Typical mean particle rates of 500 kHz/cm^2 were observed during the 4.8 s spills, at intervals of 25 s. Tracking information was provided by the AIDA telescope [7], which provided a pointing precision at the device under test of $1.6 \mu\text{m}$. Due to the difference in physical size between the Device Under Test (DUT, $1.6 \times 1.6 \text{ mm}^2$) and the telescope active area ($10 \times 20 \text{ mm}^2$) and the difference in readout architecture, the CLICpix shutter was held open for several of the $230 \mu\text{s}$ telescope rolling-shutter readout periods. Each frame from the CLICpix was then copied and attached to the telescope data for all rolling shutters which occurred during

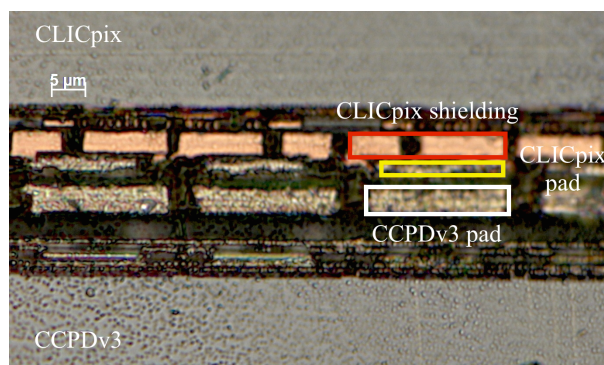


Figure 3: Cross section of a CLICpix (top) CCPDv3 (bottom) assembly, taken with an optical microscope.

the combined data taking. To further improve the efficiency of the data taking, a Region of Interest (RoI) was chosen on a FE-I4 [8] trigger plane, used in conjunction with three crossed scintillators at upstream and downstream of the telescope. The clock used for the ToT measurement on the CLICpix was set to 20 MHz, and the integration time of the CLICpix was short with respect to the CCPDv3 pulse.

3 Standalone measurements with the CCPDv3

Using the analogue output from single pixels, the response of the CCPDv3 device can be investigated. Source measurements have been carried out on a bare CCPDv3 device, in order to deposit charge on the implant side of the detector. The output pulse from a single event is shown in figure 4. The DC output of the amplifier is around 1.15 V and swings of up to ~ 700 mV are observed, beyond which there is saturation of the amplifier output. The pulse height spectra for ^{55}Fe and ^{90}Sr are shown in figure 5. The ^{55}Fe K_{α} peak (5.90 keV) is clearly visible, and can be used to obtain a rough calibration of the CCPDv3, with 1000 electrons deposited charge equivalent to 270 mV (for the peak position of 1600 electrons at 445 mV). The ^{90}Sr spectrum is harder to interpret, given the limitation of reading out only a single pixel per event and the fact that the raw distribution will be smeared by events where charge has been shared between several pixels. The effects of the amplifier saturation can be seen, with no events present above 750 mV.

Variations in the output amplitude between pixels have been observed using the 16 pixels with standalone readout capability, to the approximate order of 20%. Given the limited number of pixels which can be read out directly it is not possible to accurately quantify the variation in performance across the device using this method.

4 Measurements of capacitively coupled assemblies

4.1 Induced signal and feedback loop

Using the method described above, it is possible to calibrate the CLICpix CCPDv3 assemblies with a ^{90}Sr source by comparing the analogue output of the CCPDv3 with the ToT recorded by the CLICpix on an event-by-event basis. This was performed for assemblies in the lab, with the results of one device shown in figure 6. The calibration has been performed with a substrate bias of 60 V and for pixels with single- (plot a) and two-stage (plot b) amplification. The discriminator threshold of the CLICpix is different for these two cases - an observed increase in noise for operation in negative polarity led to the

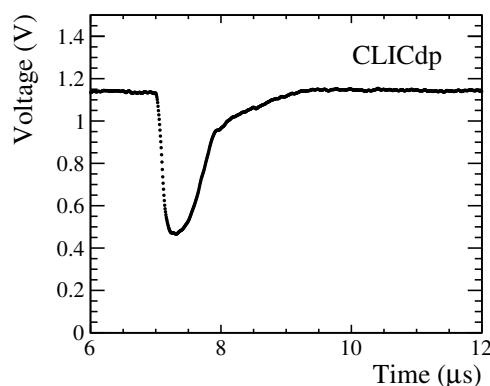


Figure 4: Example output pulse for the two-stage amplification pixels on the CPPDv3 with a substrate bias of 60 V.

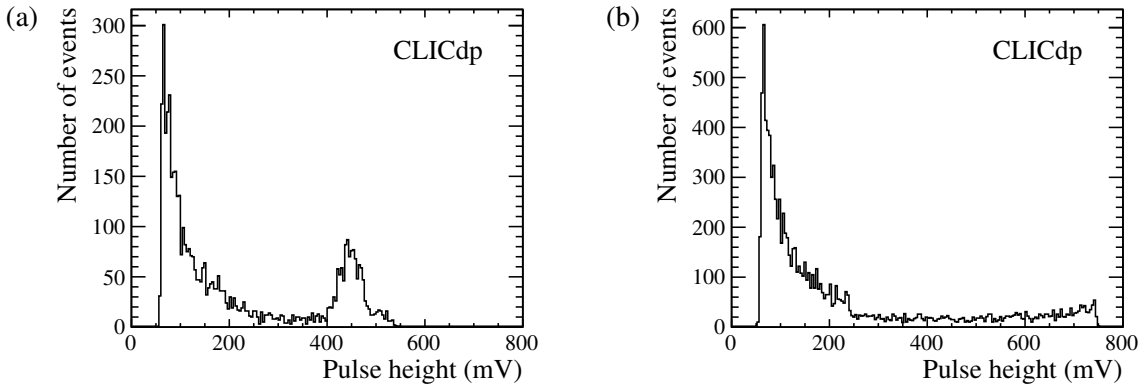


Figure 5: CCPDv3 pulse height spectra for (a) ^{55}Fe and (b) ^{90}Sr , using two-stage amplification pixels and with a substrate bias of 60 V.

use of a higher threshold than the design value. When operating in positive polarity the threshold applied was approximately half that for negative polarity.

Given the difference in threshold, the change in performance between the pixel types is striking. When operating with a nominal threshold of 1000 electrons and negative polarity, a pulse from the CCPDv3 of approximately 50 mV is sufficient to inject enough charge into the CLICpix that the pixel crosses the threshold. When operating in positive polarity, with an expected threshold half that of the negative polarity measurements, a pulse of more than 150 mV is required instead. The cause of this discrepancy has been found in the layout of the analogue part of the CLICpix pixel cell. A portion of the signal line which connects the discriminator output to the digital logic was found to lie underneath the analogue input pad of the CLICpix preamplifier. This has the effect of injecting a negative charge pulse into the preamplifier, creating a feedback loop which can either drive the pixel over threshold or reduce the height of the input charge (depending on the polarity of the charge signal). For all data taken in negative polarity, the charge injected by the discriminator output will therefore be added on to the signal from the CCPDv3, while for positive polarity data the injected charge will be subtracted from the signal. The CLICpix design additionally breaks down the pixel matrix into double column structures; the magnitude of this injected charge is therefore expected to vary between the two column types located therein.

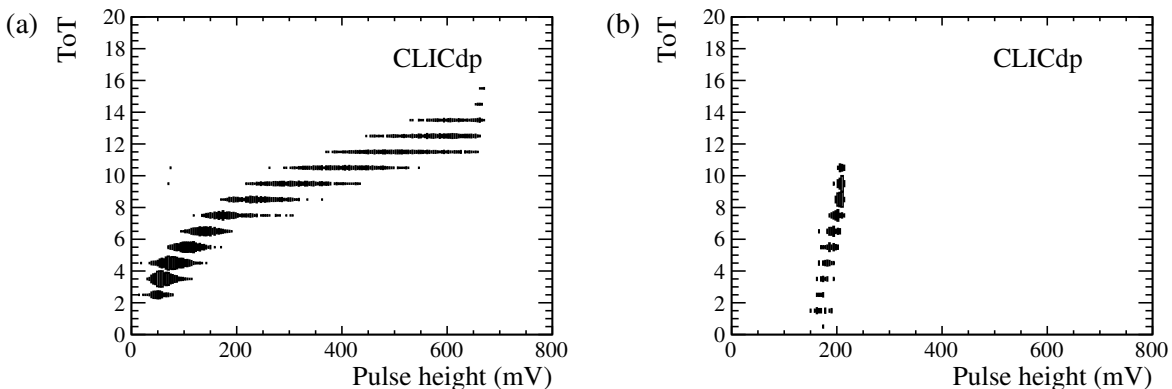


Figure 6: Calibration curves for CLICpix CCPDv3 assemblies taken with ^{90}Sr , showing the pulse height in the CCPDv3 versus the observed ToT in the CLICpix for (a) two- and (b) single-stage amplification pixels. The difference between the two cases is largely due to the injection of charge into the front end by the discriminator.

From the calibration curves in figure 6 an estimate of the injected charge can be made. Using the expected value of the threshold DAC from the design of the CLICpix ASIC (10 electrons per DAC step) it is possible to estimate the threshold for the cases above as 500 and 1000 electrons for positive and negative polarity operation respectively. Assuming that the mode of operation has no effect on the capacitance, C , between the CLICpix and CCPDv3 pads, and that the injected charge is the same regardless of the polarity, the value of the injected charge Q_{inj} can be estimated by noting the voltage swing V required to cross threshold. This gives two expressions: $50 \text{ mV} \times C + Q_{inj} = 1000$ electrons for the negative polarity case and $150 \text{ mV} \times C - Q_{inj} = 500$ electrons for positive polarity. Combining these gives a rough value of the injected charge as 625 electrons.

4.2 Pixel cross-coupling measurements

As the method of signal transfer between the sensor and readout ASICs proceeds via a capacitive injection, the issue of cross-talk in the form of coupling to neighbouring pixels must be considered. The CCPDv3 pixel design contains a guard ring surrounding each pixel which reduces the capacitance to neighbouring pixels. Cross-talk here is not expected to be a major issue, but other sources of unwanted capacitive coupling such as that between CLICpix input pads and neighbouring CCPDv3 pixels can be anticipated. These can be measured by observing the pixel response as a function of the track intercept position. This is shown in figure 7, plotted separately for the column and row directions. Tracks reconstructed in the telescope are extrapolated to the DUT, and the distance between the track intercept and nearby hit pixels is observed. A fit is performed based on a top-hat² contribution for the pixel hit and an additional top-hat from each neighbouring pixel, with the width and sigma of the error functions left floating and the offset in distributions fixed to the pixel pitch. This can be expressed as

$$\sum_{pixels} \frac{a}{2} \left[\text{erf} \left(\frac{x + x_{pixel} + \frac{\sigma}{2}}{\sigma\sqrt{2}} \right) - \text{erf} \left(\frac{x + x_{pixel} - \frac{\sigma}{2}}{\sigma\sqrt{2}} \right) \right] \quad (1)$$

where x is the distance between the track intercept and the pixel centre, x_{pixel} is the distance to neighbouring pixel centres, σ controls the width of the contribution and a is a constant related to the magnitude of the cross-coupling.

The left hand plot in figure 7 (along the column direction) shows an induced signal by the nearest and next-to-nearest pixels, notably in a symmetric fashion. The response along the row direction however (right hand plot) is distinctly asymmetric: this is assumed to be the result of the alignment procedure

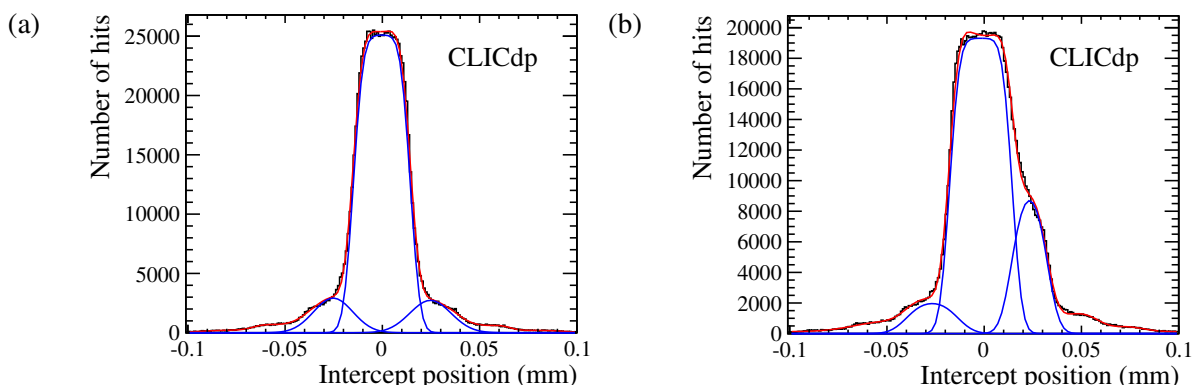


Figure 7: Pixel response as a function of track intercept, in the column (a) and row (b) direction. The substrate bias shown is 60 V, for two-stage amplification pixels.

²The combination of two error functions

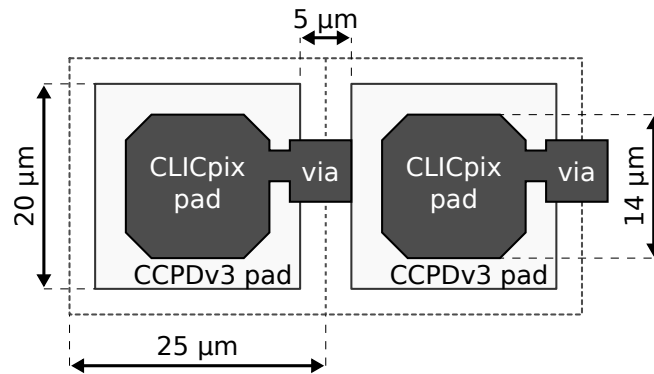


Figure 8: Layout of the CLICpix and CCPDv3 pads in the nominal glueing position, for two pixels in the same column.

during the gluing process, where the output pad of the CCPDv3 and the CLICpix were aligned with each other. As shown in figure 8, a *via* exists on the CLICpix in order to connect the input pad of each pixel (on the uppermost metal layer of the chip) with the circuitry located in lower metal layers. This *via* directly overlaps with a portion of the neighbouring CCPDv3 output pads in one direction, giving rise to the observed asymmetric coupling.

It is not possible from the data available to extract the coupling capacitance between the CLICpix *via* and the neighbouring CCPDv3 output pad. The pixel ToT distribution is shown as a function of track intercept in figure 9. The asymmetry can be clearly seen, though the ToT distribution is broadly the same on both sides. As the charge spectra are so similar between the two side pixels, one of which couples much more strongly, the charge observed for these events must still be dominated by the charge injected by the discriminator output. It is therefore expected that this effect will be significantly reduced for future versions of the CLICpix chip.

The value of the capacitance between the CCPDv3 output pad and the CLICpix input is controlled by the thickness of the glue layer between the devices. An important parameter for the device uniformity is therefore the planarity of the devices during the glueing process. This can be measured non-destructively by comparing the mean of the ToT spectrum as a function of the track intercept across the DUT, as shown in figure 10 (for single-pixel clusters). A gradient in the measured charge can be seen across the device diagonal. Given the local uniformity of the detector response, this would imply a non-uniform layer of glue between the CLICpix and CCPDv3.

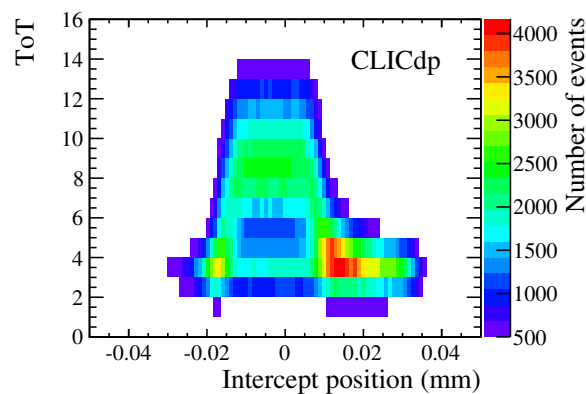


Figure 9: Pixel ToT distribution as a function of the track intercept in the row direction.

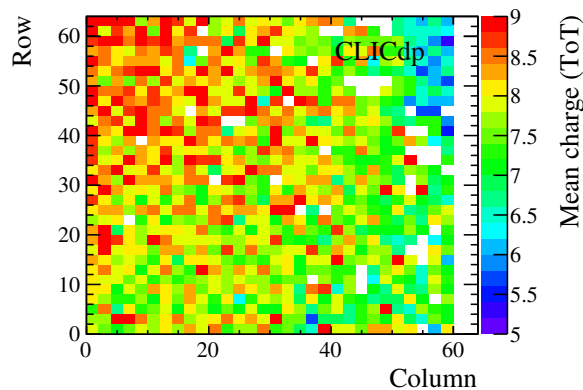


Figure 10: Mean ToT for single pixel clusters as a function of track intercept. The mean is extracted from a gaussian fit to the ToT distribution for each track intercept.

4.3 Tracking performance

Due to the charge injection issue, it is not possible to make a simple direct comparison between the performance of the single- and two-stage amplifier designs. The results are shown separately below for both pixel architectures, with the thresholds quoted in Digital-to-Analogue Converter (DAC) codes (threshold DAC denoted by THL). In all cases the centre of the noise distribution is found at $\text{THL} = 1220$ and each DAC code step should correspond (by design) to approximately 10 electrons. For positive polarity increasing the THL DAC corresponds to a higher threshold, while for negative polarity higher thresholds are found at lower THL values. Threshold dispersion over the pixel matrix is first corrected for using a 4-bit threshold adjustment in each pixel. Efficiency measurements were performed by extrapolating telescope tracks to the DUT and searching for clusters within a region of $75\ \mu\text{m}$ in the local x - and y -directions (corresponding to a distance of 3 pixels). A χ^2 cut was applied to the tracks in order to remove tracks with significant scattering. Noisy pixels on the DUT (defined as those responding more than 5σ above the mean rate) were removed from the analysis, as were tracks occurring within a half-pixel of any such pixels. The total number of masked pixels was in all cases below 3%. Tracks within $125\ \mu\text{m}$ of each other were also removed from the analysis, and the same conditions were used to compute the residuals of the device. For multi-pixel clusters, the cluster centre is defined as the ToT-weighted centre of gravity.

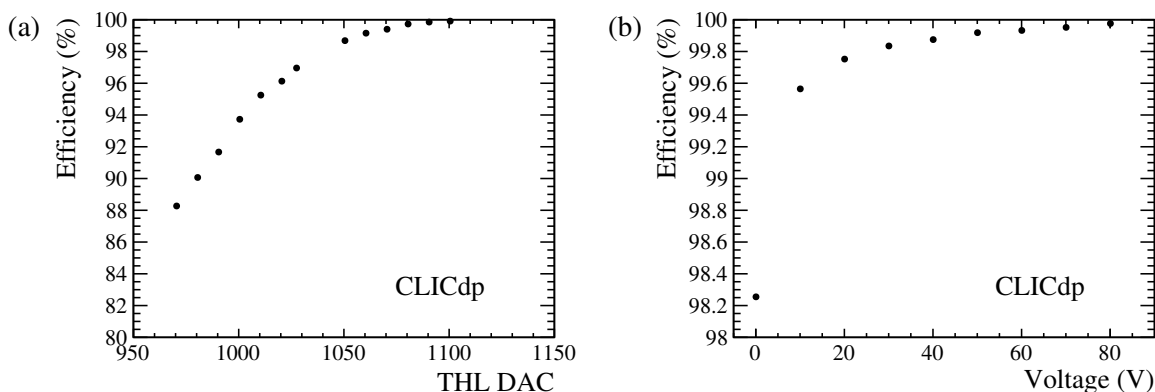


Figure 11: Single hit efficiency for two-stage amplification pixels (CLICpix in negative polarity) versus (a) threshold at 60 V, and (b) bias voltage at $\text{THL} = 1100$.

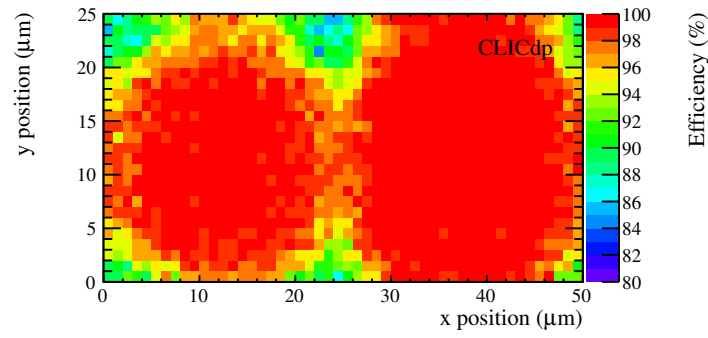


Figure 12: Efficiency map over the two-pixel unit cell, for two-stage amplification pixels and a substrate bias of 0 V.

4.3.1 Two-stage amplification

Single hit detection efficiencies for the assembly, operating in negative polarity (with two-stage amplification pixels), are shown in figure 11. Plot (a) shows the response versus threshold, taken with a substrate bias of 60 V. The assembly is observed to become fully efficient once the threshold reaches around 1200 electrons (THL = 1100).

The variation in efficiency with applied bias voltage, taken with low threshold (THL = 1100), is shown in plot (b) of figure 11. A slight (2 %) drop in efficiency is observed as the sensor is biased to low potential (0 V), though for all bias voltages above 10 V remains above 99 %. At all points a potential difference between the n-well and the p-type substrate of 1.8 V exists in addition to the externally supplied bias voltage.

For the data taken with 0 V, where a measurable drop in efficiency occurs, it is possible to map the

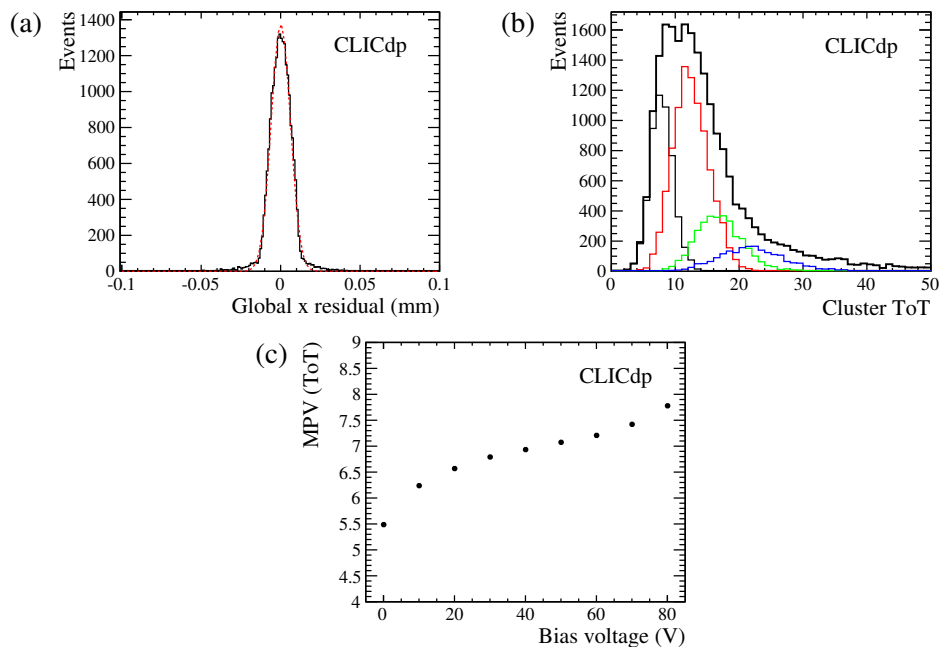


Figure 13: Single hit resolution (a) and ToT distribution (b) at 80 V and low threshold (THL = 1100). Cluster charge is shown separately for all associated clusters (solid black), along with the contributions for 1- (black), 2- (red), 3- (blue) and 4- (green) pixel clusters. Most probable value of the ToT distribution for single-pixel clusters as a function of bias (c).

single hit efficiency over the pixel cell. Due to variations in the CLICpix design between odd and even columns, the magnitude of the injected charge due to the discriminator firing is different for each column type. The efficiency is therefore shown in figure 12 over a two-pixel unit cell, showing the resulting difference in the response. There is almost no drop in efficiency for odd numbered columns (right hand pixel in the plot) and a small drop in efficiency for even numbered columns (left hand) where charge is shared between neighbouring pixels.

The single hit resolution for the device at 80 V and low threshold (THL = 1100) is shown in figure 13, along with the ToT distribution for clusters associated to tracks. The offset in peak position between clusters of different sizes is due to the non-linear response of the amplifier and the addition of the charge injected by the discriminator firing in each pixel. Residuals are calculated in the local x (column) direction, and a Gaussian fit to the distribution gives a resolution of 6.1 μm after subtraction of the 1.6 μm telescope pointing resolution. The spatial resolution appears to be insensitive to the applied bias voltage. The charge collected versus bias voltage is also shown in plot (c) of figure 13. The most probable value of the charge distribution was taken as the mean of a Gaussian fit to the single-pixel ToT distribution, with the same trend observed in clusters of all sizes.

4.3.2 Single-stage amplification

While the injection of a negative voltage pulse has a beneficial effect on the operation of the assembly in negative polarity (where the CCPDv3 additionally contains two amplification stages), data taken in positive polarity will be significantly degraded.

The efficiency of the single-stage pixel design is shown in figure 14 as a function of threshold (with 60 V applied bias) and bias voltage (with operating threshold THL = 1340, corresponding to the same nominal threshold as shown above for negative polarity operation). The impact of both the charge injection and reduced amplification on the CCPDv3 are clearly visible, with a maximum efficiency of just over 80 %.

5 Summary

First results for a prototype capacitively coupled pixel detector for the CLIC vertex detector have been presented. The performance of an HV-CMOS chip with two-stage amplification, coupled to the CLICpix readout ASIC, has been measured, and is observed to be fully efficient at a substrate bias of 80 V and

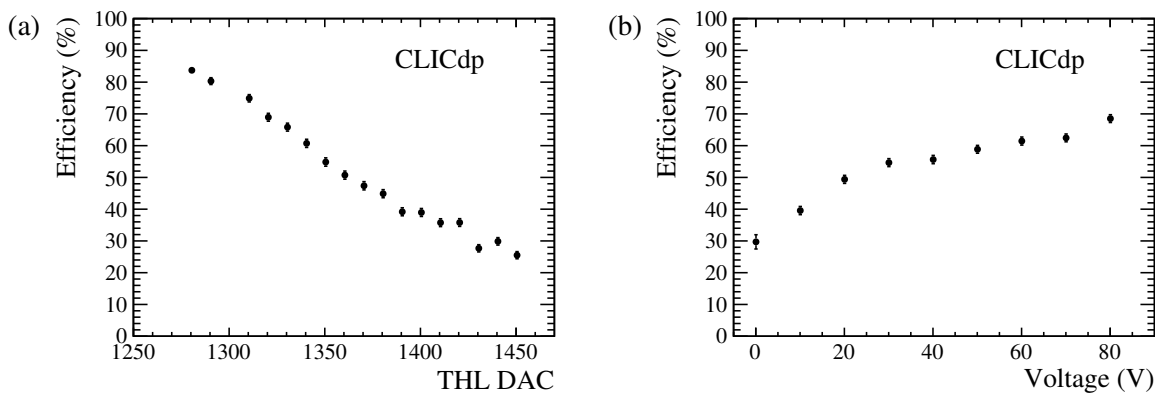


Figure 14: Single hit efficiency for single-stage amplification pixels (CLICpix in positive polarity) versus (a) threshold at 60 V, and (b) bias voltage with THL = 1340.

threshold of 1200 electrons. A single hit resolution of 5.5 μm has been measured at perpendicular track incidence. Cross-coupling between neighbouring CCPDv3 and CLICpix pixels has been observed, with an asymmetry in one direction that can be explained by the layout of metal layers in the CLICpix and the glueing geometry. Variations in the coupling capacitance across the pixel matrix have also been observed, ascribed to the non-planarity of the devices during glueing.

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