Tile Calorimeter Upgrade Program for the Luminosity Increasing at the LHC

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on behalf of the ATLAS Tile Calorimeter System

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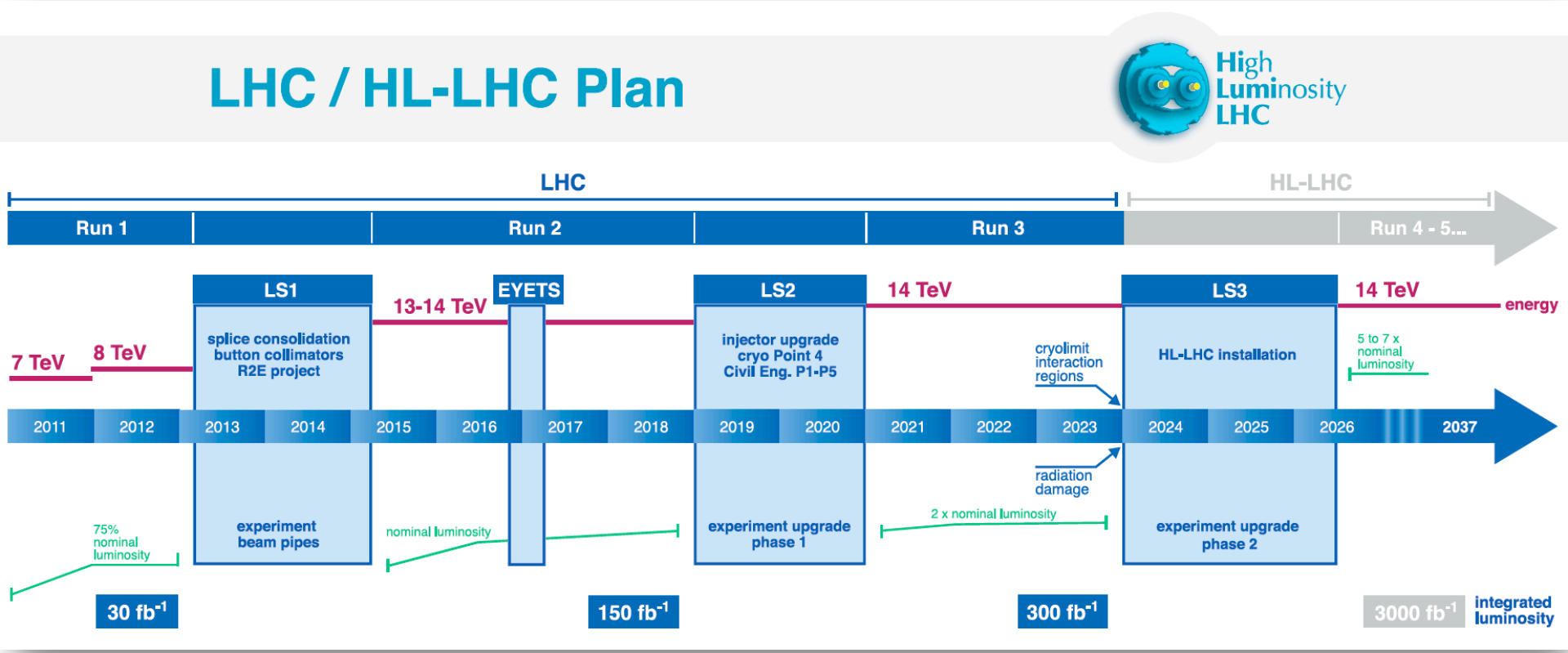
- TileCal
- ATLAS and TileCal Upgrade Program
- TileMuon Project
- Electronics Upgrade
- Summary

Introduction

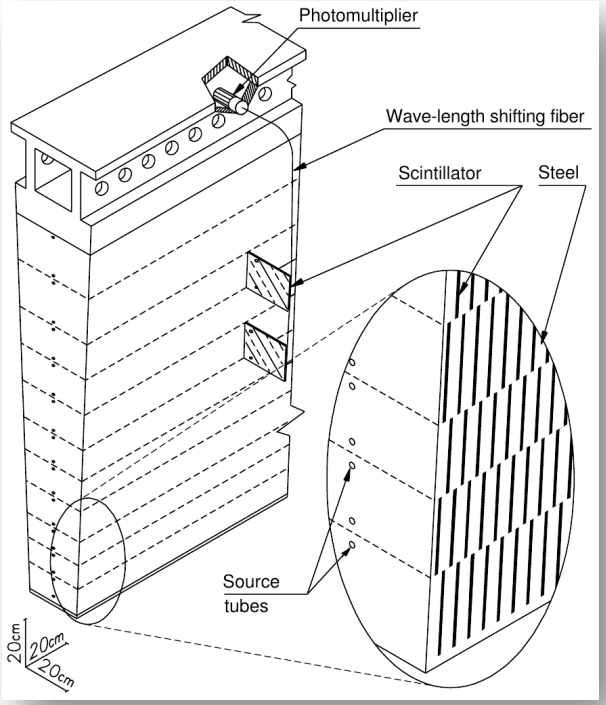
- The LHC is scheduled to undergo a major upgrade, in 2023, for the HL-LHC. The LHC luminosity will be increased by a factor of 10
- The ATLAS experiment is currently undergoing an ambitious 10 years upgrade to cope with the LHC luminosity increase
- Therefore, the Tile Calorimeter (TileCal), the central hadronic calorimeter of the ATLAS experiment, is currently in a very challenging R&D period

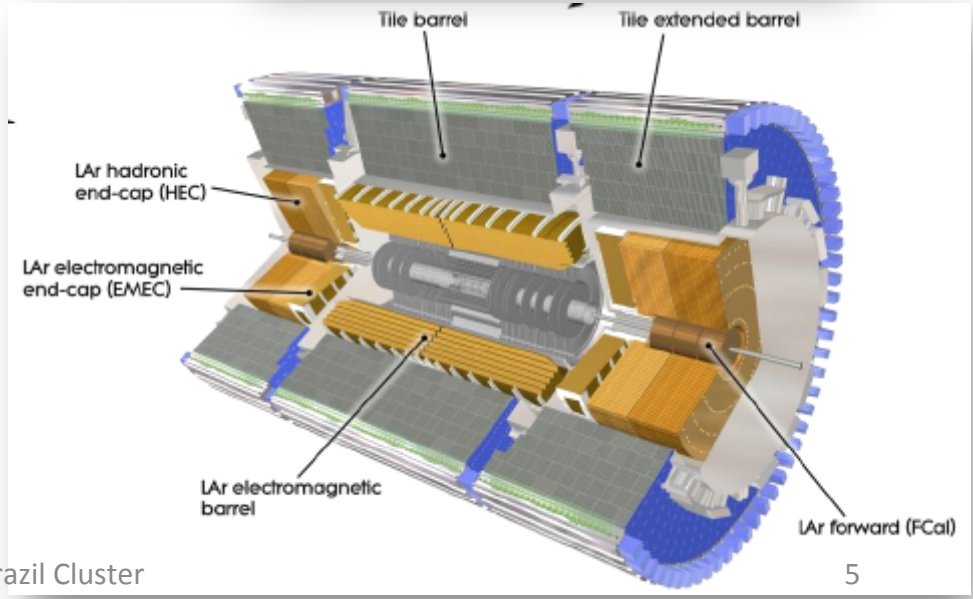
LHC luminosity increasing



Tile Calorimeter

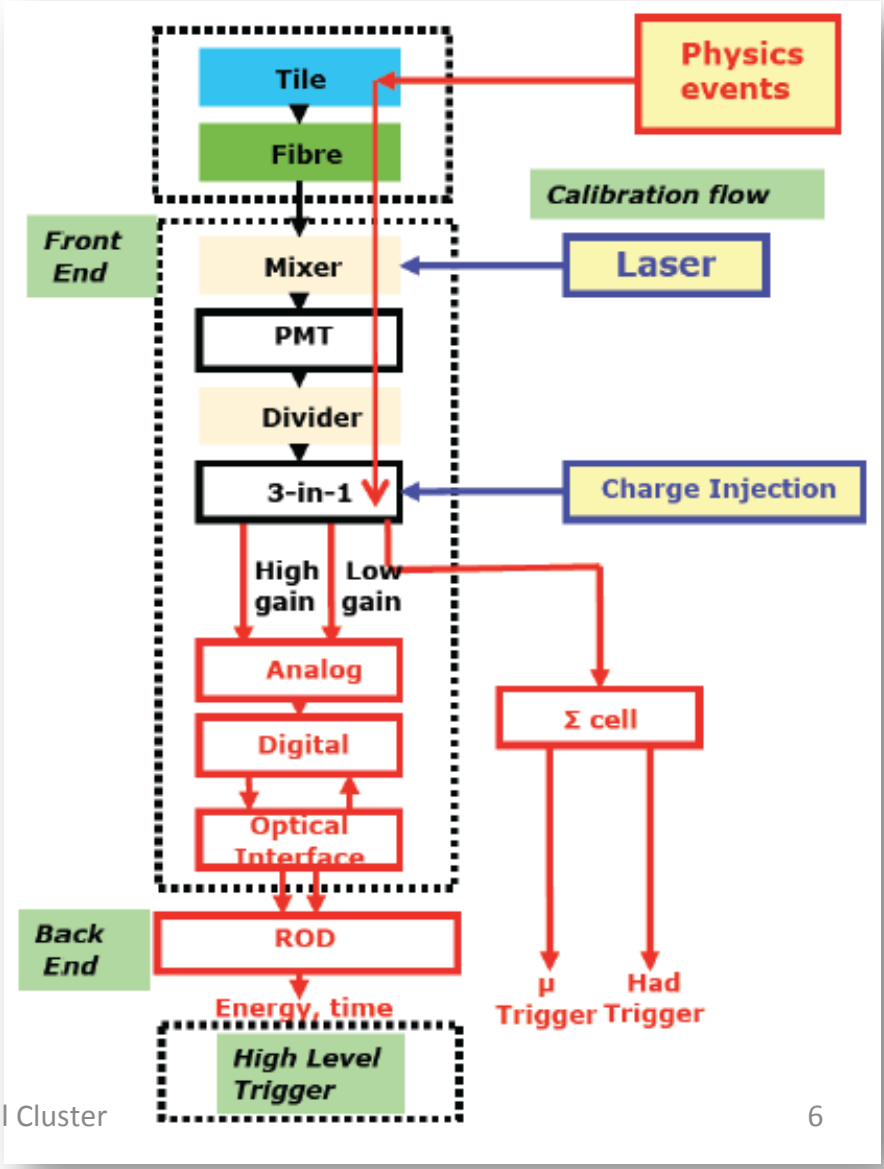
- ATLAS hadronic calorimeter
- Sampling calorimeter with steel plates as absorber material and plastic scintillating plates (tiles) to sample the energy
- Optical fibers to transmit the light to PMT cells located inside the girder (electronics drawer)
- Cylindrical structure divided in 1 central barrel and 2 extended barrels formed by 64 modules each
- Approximately 10,000 readout channels
- Operating successfully in ATLAS since the start of the LHC collisions (data quality efficiency above 99%)



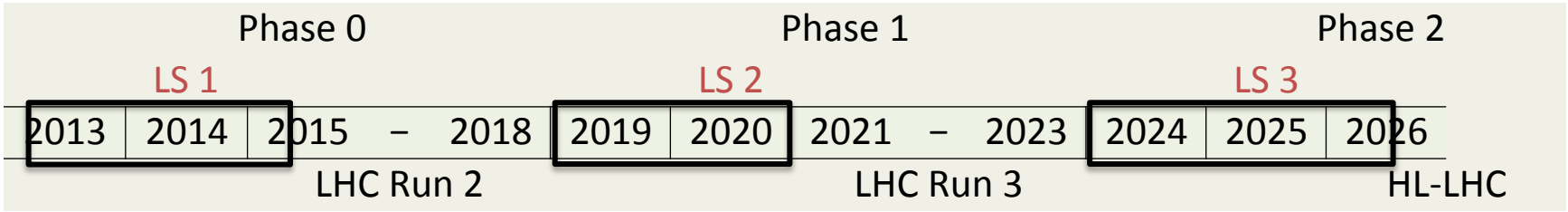


TileCal Signal Chain

- PMT signals are conditioned and amplified by two channels with gain ratio of 1:64 (3-in-1 card)
- Pulses are digitized by 10-bit ADC at 40 MHz
- The digital signals are sent to back-end through an optical interface (Interface Board)
- Compact information (tower sum) is sent to ATLAS LVL1 trigger (analog signals) (Trigger Boards)

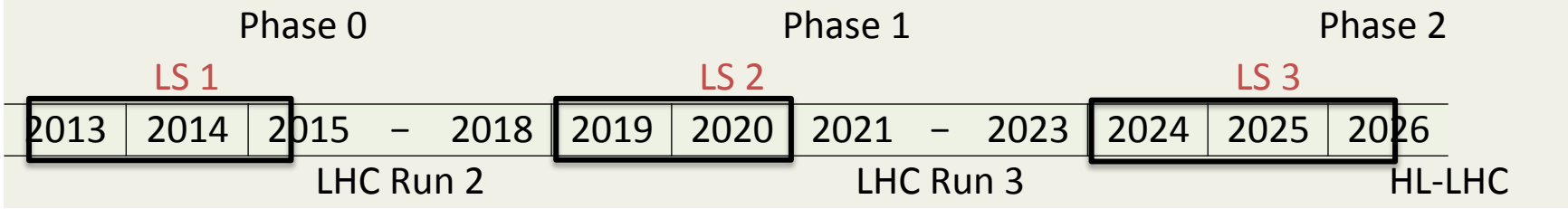


The ATLAS Upgrade Program



- Phase 0: occurred during 2013-2014 (Long Shutdown 1), and prepared the LHC for Run 2 (peak luminosity 1.5 x 10^{34} cm^2s^{-1})
- Phase 1: foreseen for 2019-2020 (Long Shutdown 2). It will prepare the LHC for Run 3 (peak luminosity reaches 2 x 10^{34} cm^2s^{-1})
- Phase 2: foreseen for 2024-2026 (Long Shutdown 3). It will prepare the collider for the HL-LHC operation (5-7 x 10^{34} cm^2s^{-1})

TileCal Upgrade Summary

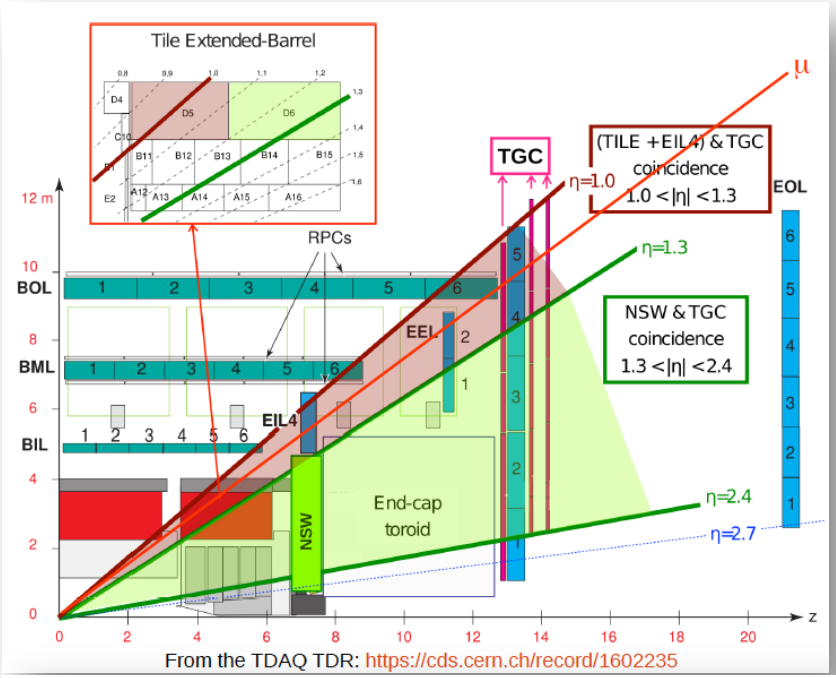


- LS 1**:** installation of the new low voltage power supplies and the activation of the TileCal third layer signal for assisting the muon trigger at 1.0<|η|<1.3 (**TileMuon Project**)
- LS 2**:** it is foreseen the replacement of the gap scintillators
- LS 3**:** a major upgrade in the **TileCal readout electronics** is planned. Except for the photomultipliers tubes (PMTs), most of the on- and off-detector electronics will be replaced

TileMuon Project

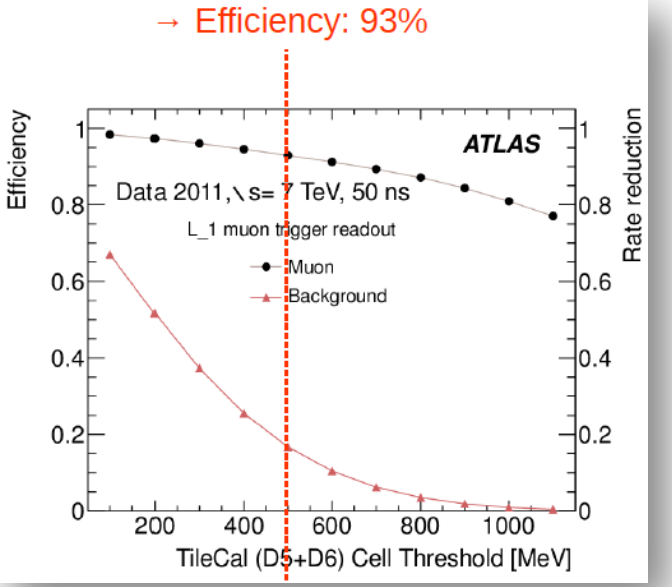
- The TileMuon project aims at reducing the muon trigger rates due to the low energy charged particles, which interact with the muon detector, by using the TileCal third layer signal (D layer) during LHC Run 2 & 3
- Protons emerging from the endcap toroid and beam shielding were the main source of trigger background for the L1Muon endcap
- The TileCal 3rd layer analog signal was already available in the USA15 cavern.
- The development of an electronic system to digitize, detect, process and communicate with the muon endcap trigger was required

TileMuon Project

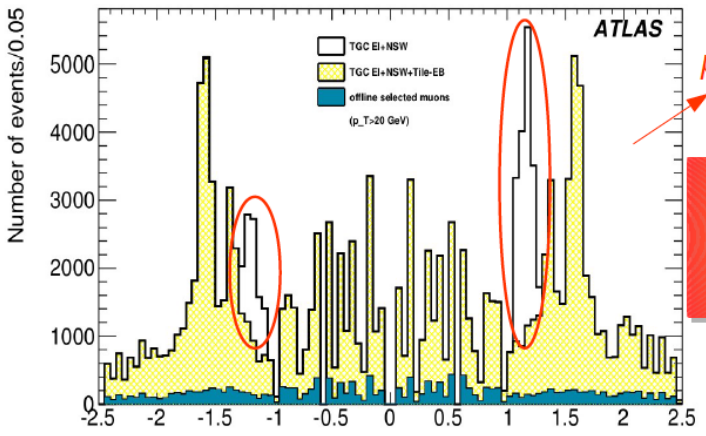


From the TDAQ TDR: https://cds.cern.ch/record/1602235

Tile extended barrel matches the muon endcap region (TGC) 1.0<|η|<1.3



Muon trigger in coincidence with Tile: 92% efficiency with 80% fake muons reduction (500 MeV cut)



From the TDAQ TDR: https://cds.cern.ch/record/1602235

p_T theshold of 20 GeV → L1_MU20

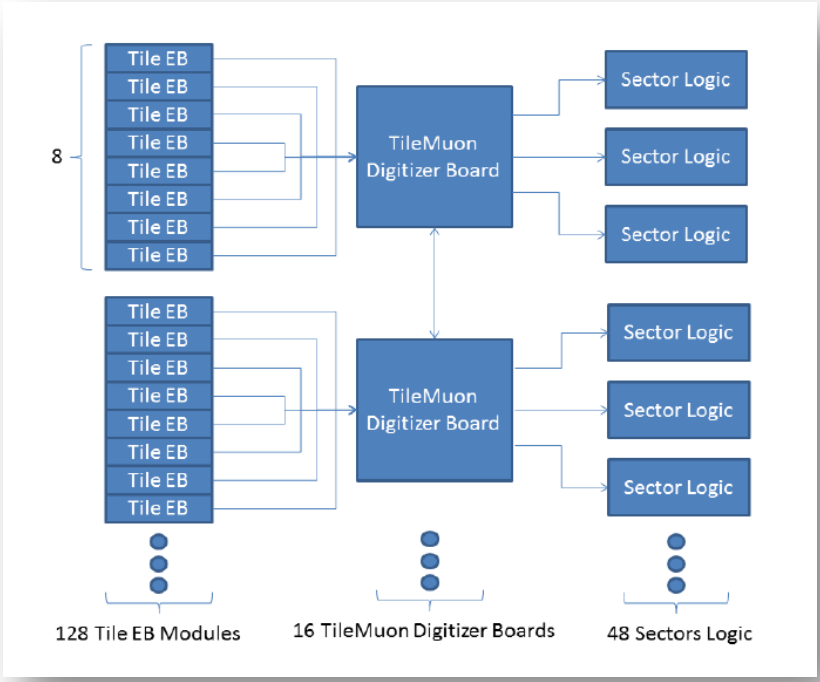
Improve rejection in 1.0 < |η| < 1.3 (not covered by the NSW)

→ BW-TGC + Tile EB (D5+D6)

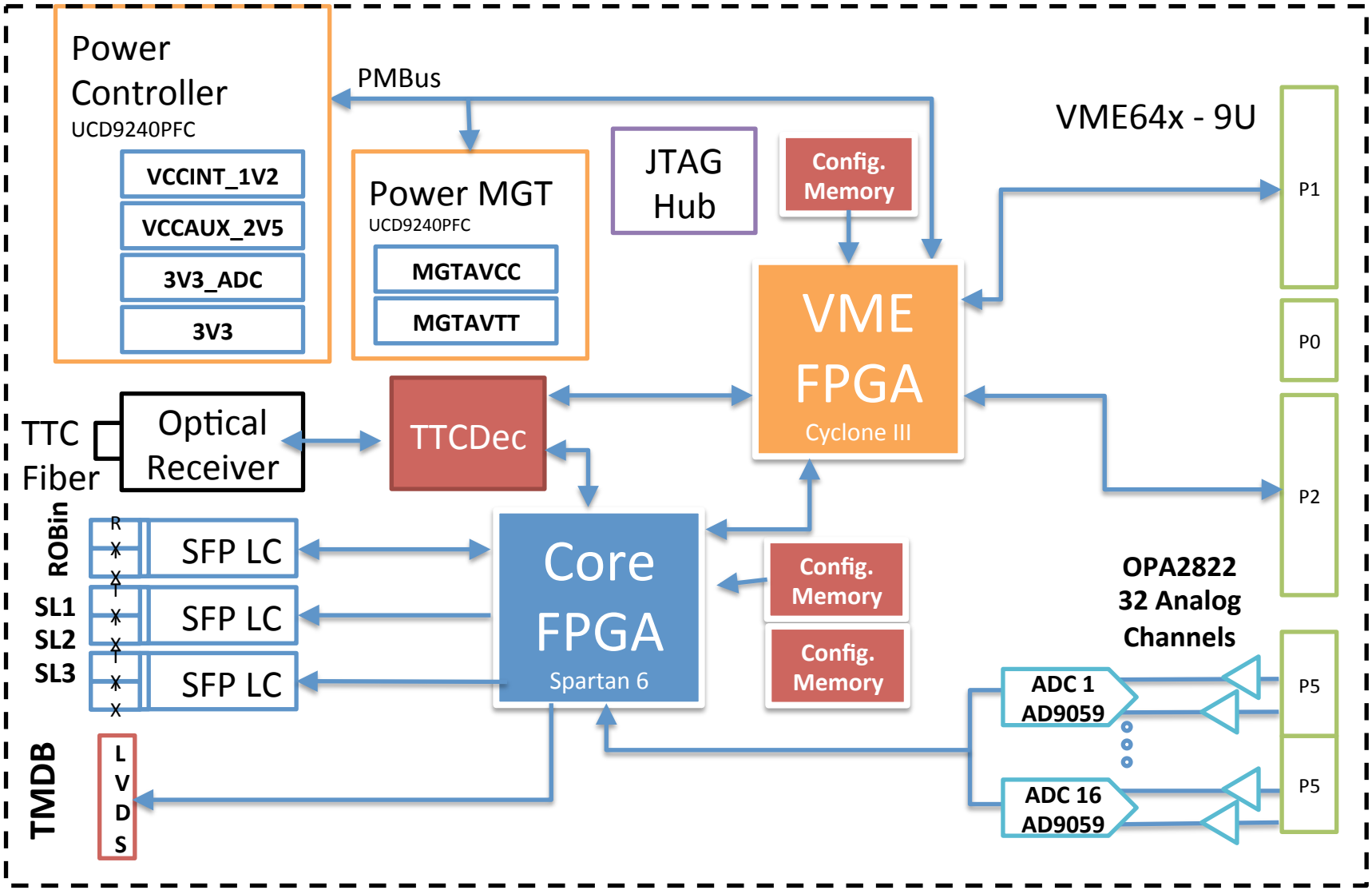
The coincidence with TileCal reduces the trigger rates due to fake muons in the extended barrel region 1.0<|η|<1.3

TileMuon System Overview

- Each receiver board interfaces 8 TileCal modules with 3 Sector Logic Blocks
- The 32 channels from the 16 TileCal cells are available at the core FPGA for processing
- One VME crate in USA15 for the 16 receiver modules, a second crate will be used to receive some TileCal barrel modules
- The TTC optical signal is received in each board
- Clock and control signals (TTC) through the TTCDEC mezzanine in each board
- Communication between boards using LVDS
- Output data available through optical links:
  - A hit to the muon sector logic (Glink)
  - ROD functionality (Slink)

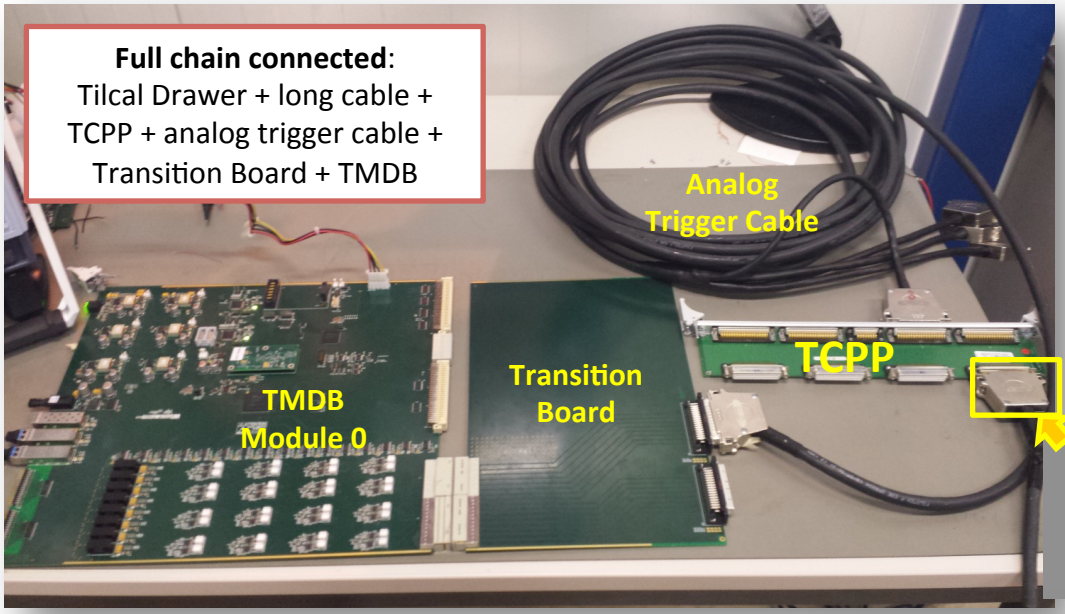


TileMuon Digitizer Board (TMDB)

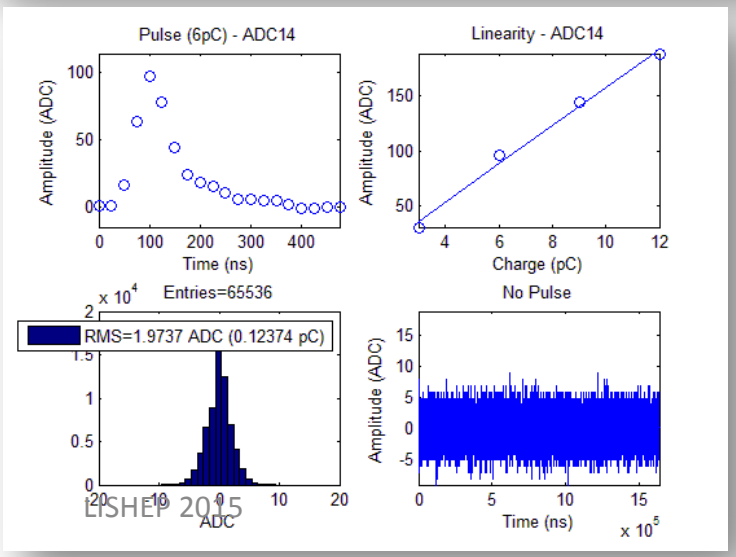


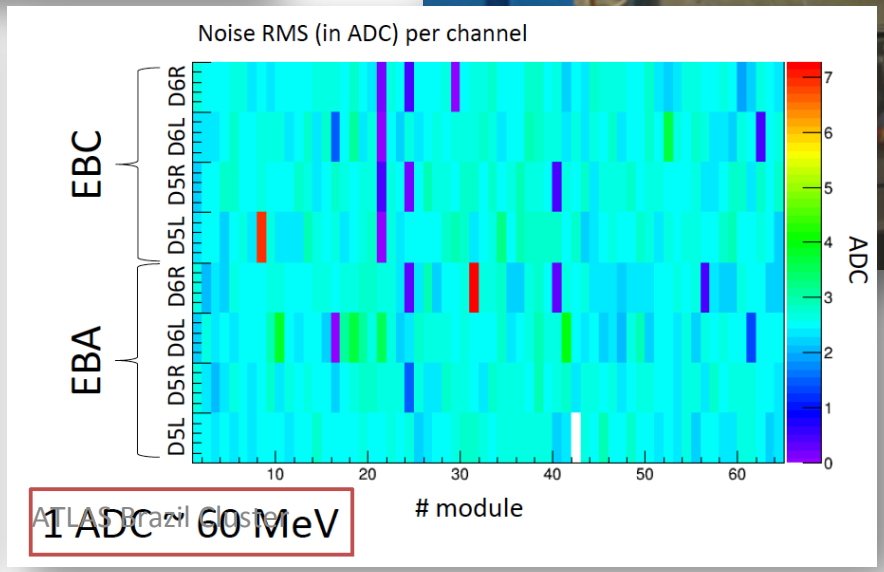
TileMuon System

Full chain connected:
Tilcal Drawer + long cable +
TCPP + analog trigger cable +
Transition Board + TMDB



TileCal
Drawer
Trigger
Output





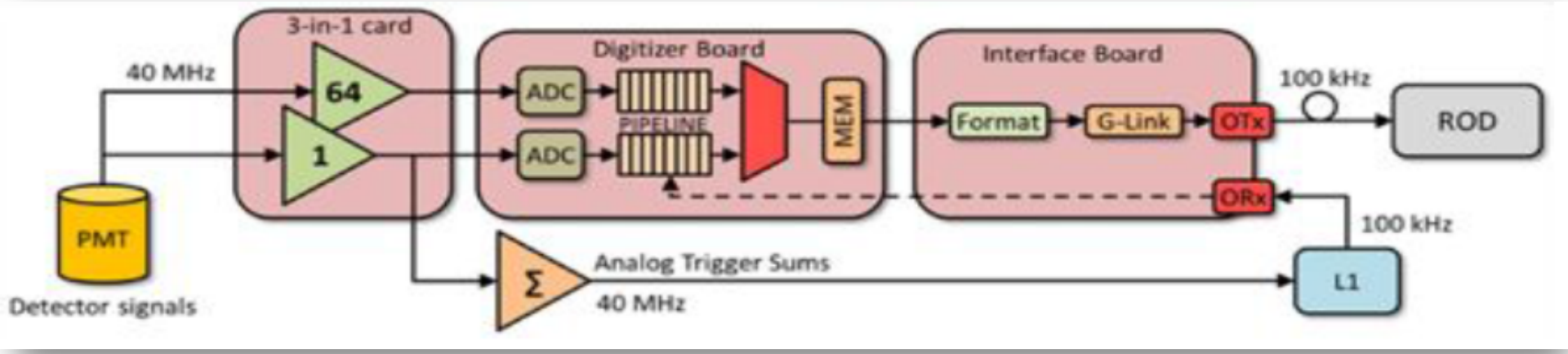
TileMuon Status

- The required infrastructure and all 16 TMDB boards are already installed in USA15 cavern
- More than 96% of the channels (512 in total) are working within the required specifications
- Communication with the muon sector logic (glink) is almost fully operational
- Commissioning ongoing
- Operation until the end of 2015 or 2016

Phase 2 Electronics Upgrade

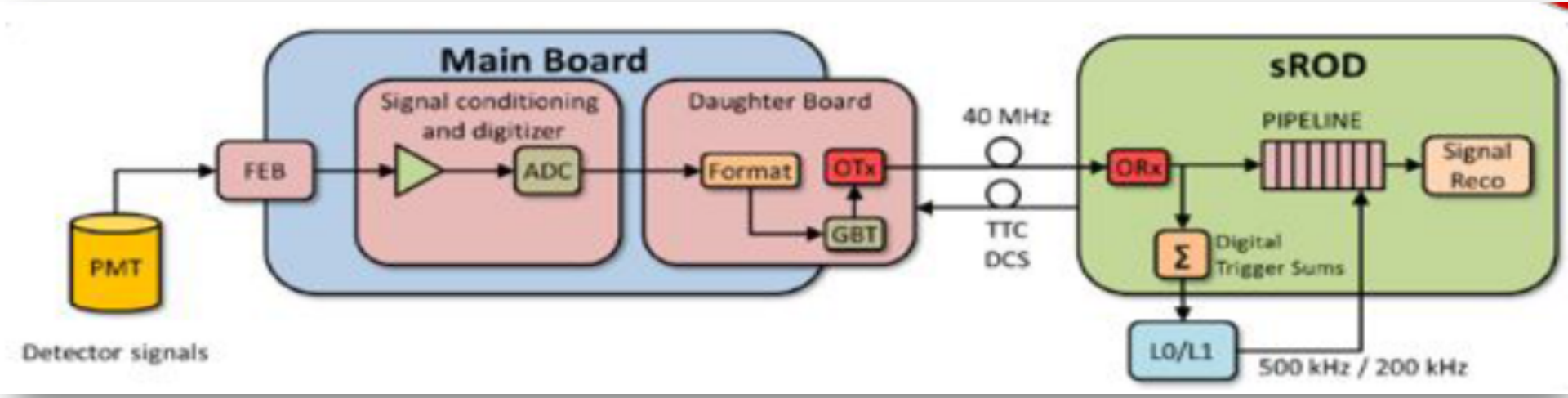
- Increase of the LHC luminosity at LHC
  - The system needs to cope with higher initial event-rates
  - On-detector electronics exposed to higher radiation levels
  - More fake muons
- More selective trigger system – more complex algorithms
  - Introduce lvl0 trigger to reduce lvl1 input rate
  - Use track trigger at lvl1
  - Trigger towers with improved spatial resolution
  - Topological trigger at lvl1
  - Better muon identification
- most of the on- and off-detector electronics must be replaced

Electronics Current Architecture



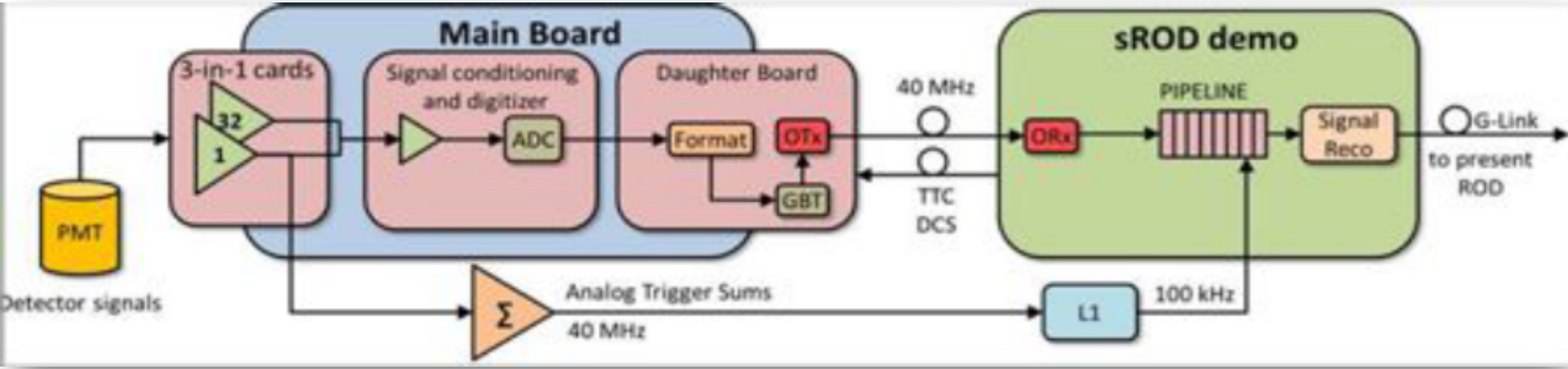
- On detector:
  - 3-in-1 front-end board: shaping/amplification, integration, calibration
  - Mother board: programming, control and powering
  - Digitizer cards: digitization and data processing
  - Interface card: optical transceiver to the ROD at 100 kHz
  - Trigger board: analog trigger tower builder
- Off detector:
  - Readout driver (ROD): back-end electronics

Phase 2 Architecture



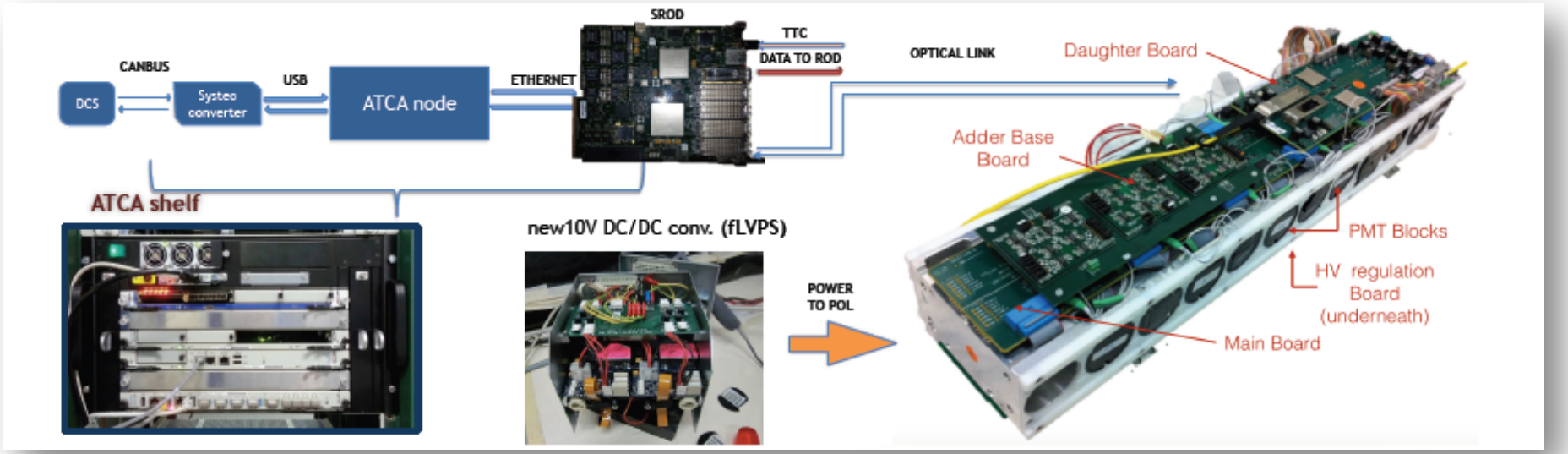
- Simplification: reduced number of boards and interconnections
- On-Detector:
  - Front-end board: three options currently under evaluation
  - Main Board: data processing and control
  - Daughter Board: data transmission
- Off-Detector:
  - Super readout driver (sROD): back-end electronics

The Demonstrator Project

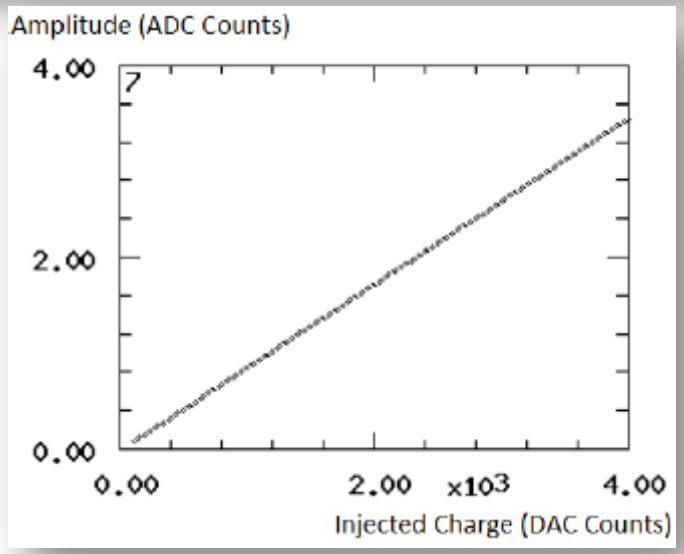


- Should contain as much of the final Phase 2 design as possible while being compatible with the present system
- However, the demonstrator may be modified on several occasions to verify new solutions
- Provide both digital and analog trigger data (3-in-1 only)
- The sROD system will interpret the TTC and the DCS commands and translate new detector data into a form acceptable by the present ROD
- Planned insertion in TileCal in 2016 Christmas shutdown
- The FEBs will be evaluated in test beams 2015-2016

The Demonstrator Project



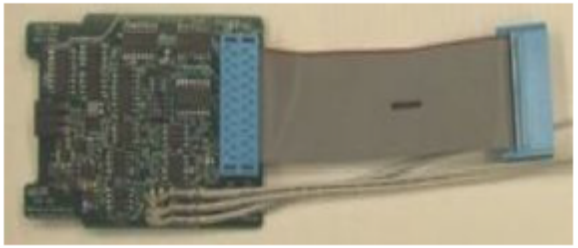
- Validation of the demonstrator prototype is ongoing
- Calibration data is being used to asses the system performance



Front-End Electronic Board Options

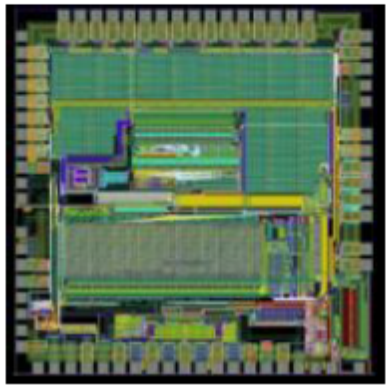
Modified 3-in-1

- Receive and shape
  - Provides analog output (2 gains)
  - Charge injection
  - Integrator
- Based on current 3-in-1 cards
  - Commercial off the shell
- 17-bit dynamic range
- Improved
  - Radiation tolerance
  - Noise performance
  - Linearity performance



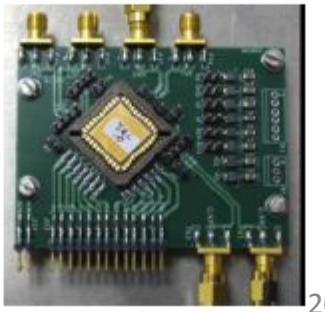
QIE ASIC

- Charge Integrator from Fermilab
- Different approach
  - Current splitter
  - Gated integrator
- Four different gains, but without shaping
  - No dead time
  - Useful for pile-up
- 17-bit dynamic range
- Clean measurement every 25 ns (40 MHz)



FATALIC

- Combines two ASIC solutions: FATALIC (Front-end for ATLAS TileCal Integrated Circuit) and TACTIC (Twelve bits AdC for atlas Tilecal Integrated Circuit)
- FATALIC
  - Shaping stage with 3 gain ranges (1, 8, 64)
  - 18-bit dynamic range
- TACTIC
  - 12-bit pipelined ADC
  - 40 MHz operations



Summary

- TileCal is facing challenging R&D activities due to the required upgrade activities for high luminosity
- For LHC Run 2, the main upgrade activity was related to the activation of the D-layer signal in order to be used in coincidence with the muon endcap trigger (TileMuon Project)
  - The TileMuon Project begun by the end of 2013 and is now in commissioning
  - A great effort from the TileCal and Muon Trigger communities
- For the HL-LHC, almost all the TileCal electronics will be replaced
  - The on-detector electronics will be completely modified. A new and more efficient architecture was conceived; three front-end boards are under evaluation; the trigger will be digital with full detector granularity available; increase of the output data rate (40 MHz)
- A demonstrator program is ongoing based on a hybrid version of the electronics drawer in order to be compatible with the present system
  - The installation of the first demonstrator in drawer in TileCal is foreseen for the end of 2016