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GigaTracker, a Thin and Fast Silicon Pixels Tracker

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GigaTracker, the NA62's upstream spectrometer, plays a key role in the kinematically constrained background suppression for the study of the $K^+ \to \pi^+ \nu\bar{\nu}$ decay. It is made of three independent stations, each of which is a six by three cm^2 hybrid silicon pixels detector. To meet the NA62 physics goals, GigaTracker has to address challenging requirements. The hit time resolution must be better than 200 ps while keeping the total thickness of the sensor to less than 0.5 mm silicon equivalent.

The 200 µm thick sensor is divided into 18000 300 µm $\times$ 300 µm pixels bump-bounded to ten independent read-out chips. The chips use an end-of-column architecture and rely on time-over-threshold discriminators. A station can handle a crossing rate of 750 MHz. Microchannel cooling technology will be used to cool the assembly. It allows us to keep the sensor close to 0°C with 130 µm of silicon in the beam area.

The sensor and read-out chip performance were validated using a 45 pixel demonstrator with a laser test setup and during a test beam. The time resolution was found to be better than 175 ps, well within the specifications.

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1. Introduction

Rare $K \to \pi\nu\bar{\nu}$ decays are good probes for beyond the Standart Model (SM) effects. They involve Z-penguin and electroweak box diagrams dominated by an internal top quark loop and are therefore governed by short distance dynamics. Since these processes are flavour-changing neutral current the long distance contributions are suppressed in the SM by the Glashow-Iliopoulos-Maiani (GIM) mechanism[1].

The involved Cabibbo-Kobayashi-Maskawa (CKM) matrix elements, $V_{\rm ts}$ and $V_{\rm td}$, are small furthermore reducing the branching ratios[2].

The hadronic matrix element contributions can be extracted from the $K^+ \to \pi^0 e^+ \nu_e$ decay[3]. As a consequence we have a very good theoretical prediction for the branching ratio[2]:

$$\mathrm{BR}\left(K^+ \to \pi^+ \nu\bar{\nu}\right)_{\rm SM} = \left(7.81^{+0.80}_{-0.71} \pm 0.29\right) \times 10^{-11} ,$$
$$\mathrm{BR}\left(K_L \to \pi^0 \nu\bar{\nu}\right)_{\rm SM} = \left(2.43^{+0.40}_{-0.37} \pm 0.06\right) \times 10^{-11} .$$

These results include NNLO QCD and NLO electroweak corrections to the quark charm loop and NLO QCD and 2 loop electroweak corrections to the top quark loop. The first error is related to the input parameters uncertainties. The second error is linked to remaining theoretical uncertainty.

Yet, the measurement of such a small branching ratio is very challenging. In 1997 the E787 collaboration[4] gave the first evidence of the $K^+ \to \pi^+ \nu\bar{\nu}$. In 2008, combining the data of E787 and E949, the E949 collaboration reported[5]

$$\mathrm{BR}\left(K^+ \to \pi^+ \nu\bar{\nu}\right)_{\rm E949} = \left(17.3^{+11.5}_{-10.5}\right) \times 10^{-11} .$$

The $K_L \to \pi^0 \nu\bar{\nu}$ branching ratio is presently being studied by the KOTO experiment in J-PARC[6].

NA62[7] aims to collect of the order of 50 $K^+ \to \pi^+ \nu\bar{\nu}$ decays per year with a 10% background level. This would bring the precision of the experimental value to the theoretical one.

The experimental apparatus is currently being build at CERN SPS. Its design is optimised for the $K^+ \to \pi^+ \nu\bar{\nu}$ channel. We use a 75 GeV/c high intensity unseparated hadron beam containing 7% of kaons. The kaons decay in flight in a 60 meters fiducial volume. NA62 uses event kinematics to reject more than 90% of background. To this end we rely on two spectrometers, *GigaTracker* upstream of the fiducial volume, *STRAW* downstream of the fiducial volume.

The backgrounds that are not constrained by kinematics are addressed by particle identification detectors and photon and muon vetos. To keep unwanted interactions at minimum level, the pressure in the whole experiment is kept at the 10^{-6} mbar level and care has been taken to reduce the material in the beam line to a minimal amount.

This paper is organised in two main parts. In the first section, we present the architecture of the GigaTracker spectrometer. The second section focuses on experimental results we obtained with a small scale demonstrator and test of different subcomponent of the final detector.

2. GigaTracker Architecture

GigaTracker[8], the NA62 upstream spectrometer, measures the momentum, direction and time of passage of all incoming particles. It is composed of three independent stations placed on

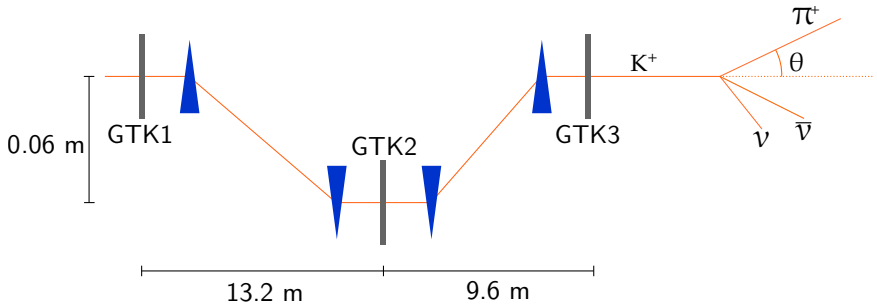


Figure 1: Sketch of the GigaTracker (GTK) layout viewed from the side. The four triangles represents the achromatic magnets.

the beam axis. To allow the momentum measurement the middle one is displaced by 60 mm on the vertical axis and placed between four achromatic magnets (Fig. 1).

Each station is a 60×27 mm^2 hybrid silicon pixel detector operated in vacuum. The requirements for these detectors are demanding. Each station has to sustain a high and non-uniform crossing rate of 1.3 MHz/mm^2 in the center part and 750 MHz in total. To match the incoming kaon and its decays products in the high rate environment the hit time resolution must be kept below 200 picoseconds.

In order to reduce inelastic scatterings and therefore accidental backgrounds, the total thickness of each station must be less than 0.5 mm (< 0.5 % of one radiation length).

Finally, due to the harsh radiation environment the sensor has to be cooled to 5°C to keep the performance to the required level during the station lifetime. A station exchange every 100 days of beam (or a fluence of $\approx 2 \times 10^{14}$ 1 MeV n_{eq}/cm^2) is foreseen. The leakage current of the sensors will be monitored.

The combination of these three characteristics, fast, thin and cool, is new for hybrid silicon pixel detectors.

In the following subsections we will briefly review each subcomponent of the station from the sensor to the mechanical integration.

Sensors

The active area covers 60×27 mm^2. The area is then divided in 18000 300 µm $\times$ 300 µm pixels arranged to form a 200×90 matrix. This was chosen to match the beam size. The pixel size is small enough to meet the requirement in terms of angular (16 µrad) and momentum resolution ($\sigma(p)/p \approx 0.2\%$).

It has been shown that a thickness of 200 µm was enough to generate enough signal while keeping the timing requirements within the limits. To guarantee the quality of the bump-bonding process we have strict tolerances for the thickness ($\pm$10 µm) and the maximal sagitta (30 µm).

Since the read-out chips are able to handle p-in-n and n-in-p structures both type of sensors have been considered. Currently the standard option is to use the p-in-n technology. The n-type substrate is phosphorous doped and has a resistivity in the range of 4-8 kΩcm.

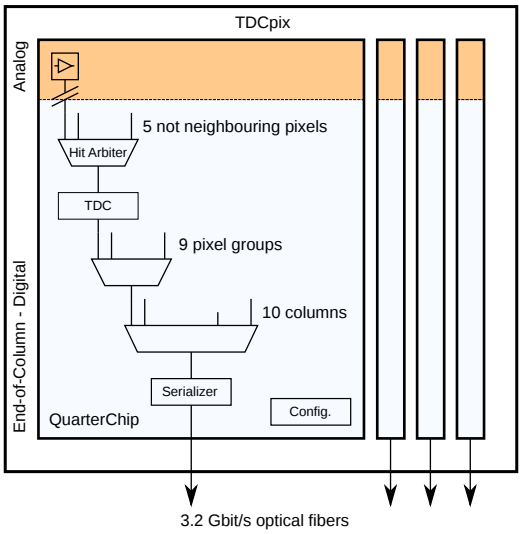


Figure 2: Sketch of the architecture of the read-out chips. Each chip is subdivided in four identical "QuarterChip" sections.

To ensure the timing properties the sensor has to be operated highly over-depleted. A multi guard ring structure has been integrated into the sensor design. This will allow us to use bias voltages above 500 V.

Radiation hardness studies have been carried out on both structures. The results are briefly discussed in section 3.

Read-out Electonics

The sensor area is covered by 10 identical and independent read-out chips. This design allows to share the rate between the chips. Each one of these chips covers an area of 12×19 mm^2 and serves 1800 pixels. They exceed the sensor by 5 mm on one edge. This space outside of the beam acceptance carries most of the digital part of the read-out electronics and will be used to connect the chips to the world. The final chip thickness will depend on the cooling solution chosen (see next section) but it will be between 100 µm and 150 µm.

The chips are built using standard 130 nm CMOS technology and follow and "end-of-column" architecture[9]. At the pixel level, charges are collected by an analog front-end made of a fast preamplifier, a shaper and a discriminator. After the discriminator, the signal is routed via a transmission line to the end-of-column area where it is converted to digital words by a time-over threshold TDC. Each TDC serves five not-neighboring pixels. For each hit we time tag the leading and the trailing edge. The data is then sent to a high speed serializer and finally off-chip (Fig. 2).

The end-of-column approach has the advantage of not requiring the distribution of the high frequency clock signals to the pixels.

Each chip ships the data via four 3.2 Gb/s optical links to an external read-out card. The card is built around a FPGA and two DDR2 SDRAM modules. We use a trigger-less approach. The data are stored in a circular buffer and sent to the NA62 DAQ via Gigabit Ethernet link only when it is requested by the trigger system.

(a) (b)

Figure 3: Sketch of the two cooling solution. The sensor is in red, read-out chip in green, glue in yellow and the cooling plate in gray. Beam is going from bottom to top.

The dissipated power of the chip was estimated to be approximately 0.4 W/cm^2 for the analog part and approximately 2.95 W/cm^2 for the digital part. These were key figures for the development of the cooling solution.

Cooling

The sensor must be kept at low temperature ($< 5^{\circ}$C) to cope with the radiation damages. The cooling solution has to be able to remove 2.95 W/cm^2 on the edge of the read-out chip (digital part). At the same time, the total thickness of the GigaTracker station has to be kept under 0.5 mm silicon equivalent. The micro-channel cooling technology meets both requirements.

Micro-channels are made by etching small grooves (200 µm $\times$ 70 µm) into the silicon wafer. The channels are covered by another silicon wafer and joined together by anodic bounding. Top and bottom wafers can then be thinned to 30 µm. The last stage is to solder two connectors on the assembly.

Currently two options are under investigation. First, the "baseline" scenario: micro-channels run under the whole sensor area (Fig. 6a). Second, the "frame" option, micro-channels run only under the digital part of chips (Fig. 6b). The frame option has the advantage to allow a thinner cooling plate in the beam area but at the price of thicker chips. This is needed to remove the heat from the central part of the sensor.

We have full scale prototypes for both solutions, the characterization is ongoing (see section 3).

Mechanical Integration

The two first GigaTracker stations will be held in independent cylindrical stainless steel vessels. The third one is only 27 mm away from the *CHANTI* detector and will therefore share the same enclosure.

The vessel design takes into account the fact that we will have to replace the station during the experiment lifetime. They will be easily swappable and an alignment device is integrated into each vessels.

3. GigaTracker in Practice

In this section we present some important results obtained with various test devices. We have full scale prototypes of the cooling plates, demonstrators of the read-out chip, and a few sensors. During the sensor fabrication diodes were placed next to them on the silicon wafers. After the production, they were diced and used for radiation hardness test purposes.

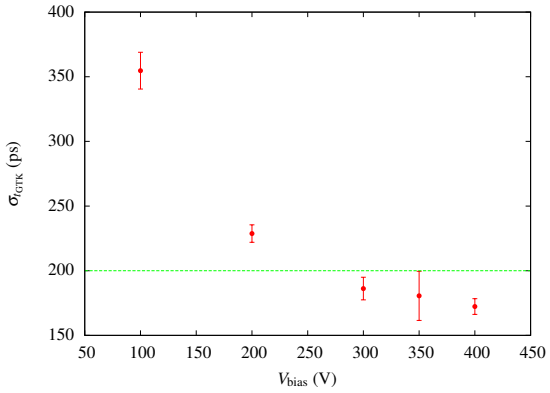


Figure 4: The graph shows the hit time resolution as a function of the bias voltage. For resonable bias voltage (> 300V) we are well under the required 200 picoseconds.

In 2009, demonstrator ASICs were produced by IBM. The prototype includes 45 pixels and the full electronic chain up to the time-over-threshold TDC. The read-out was simplified compared to the final version of the chip. A series of tests were carried out with and without sensors bump-bonded to the ASIC. The main goals were to assess the time resolution, the charge collection efficiency and the read-out efficiency.

Full scale mock-ups of the micro-channel cooling plate were produced for both options under investigation. A set of heaters glued on top of the assembles allowed to simulate different power output scenarios. Mechanical stress tests were also conducted on the assemblies.

Laser Test Bench

The first tests were made using a laser test bench. The objective was to study the timing behavior of the full chain, sensor and read-out electronics combined. The effect of the impact position in the pixel surface was also carefully studied. The results are reported in the NA62 Technical Document[7].

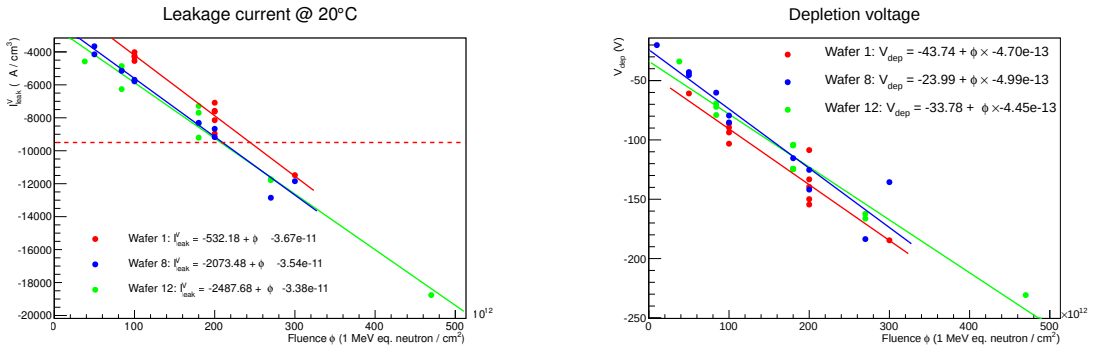
Test Beam

In fall 2010, a test beam was carried out using the CERN PS infrastructure. Four GigaTracker demonstrators were placed between a set of fast scintillators and put in a 10 GeV/c beam. The fast scintillators were used as a trigger signal and time reference ($\sigma_t = 45$ picoseconds).

The main result is summarized in the Fig. 4. The hit time resolution was found to be less than the 200 picoseconds target for bias voltage higher than 300 V. This voltage is well within specification and gives us margin to compensate some of the performance loss due to the radiation damages.

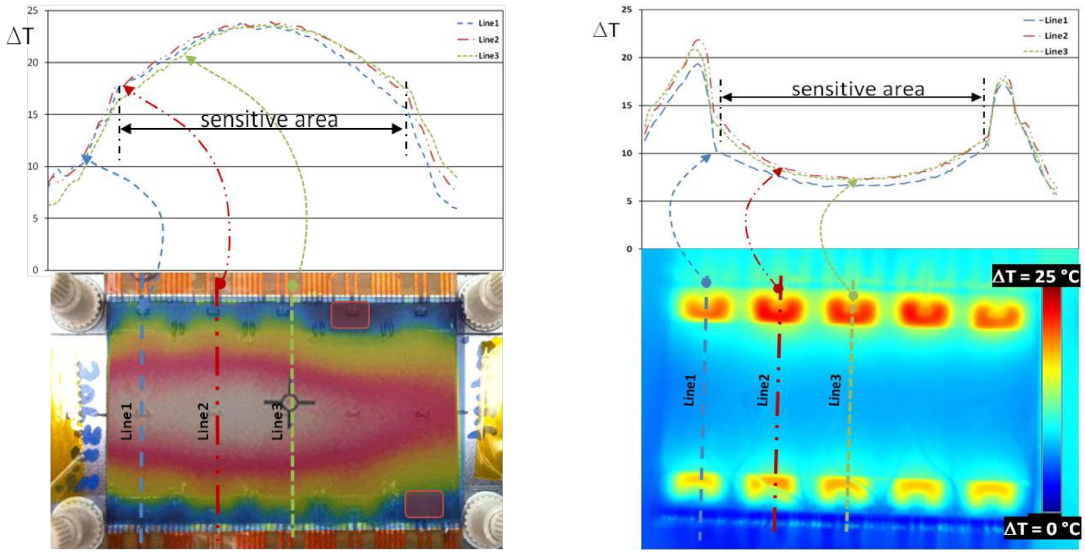
Radiation Hardness

The test diodes were irradiated by 50 MeV/c protons at Centre de Ressources du Cyclotron, Louvain-la-Neuve. Diodes were exposed to fluxes from 1×10^{13} to 4.7×10^{14} 1 MeV n_{eq}/cm^2. They were immediately stored in a container at $-20°C$.



(a) (b)

Figure 5: Main results of the radiation hardness tests carried on n-in-p test diodes. The dashed red line marks the maximum allowable value for the leakage current. 100 days of operation corresponds to a fluence of $\approx 2 \times 10^{14}$ 1 MeV n_{eq}/cm^2.



(a) (b)

Figure 6: The figure shows thermal images and the corresponding temperature profile across the sensor surface. The frame option is on the left and the base option is on the right.

The irradiated diodes were then characterized at Semiconductor Lab, CERN. For each diode an I-V and a C-V curve were measured. The leakage current and full depletion voltage were extracted. The results are summarized in Fig. 5a and 5b.

Similar measurements were made for p-in-n test diodes in 2008[10].

Cooling

The measurements are presented at the Fig. 6b and 6a. The top plots show temperature difference in °C. between temperature at the coolant inlet and the sensor surface temperature as a function of the position. The results presented are worst case scenario, a dissipated power of 4 W/cm^2 for the digital part and 0.65 W/cm^2 for the analog part of the chip.

Compared to be baseline option, the frame option has poorer thermal performance but costs less and is easier to build and integrate. Both solution are viable, the final decision will be taken in the following months.

4. Summary

GigaTracker is an innovative silicon pixels tracker. It has to meet a demanding set of requirements. The hit time resolution must be less than 200 picoseconds, the thickness below 0.5 mm silicon equivalent and sensor temperature has to be kept below 5°C. This was achieved by using novel techniques like micro-channel cooling and new read-out chip architecture.

To assess the performance of the design, a 45 pixel demonstrator was build and tested using a laser test bench and during a test beam. The hit time resolution was found to be less than 175 picoseconds for bias voltage of 300V, well within the requirement. The micro-channel plate was tested with a sensor mockup. The first results are inline with the expectation.

The prototype meets all the specifications. We are now building the full scale detector. The integration the GigaTracker in the NA62 experimental apparatus should be completed in fall 2014.

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