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Design of the analog front-end for the Timepix3 and Smallpix hybrid pixel detectors in 130 nm CMOS technology

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ABSTRACT: This paper describes a front-end for hybrid pixel readout chips, which was developed for the Timepix3 and Smallpix ASICs. The front-end contains a single-ended preamplifier with a structure for leakage current compensation which can handle both signal polarities, and a single-threshold discriminator with compensation for pixel-to-pixel mismatch. Preamplifier and discriminator are required to be fast, to allow a Time-Of-Arrival (TOA) measurement with a resolution of 1.56 ns. Time-Over-Threshold (TOT) is also measured; the monotonicity of TOT with respect to the input charge is greatly improved as compared to the previous Timepix chip. The analog area is only 55 μm $\times$ 13.5 μm. Timepix3 has already been fabricated and the first test results are also presented in this paper.

KEYWORDS: Analogue electronic circuits; Pixelated detectors and associated VLSI electronics; Electronic detector readout concepts (solid-state); Front-end electronics for detector readout

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1 Introduction

The Medipix team at CERN [1] develops readout ASICs for hybrid pixel detector applications (sensors or detectors generate signals which are read out by a separated chip). In this field, there is a demand for fast readout of different types of pixelated sensors, at low-medium hit rates and with high spatial resolution. Such a readout system can be used by the High-Energy Physics community, for example for the readout of solid-state vertex detectors, or also for gaseous detectors, such as Time-Projection Chambers (TPC) equipped with GEM or MicroMegas readout. A large system, with many thousands pixels, finds applications also in powering tests for the vertex detector of the future Linear Collider (power pulsing), and in the domains of dosimetry and X-ray imaging.

Two chips are particularly interesting for these applications: Timepix3 and Smallpix. The former has been designed and fabricated; the first tests are taking place in this period and preliminary measurements are reported in this paper. Smallpix is under study and it is expected to reuse the front-end designed for Timepix3.

1.1 Timepix3

Timepix3 is the successor of Timepix [2]. Timepix was developed in a 250 nm CMOS technology and provides arrival time (TOA), charge by means of time-over-threshold (TOT) or event/photon counting (PC) measurement. Timepix3 has the same pixel arrangement as Timepix, a matrix of 256×256 pixels with a pitch of 55 μm in both directions, but is capable of simultaneous TOA and

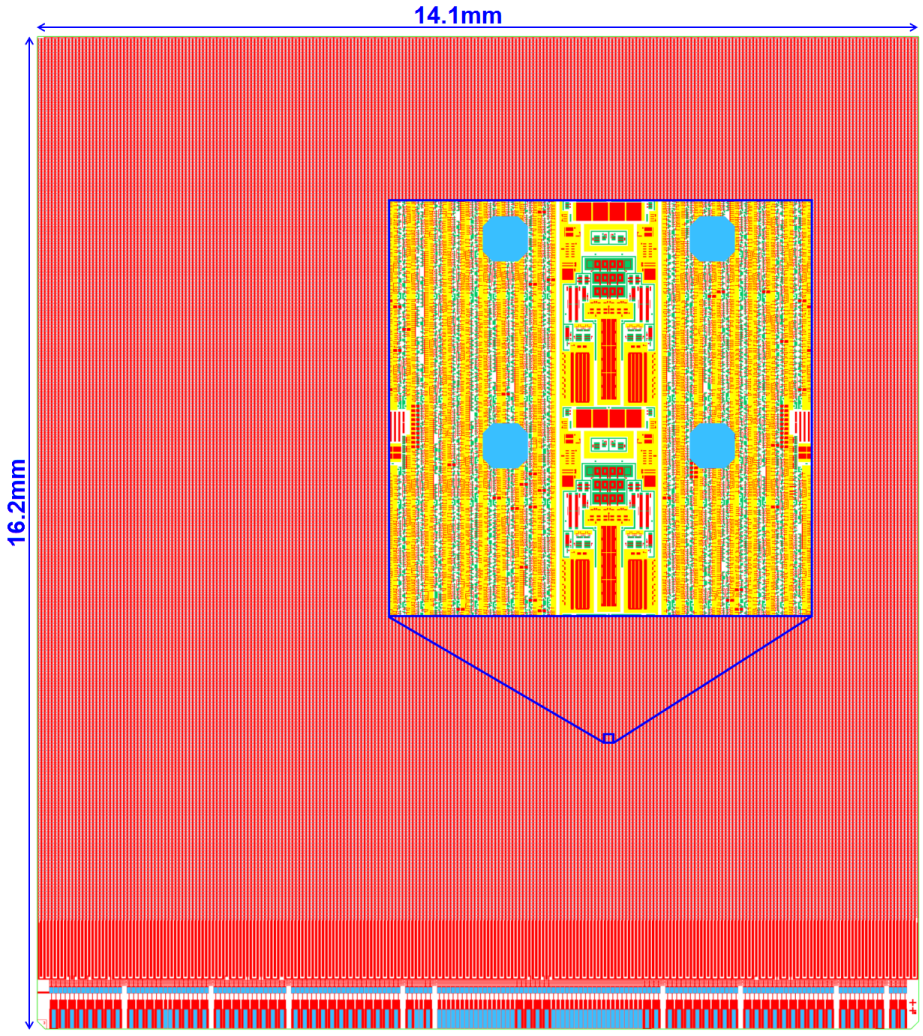

Figure 1. Layout of Timepix3. The matrix contains 256×256 pixels at 55 μm pitch; in the explosed rectangle, four pixels are visible, with limited area allocated to the analog front-end and the pads (blue octagons) sitting on top of digital circuits. The chip is buttable on three sides, while the 4^{th} side (bottom) hosts periphery and wirebond pads.

TOT or PC and integral TOT (iTOT) measurement. The design effort for this chip has been shared between CERN, University of Bonn (Germany) and NIKHEF (Netherlands). Figure 1 depicts the chip layout.

Timepix3 is operated by means of an external shutter signal and offers two main measurement modes: TOT & TOA or event counting and integral TOT. In the former, 10 bit TOT and 18 bit TOA are recorded simultaneously in each pixel. TOA is measured using a reference clock at a frequency of 40 MHz for the most significant 14 bits; the additional 4 bits of fine TOA measurement are provided by some Voltage-Controlled Oscillators (VCO), which are distributed across the pixel matrix. In the latter mode of operation, the number of hits is stored in a 10 bit register, while another 14 bit register computes the integrated TOT of all hits occurring during a period of the external shutter signal.

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A requirement that marks a difference between Timepix3 and the previous Timepix is that the measurement of TOT vs input charge must now be monotonic for large positive charges (holes) up to 300 kh^+.

The chip can be read out in two modes: at the end of the shutter period (classical sequential readout) or in data-driven mode. In the latter mode, Timepix3 sends out a 48 bit packet every time a pixel is hit; this optimizes the bandwidth of the system for the expected maximum hit rate of 40 Mhits/s/cm^2. In order to implement data-driven mode, pixels are grouped in clusters (2 by 4), named superpixels. Each superpixel contains a VCO generating a local clock at a frequency of 640 MHz, which is used for the fine TOA measurement with a resolution of 1.56 ns.

Timepix3 chips can be tiled next to each other on three sides in order to build a large detector. The additional dynamic shutdown/wake-up features of the chip make it suitable for power pulsing tests on large systems, which are necessary R&D steps for the future Linear Collider.

2 Front-end design

Table 1 summarizes the requirements of the analog front-end for Timepix3.

The available area is limited by the pixel pitch and the massive digital functionalities included in the digital area of each pixel. Because the measured quantity is time, signal amplitude linearity is not required. On the other hand, TOT must be monotonic for large positive charges and the TOA measurement must be adequate to the fine VCO timing resolution.

The time-to-peak of the front-end should be in the order of 25 ns, in order to yield a sufficiently low timewalk. This matches Large Hadron Collider (LHC) applications, where the main clock has a frequency of 40 MHz, and is particularly important in view of the VELOpix chip. VELOpix is a further development of Timepix3, now in design phase, and is intended primarily for the future upgrade of the VErtex LOcator of the LHCb experiment at CERN [3].

Each pixel is equipped with a threshold-equalization DAC (Digital-to-Analog Converter), which corrects for pixel-to-pixel mismatches. The target minimum applicable threshold is about 500 e^- (6σ). Therefore, the quadratic sum of noise and residual mismatch after equalization should be in the order of 90 e^- r.m.s. or less.

2.1 Front-end architecture

The front-end is based on a charge preamplifier with Krummenacher feedback [4] and a single-threshold discriminator. The full diagram is shown in figure 2.

The preamplifier has a cascoded single-ended input; as compared to the differential option, this choice allows a more efficient power usage at the price of increased sensitivity to pick-up noise from the substrate. The NMOS input transistor and its cascode are placed in a triple well, biased with a dedicated ground.

The feedback capacitor C_{fb} is only 3 fF, corresponding to a large preamplifier gain of 50 mV/ke^-. Such high gain is favourable because it reduces the impact of the discriminator on the overall mismatch and noise. As the measured quantity is time rather than amplitude, high gain and consequently small linear dynamic range are not an issue; at nominal operating settings, the amplifier is allowed to saturate for input charges as small as 12 ke^-.

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Table 1. Requirements of the Timepix3 analog front-end.

Parameter	**Value**
Area	55 μm $\times$ 13.5 μm
Signal polarity	Positive and negative
Detector capacitance	25 fF min - 50 fF typical - 100 fF max
Leakage current	-5 nA to +20 nA
Amplitude linearity	Not required
TOT monotonicity	Yes, up to 300 kh^+
TOA jitter and mismatch	Compatible with 1.56 ns resolution
Time-to-peak	Target 25 ns
Noise + threshold mismatch	90 e^-
On-pixel equalization DACs	4 bit
Power consumption	12 μW/pixel

Leakage current compensation is provided by the Krummenacher feedback network. Its current I_{Krum} is in the nA range and controls the discharge rate of the feedback capacitor: the TOT vs input charge relationship is ideally a linear function of I_{Krum}. Transistors in the feedback network operate in weak inversion at low current; therefore, all NMOS transistors are laid out as Enclosed-Layout Transistors (ELT) to improve their tolerance to radiation [5]. The current mirror which generates $I_{Krum}/2$ is implemented locally and shared between two neighbouring pixels, in order to save space. A dedicated supply line for the feedback network guarantees a low voltage drop along the columns of the pixel matrix, improving the uniformity of the feedback current.

The continuous-time discriminator is composed of a transconductance amplifier (OTA) followed by a two-stage amplification section (DAS). The OTA converts preamplifier output and global threshold into currents. The 4 bit current DAC can therefore adjust the currents in the two branches; by doing this, the effective threshold of each pixel can be shifted individually to compensate pixel-to-pixel mismatches. The largest mismatch contributors are the PMOS differential pair of the Krummenacher feedback, the NMOS generating $I_{Krum}/2$ and the input PMOS differential pair of the OTA. The equalization DAC is built with segmented and cascoded PMOS current sources. The sum of the two currents provided by each DAC is constant and uniform across the pixel matrix, independently of the 4 bit DAC code; this avoids issues with non-uniform current distribution across the pixel matrix.

Between OTA and amplification section, some switches are inserted to adapt discriminator polarity to detector signal polarity. The first amplification stage is a differential amplifier. The second stage is a current-starved inverter, which presents a transient current consumption only during switching and no consumption when the output is stable at either level (supply voltage or ground).

The discriminator output is fed to the digital part of the pixel. Its rising and falling edges provide TOA (time stamping of the hit) and TOT measurement (proportional to the energy deposited in the pixel).

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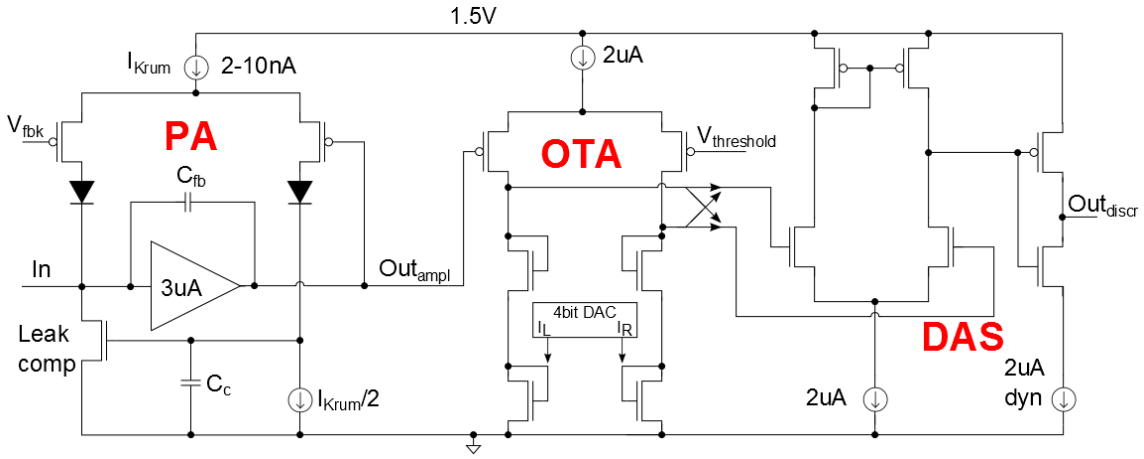

Figure 2. Diagram of the front-end. PA: preamplifier with Krummenacher feedback and diodes for the TOT monotonicity. OTA: discriminator OTA and pixel DAC for threshold equalization. DAS: discriminator amplification section.

2.2 TOT monotonicity

The diodes added to the Krummenacher feedback, visible in figure 2, avoid an unwanted effect observed in Timepix. When the sensor collects a very large number of holes, the input node voltage rises because the saturated preamplifier is not capable of attracting all the input charge to the feedback capacitor. For charges in the hundreds of kh^+ range, the input voltage increases so much, that without diodes the current in the Krummenacher feedback (through the PMOS connected to V_{fbk}) would reverse polarity and discharge rapidly the input following the wrong path (into C_c and, as a consequence, through the leakage compensation NMOS). The addition of PMOS diodes cuts this current path and ensures that the currents in the Krummenacher feedback are always in the correct sense. Figure 3 shows the expected improvement in TOT monotonicity due to the presence of these diodes.

2.3 Noise coupling

Digital functionalities occupy most of the pixel area. As visible in figure 1, the front-end input pads must sit over the digital domain. Therefore, the input pad area is reduced to $12\,\mu\text{m} \times 12\,\mu\text{m}$ (was $20\,\mu\text{m} \times 20\,\mu\text{m}$ in Timepix), in order to minimize parasitic coupling to the digital domain. Additionally, each pad is shielded using a lower metal connected to a clean analog ground.

Nevertheless, careful studies are needed to evaluate the impact of digital activity on the analog performance of the chip, especially concerning noise. After extraction of parasitic layout components, a model for simulation has been built. This model contains bondwire parasitics (mostly inductance), resistances of supply lines across the chip and distributed resistance and capacitance of bias lines along the columns of the pixel matrix; from a design point of view, the most troubling components are inductances and parasitic capacitances between nodes of different power domains (analog-digital). On the digital side, the largest noise contributor is the clock tree.

Figure 4 shows a simulation where the clock tree, switching at the nominal frequency of 40 MHz, injects pick-up noise into the analog domain. The simulation covers two pixels at the

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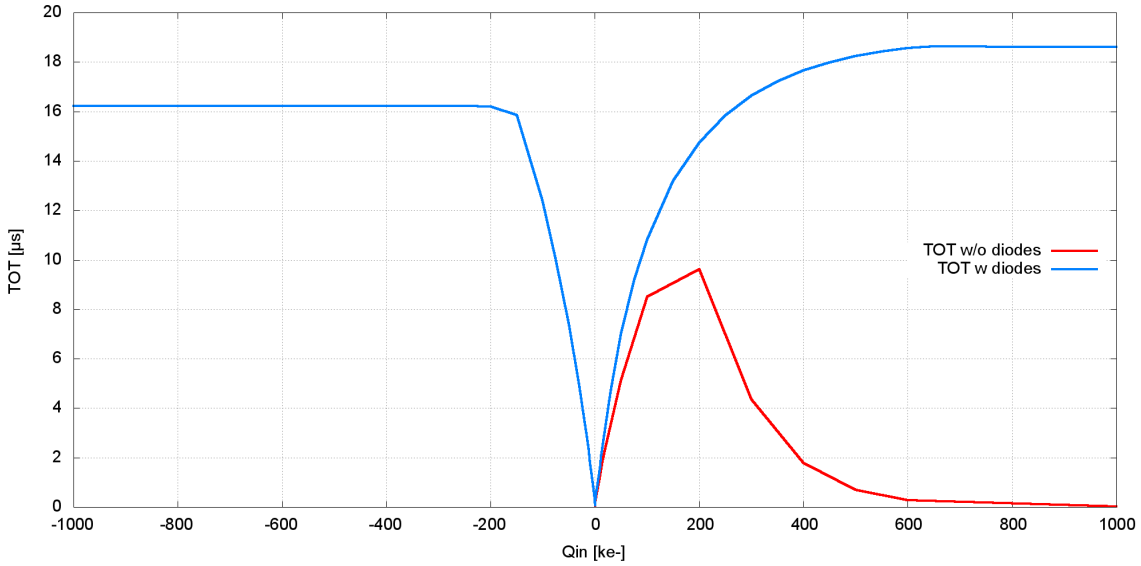

Figure 3. Simulation of TOT versus input charge. The red plot shows how non-monotonic the TOT characteristic would be if diodes were not added to the feedback network.

top of the chip, which is the most delicate area because it is furthest from the bondpads in the periphery. In one of the two pixels, no charge is present; in the other pixel, a pulse of 3 ke^- is injected. The simulation shows clearly that only the preamplifier output of the hit pixel crosses the threshold, while the non-hit pixel output stays well below threshold. Therefore, the noise injected from digital into analog domain is sufficiently small and mitigated by shielding.

2.4 Power pulsing

The front-end bias currents are determined by several DACs located in the chip periphery. In order to implement power pulsing features, current-setting DACs are duplicated. Therefore, while a DAC provides the control voltage for the nominal current in a given block, e.g. the preamplifier, another DAC generates the control voltage for a low-current mode (shutdown mode). An analog multiplexer, controlled by an external line, distributes to the pixel matrix one of the two control voltages. By doing this, the Timepix3 front-end can switch dynamically between nominal power and shutdown modes; this is commonly referred to as power pulsing. From simulations, expected power savings are in the order of a factor 7 during shutdown mode.

In the digital domain, the clock of the pixel matrix is gated in the periphery, to avoid switching losses during shutdown mode.

3 Timepix3: first measurement results

Timepix3 was submitted for production and the first samples were available at the beginning of September 2013. Five chips (without sensor) were tested so far and proved functional. First measurements are reported in this section. The results, when expressed in electrons, are calculated assuming a front-end gain of 50 mV/ke^-. The actual gain depends on the value of the feedback

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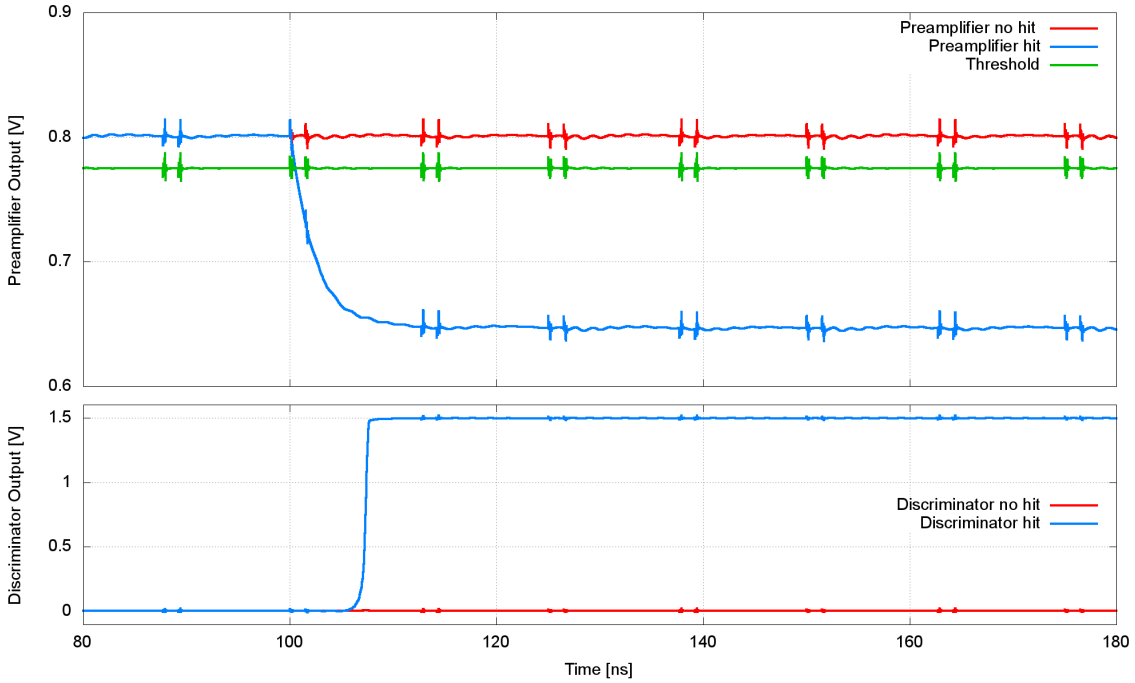

Figure 4. Simulation of noise injection from digital into analog domain. Preamplifier outputs and threshold reference line pick up noise from the digital clock. Anyhow, pick-up noise does not induce a fake hit in a non-hit pixel (red plot) nor hides the event in a pixel where real charge is injected (blue plot).

capacitor C_{fb} which is not known, yet; when an assembly with Timepix3 and a sensor is available, the gain will be measured. Meanwhile, the design value for the gain is used.

After reset, the current consumption of the chip is 450 mA for the analog domain and 370 mA for the digital, as expected from simulations.

3.1 Pixel DACs and threshold equalization

Figure 5 plots the number of events counted while scanning the threshold voltage for a single pixel. The measurement is repeated for each possible value of the 4 bit equalization DAC. Clearly, the DAC is capable of shifting the effective threshold and therefore can be used to compensate pixel-to-pixel threshold mismatches.

By computing the centroid of each Gaussian, the INL of the DAC is found to be less than ± 0.2 LSB. This very good value is consistent with design expectations.

Figure 6 shows the improvement when the full pixel matrix is equalized using the pixel DACs. Before equalization, mismatch is 19.0 LSB r.m.s. (190 e^-); after equalization it is reduced to 2.9 LSB (29 e^-). This value is well below the noise.

The FWHM of gaussians like those in figure 5 corresponds to front-end noise. Figure 7 shows the distribution of noise for the whole pixel matrix. Its average value is 5.8 LSB (58 e^-), and its standard deviation 0.28 LSB. As the minimum threshold is determined by the noisiest pixels, the worst value of 7.6 LSB (76 e^-) is used for the next calculations.

The quadratic sum of mismatch and noise yields 81 e^- r.m.s. Therefore, the 6σ minimum threshold could be set around 490 e^-.

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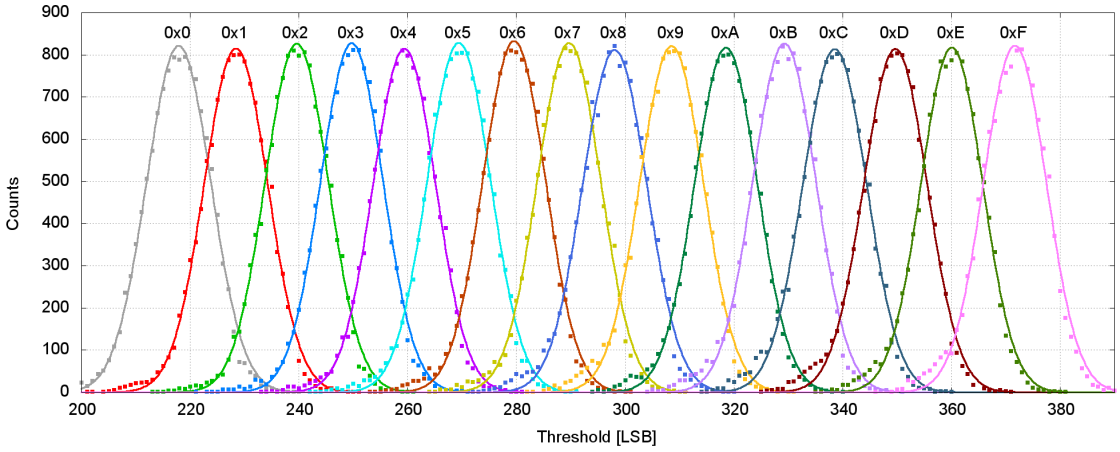

Figure 5. Threshold scan of a pixel in event counting mode for the 16 different DAC codes.

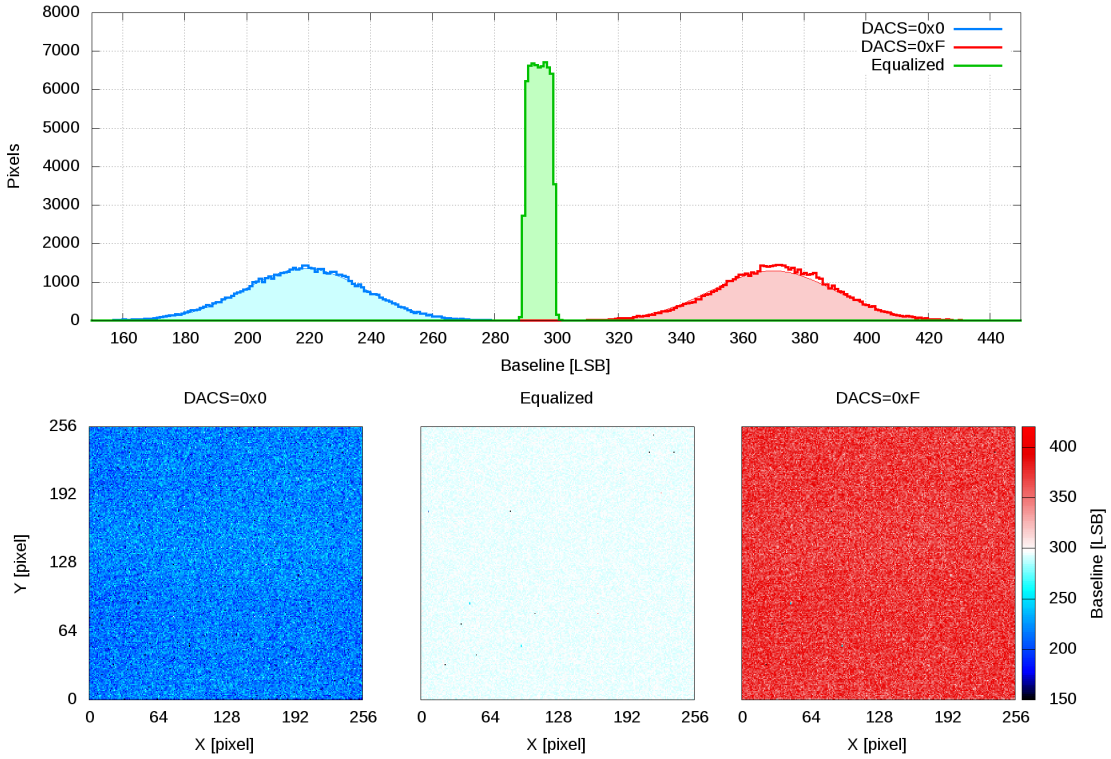

Figure 6. Using the pixel DAC, the whole matrix is equalized and a global threshold can be applied. The blue and red plots show the distribution of baselines of all 65536 pixels with the minimum and maximum DAC codes (0x0 or 0xF); the green plot shows the same distribution when each pixel is configured with its optimal DAC value.

3.2 S-curves in event counting mode

Figure 8 plots the number of events detected while doing a threshold scan for various input charges. For each value of threshold, 250 test pulses are injected by means of on-chip test capacitors which

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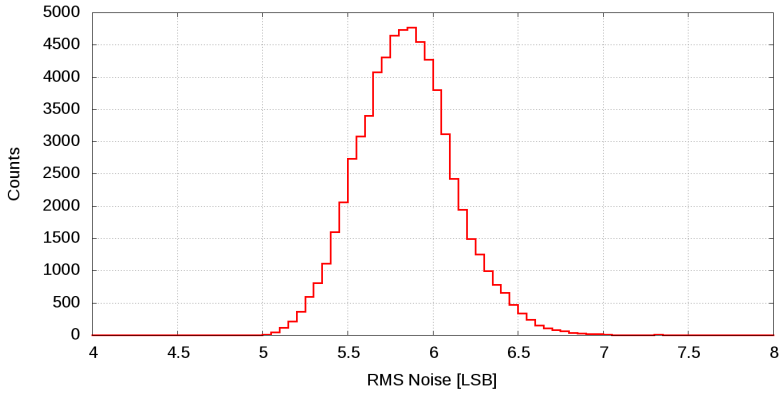

Figure 7. The distribution of noise across the pixel matrix.

are connected at the input nodes. When the threshold is very high, no event is detected. As the threshold decreases, some events are seen, and eventually all 250 pulses are detected; the transition is the S-curve, and its width is consistent with the noise measurement given in section 3.1 (5.8 LSB). When the threshold approaches baseline (around 295 LSB), noise generates many events, which rapidly fill up the digital event counter.

In this example, the flat plateau of 250 counts (especially in the green curve) shows that a threshold can be set below 500 e^-.

3.3 TOT and TOA measurement

Figure 9 shows the Time-Of-Arrival and Time-Over-Threshold for test pulses up to 18 ke^-. I_{krum} is 3 nA and the threshold is set at 500 e^-. For charges larger than 5.5 ke^-, TOA is minimum and its jitter is below 0.5 ns. Timewalk is defined as the TOA of a pulse 1 ke^- above threshold (in this case, a pulse of 1.5 ke^-); the measured timewalk is 10 ns. TOA is within 25 ns for pulses larger than 0.8 ke^-. The TOT information can be used to identify pulses smaller than this threshold. Pulses with TOT shorter than 6 counts (150 ns) can be discarded by the data acquisition system; by doing this, only pulses larger than 0.8 ke^- are accepted, whose time stamp is in the correct 25 ns clock cycle. The mismatch of the TOT slope across the full pixel matrix is 6.5 %.

4 Smallpix

The Smallpix chip is currently under study (it will also be renamed). The goals identified so far are a reduction of the pixel pitch to $\sim$40 μm, still providing simultaneous TOT and TOA measurement, and the implementation of a large array with up to 250 thousand pixels, if possible. The pixel size can be reduced with respect to Timepix3 by implementing sequential data readout rather than event-driven readout and by slightly reducing the counters' depths.

The most important feature of the chip, as foreseen today, is full Through Silicon Via compatibility. TSVs will be distributed across the pixel matrix and they will be the only connection of the chip to the outside world, carrying signals as well as power. Therefore, the chip will be tileable on all four sides, such that large area detector arrays can be built with an active area approaching 100%. To benefit from this innovation, the circuitry that is conventionally located in the

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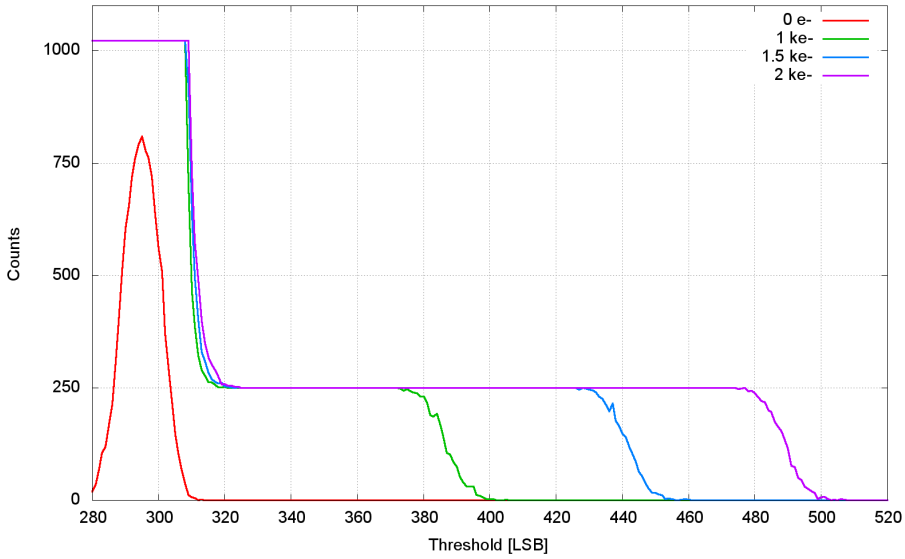

Figure 8. S-curves acquired in event counting mode, for trains of 250 test pulses with three different amplitudes. The red plot corresponds to baseline noise and is acquired with a much shorter shutter time.

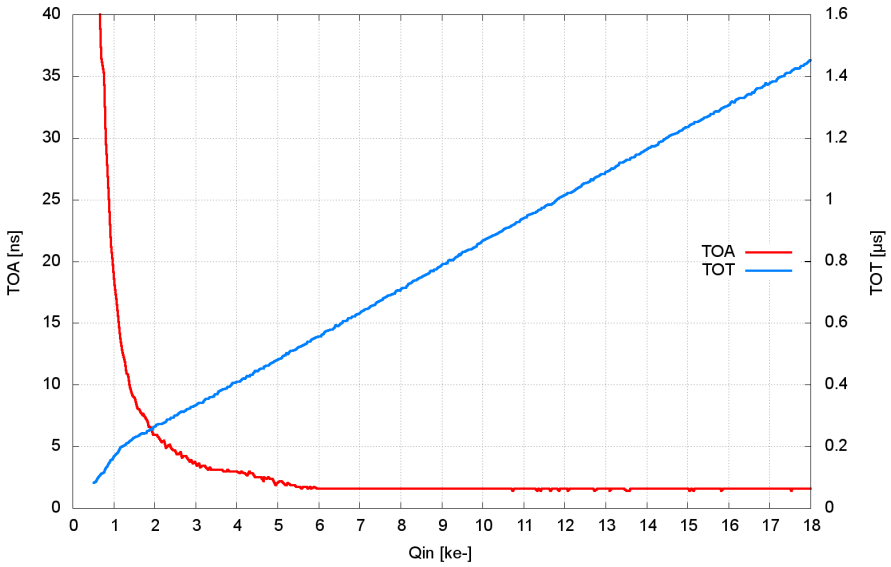

Figure 9. TOA and TOT versus input charge, averaged over 64 acquisitions.

chip periphery needs to be redistributed in the area of the pixel matrix, and therefore requires that many blocks (bandgap voltage reference, DACs, transmitters/receivers, ESD protections, etc.) be redesigned with different aspect ratios and much tighter area constraints.

Additionally, Smallpix will offer event counting and integral TOT mode, pixel- and column-based data compression and a fast OR output for triggering capability.

If the tests on Timepix3 continue giving good results, the designed analog front-end can be reused also for Smallpix, with a new layout and aspect ratio to reflect the smaller pixel size.

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Table 2. Summary of the first test results on Timepix3.

Parameter	Value
Noise	Average 58 e^- or 76 e^- in the noisiest pixels
Threshold mismatch	190 e^-
Mismatch after equalization	29 e^-
Noise + mismatch	81 e^-
Pixel DAC INL	< 0.2 LSB
TOA < 25 ns	for charges larger than 0.8 ke^-
TOA jitter < 0.5 ns	for charges larger than 5.5 ke^-
Timewalk	10 ns
TOT mismatch	6.5 %
Power consumption after reset	6.87 μA/pixel at 1.5 V supply (10.3 μW/pixel)

5 Summary

An analog front-end has been designed for hybrid pixel detectors and in particular for the Timepix3 chip. The area is only 55 μm $\times$ 13.5 μm, which makes it a very compact design in a 130 nm CMOS technology. The front-end handles input signals of both polarities and can compensate for leakage current.

The design was submitted for production. Testing activities have recently started and the first measurements, summarized in table 2, are very encouraging.

After reset, the current consumption is 6.87 μA per pixel, consistent with expectations.

Threshold adjustment DACs show very good linearity (INL < 0.2 LSB) and allow equalization of the pixel matrix. At $I_{krum} = 3$ nA, threshold mismatch is 190 e^- before equalization and 29 e^- afterwards, across the full 65 k pixels matrix. Average noise is 5.8 LSB, or 7.6 LSB in the noisiest pixels; these values correspond to 58 e^- and 76 e^-, under the assumption that the front-end gain is 50 mV/ke^-. This assumption will be verified once an assembly with a sensor is available. With these values of noise and mismatch, the minimum threshold can be set below 500 e^-.

Time-Of-Arrival and Time-Over-Threshold measurements are compatible with expectations from simulations. In particular, TOA is below 25 ns (compatible with LHC applications) for pulses larger than 0.8 ke^- and jitter matches the fast TOA resolution (1.56 ns) for pulses larger than 5.5 ke^-.

Unless some issues show up in the continuation of tests, this front-end can be reused, with a different layout aspect ratio, for the Smallpix chip, currently under study.

Acknowledgments

The authors would like to thank the colleagues at NIKHEF and at the University of Bonn for the fruitful collaboration, and in particular for the new SPIDR readout system which is used for Timepix3 testing activities.

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References

[1] Medipix webpage, http://medipix.web.cern.ch.

[2] X. Llopart et al., *Timepix , a 65k programmable pixel readout chip for arrival time, energy and/or photon counting measurements*, *Nucl. Instrum. Meth.* **A 581** (2007) 485.

[3] P. Collins, *The LHCb VELO (Vertex Locator) and the LHCb VELO upgrade*, *Nucl. Instrum. Meth.* **A 699** (2013) 160.

[4] F. Krummenacher, *Pixel detectors with local intelligence: an IC designer point of view*, *Nucl. Instrum. Meth.* **A 305** (1991) 527.

[5] F. Faccio and G. Cervelli, *Radiation Induced Edge Effects in Deep Submicron CMOS Transistors*, *IEEE Trans. Nucl. Sci.* **52** (2005) 2413.

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