VeloPix: The Pixel ASIC for the LHCb VELO Upgrade

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Outline

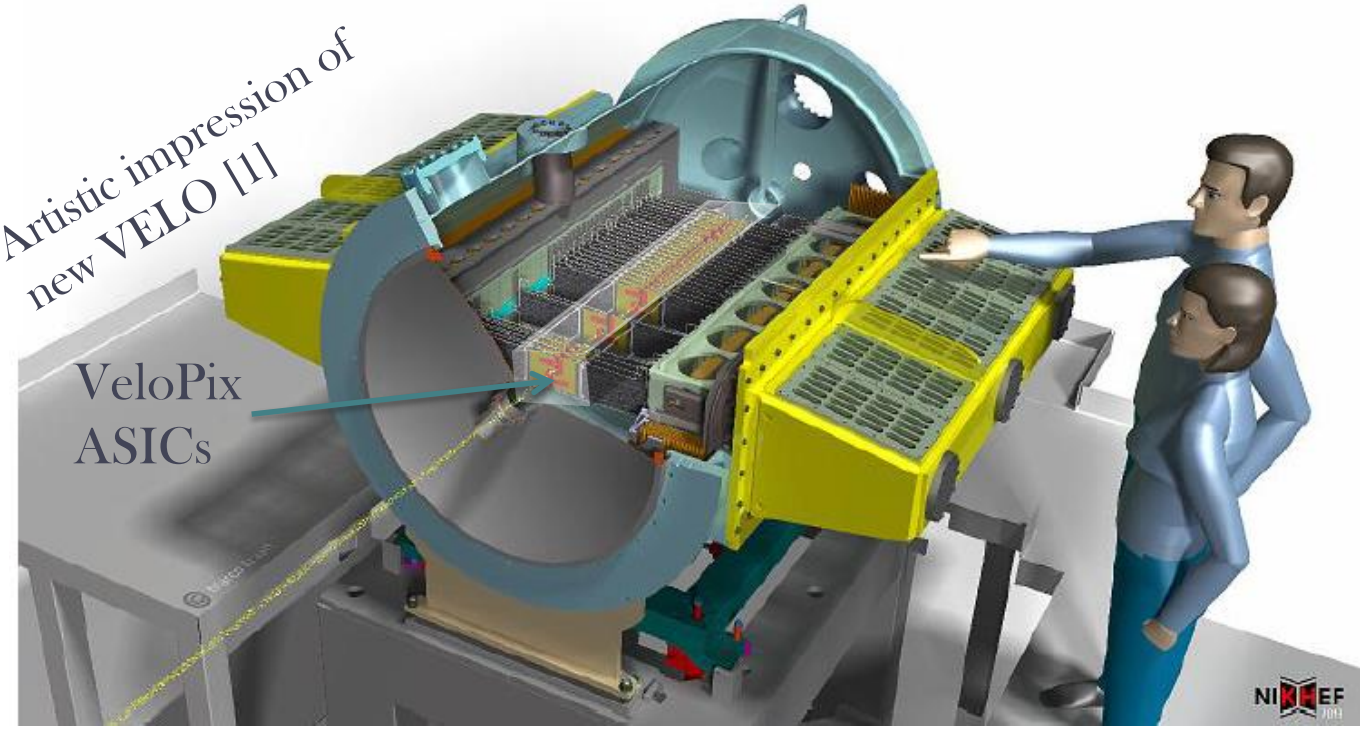
- Introduction
- VeloPix vs Timepix3
- Readout Architecture
- GWT Serializer
- Summary

Introduction

- VeloPix: Hybrid pixel detector Readout ASIC for the LHCb VELO upgrade
- The ASIC reads out all bunch crossings at 40 MHz

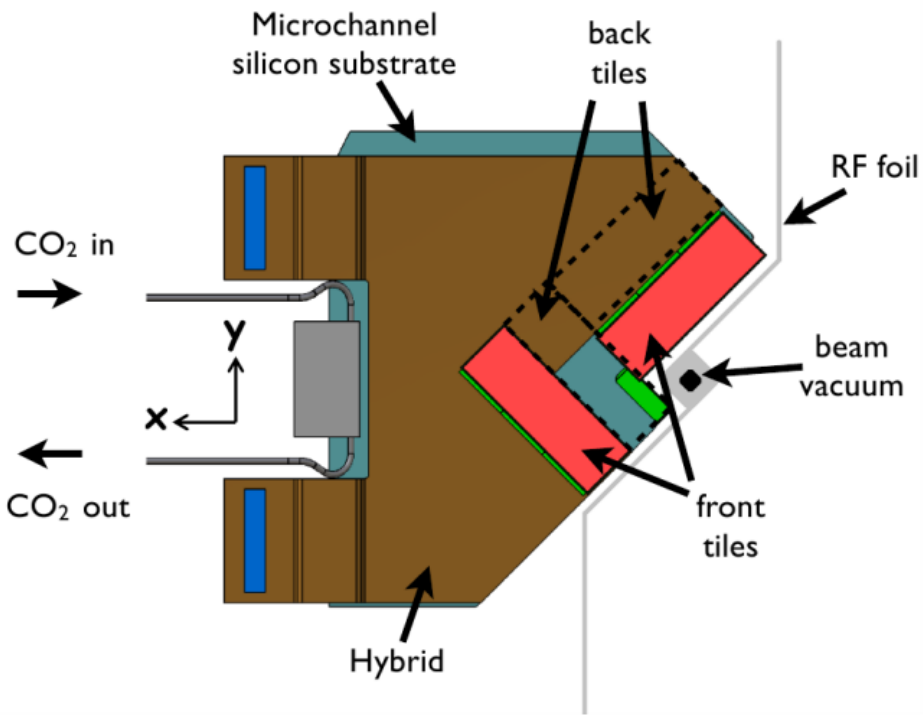
The VELO upgrade:

- Approx. 2.85 Tbit/s
- 26 module pairs
- 624 ASICs
- 41 Mpixels

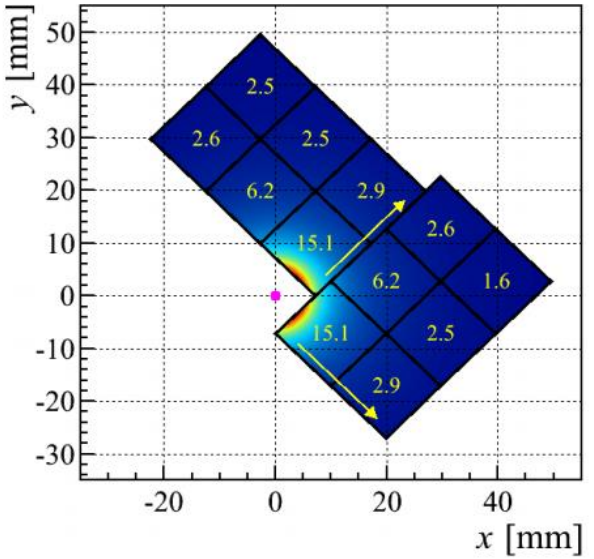


VeloPix ASIC module (12 ASICs)

Module of 12 VeloPix ASICs [1]:



Track rates for module [2]:



Data rate [Gbit/s] for hottest module.

Highly non-uniform radiation dose:
8×10^{15} to 2×10^{14} n_{eq}/cm^2

Peak rates:
Hottest chip 15.1 Gbits/s
hottest module: 61.2 Gbits/s

See Sophie Richards' overview of the VELO upgrade: "LHCb VELO Upgrade"

VeloPix ASIC specifications

Feature	VeloPix	Timepix3 [2]
Readout type	Continuous, trigger-less, binary	Continuous, trigger-less, ToT
Timing resolution/range	25 ns, 9 bits	1.5625 ns, 18 bits
Power consumption	< 1.5 W cm^{-2}	< 1.0 W cm^{-2}
Pixel matrix, pixel size	256 x 256, 55 um x 55 um	256 x 256, 55 um x 55 um
Radiation hardness	400 Mrad, SEU tolerant	-
Peak hit rate	900 Mhits/s/ASIC 50 khits/s/pixel	80 Mhits/s/ASIC 1.2 khits/s/pixel
Sensor type	Planar silicon, e- collection	Various, e- and h+ collection
Max. data rate	20.48 Gbps	5.12 Gbps
Technology	130 nm CMOS	130 nm CMOS

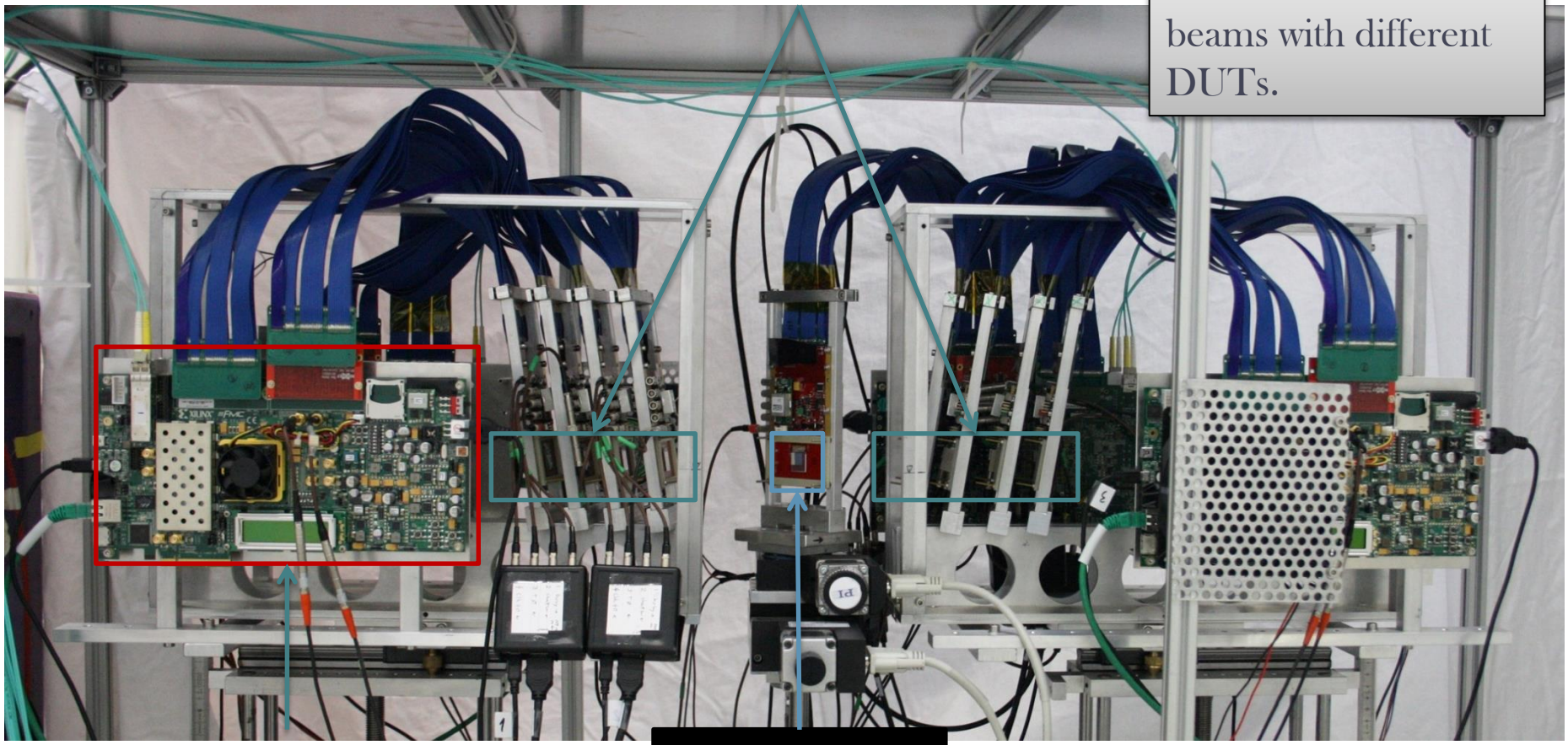
> x 10

x 4

Timepix3 Test Beams

8x Timepix3 telescope

Several successful test beams with different DUTs.



SPIDR readout

Timepix3 DUT

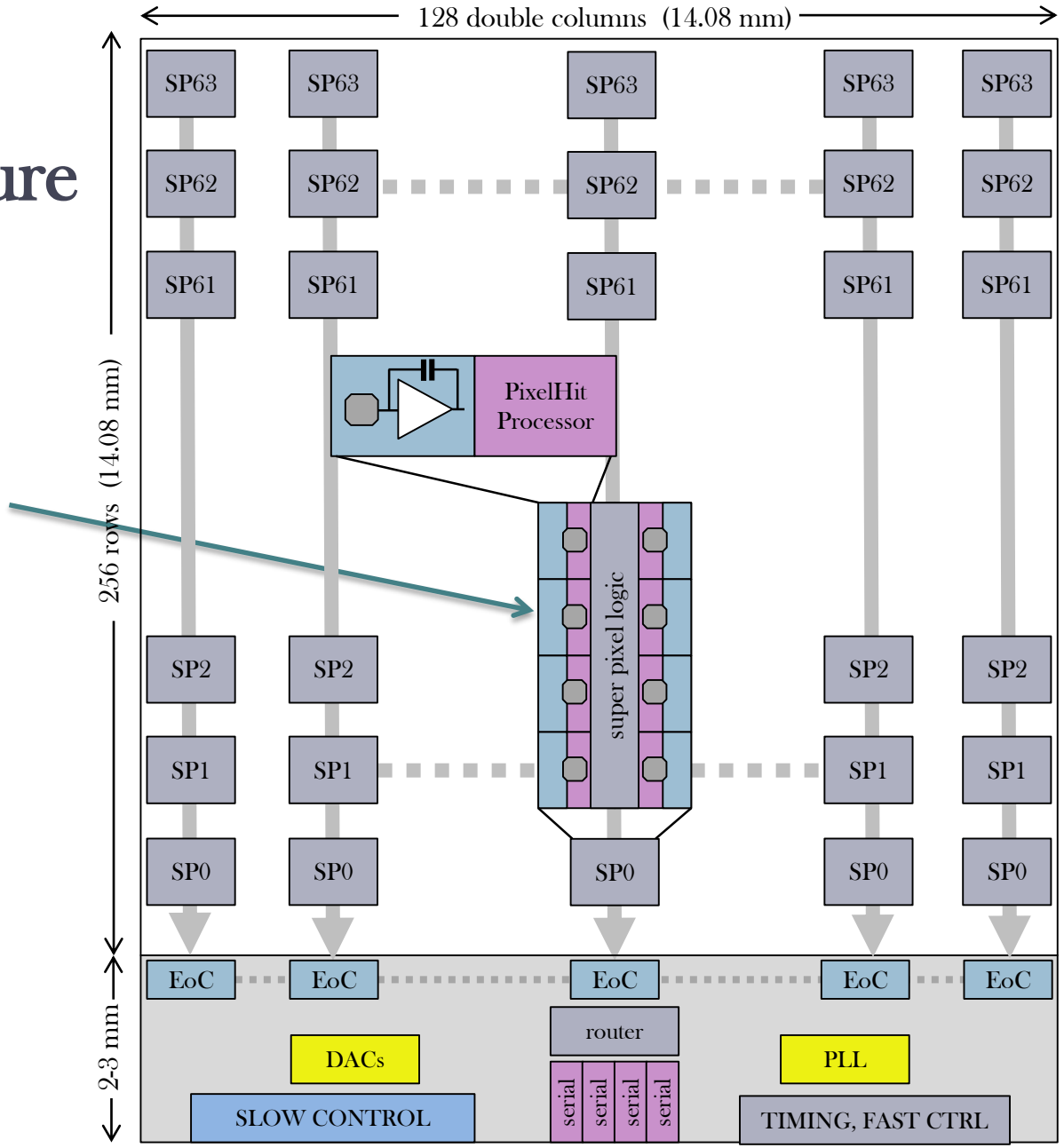
Mechanics: CERN

See [4] for more about Timepix3.

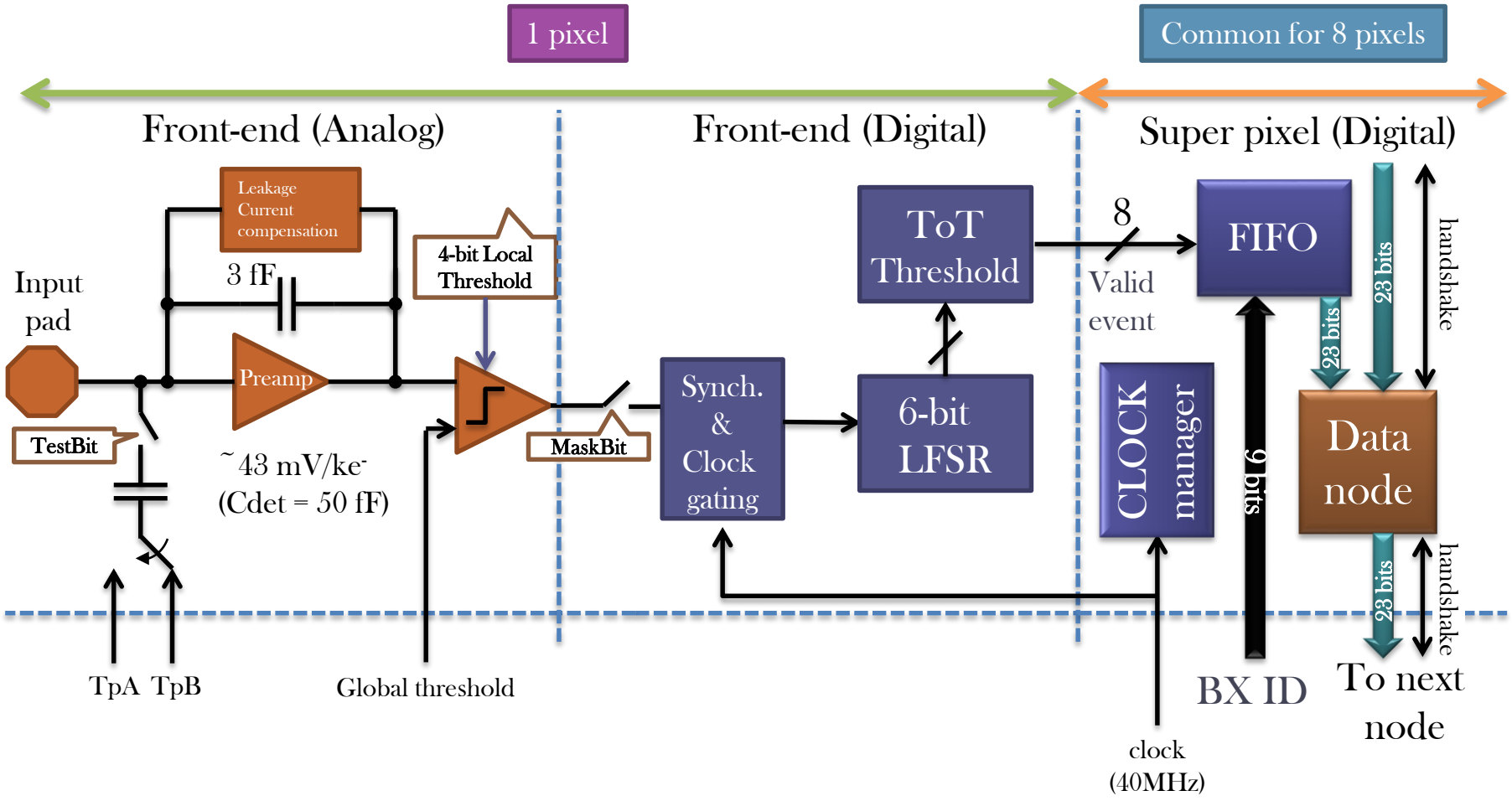
VeloPix Architecture

Super pixel:

- 2x4 pixels to reduce the data rates
- 30% reduction vs. single-pixel

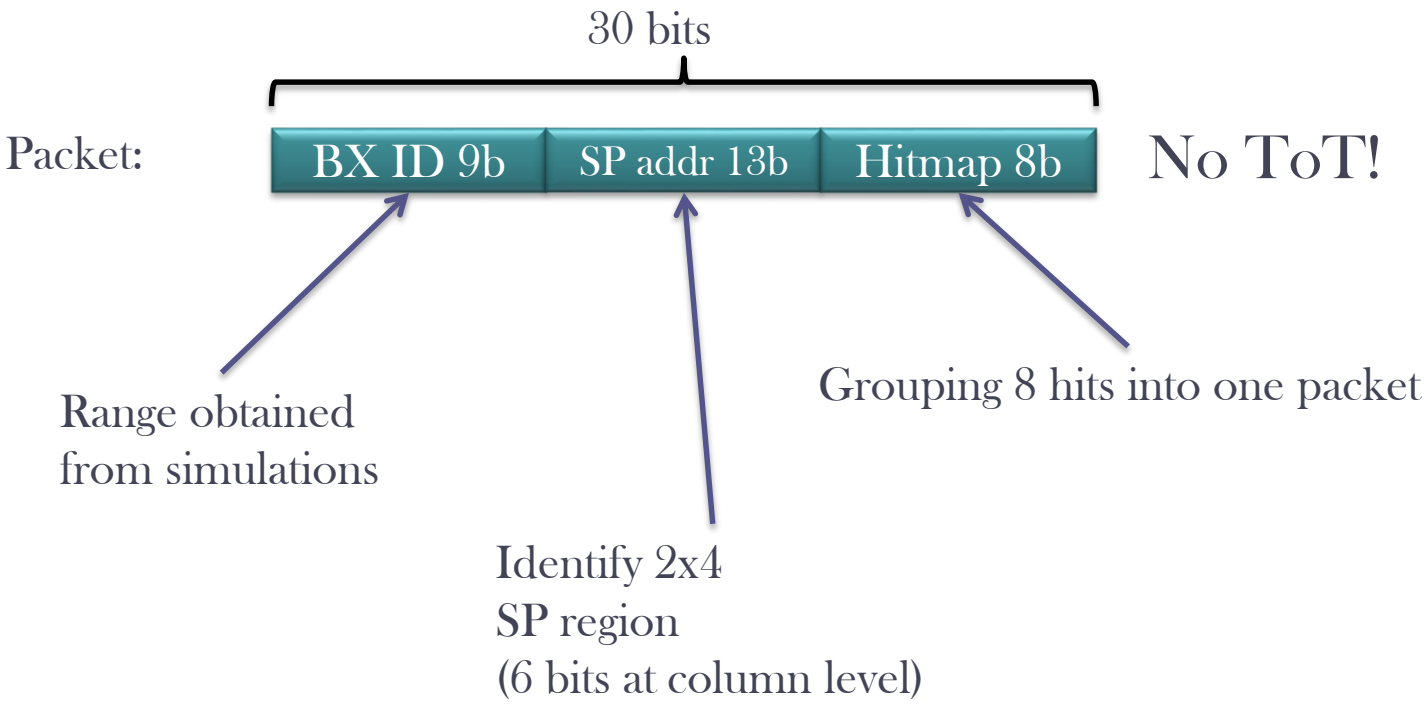


VeloPix Pixel Schematic



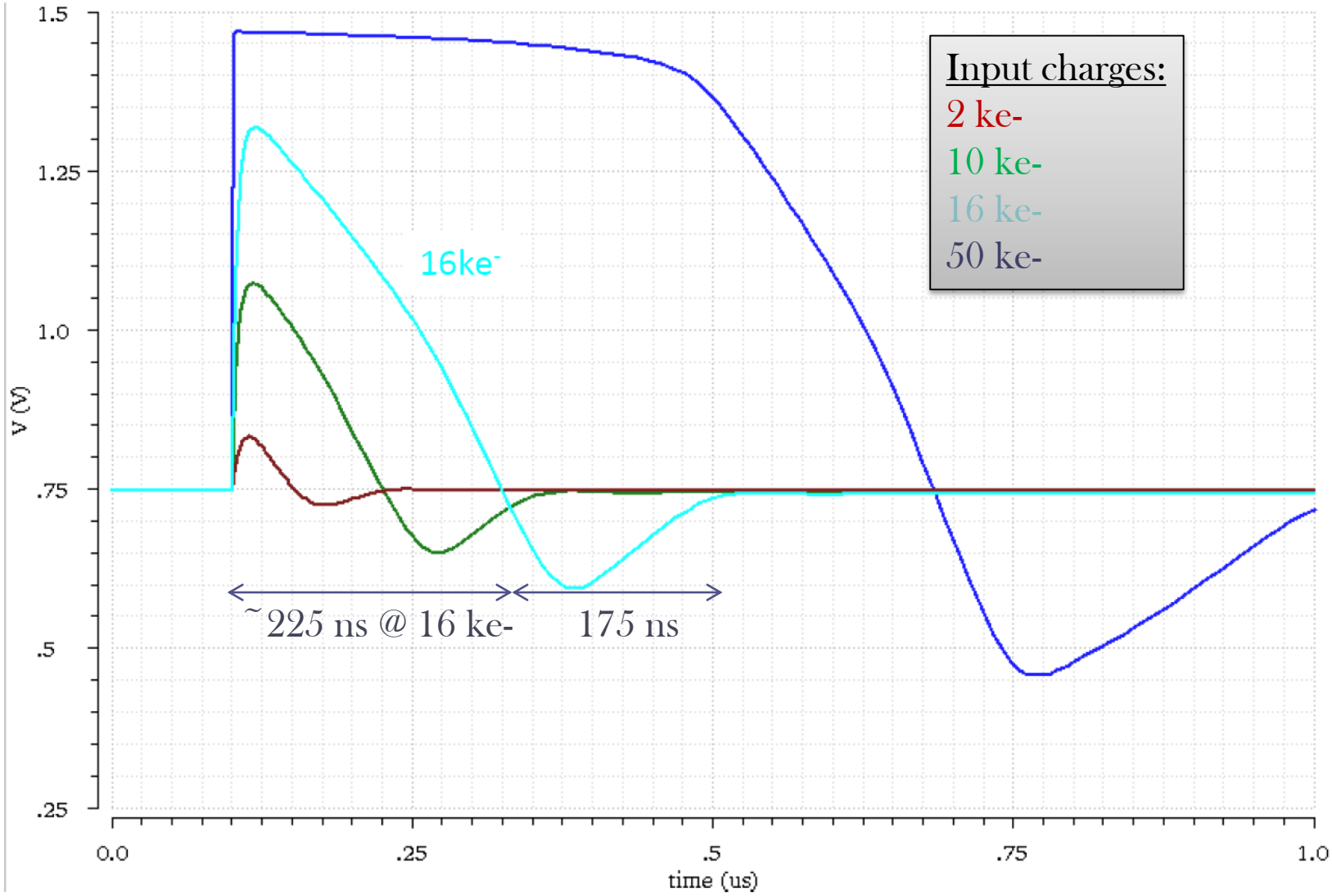
Packet Format

30% data reduction from sharing the BX ID and super pixel address among multiple pixels.



BX ID = bunch crossing ID/ time stamp/time-of-arrival

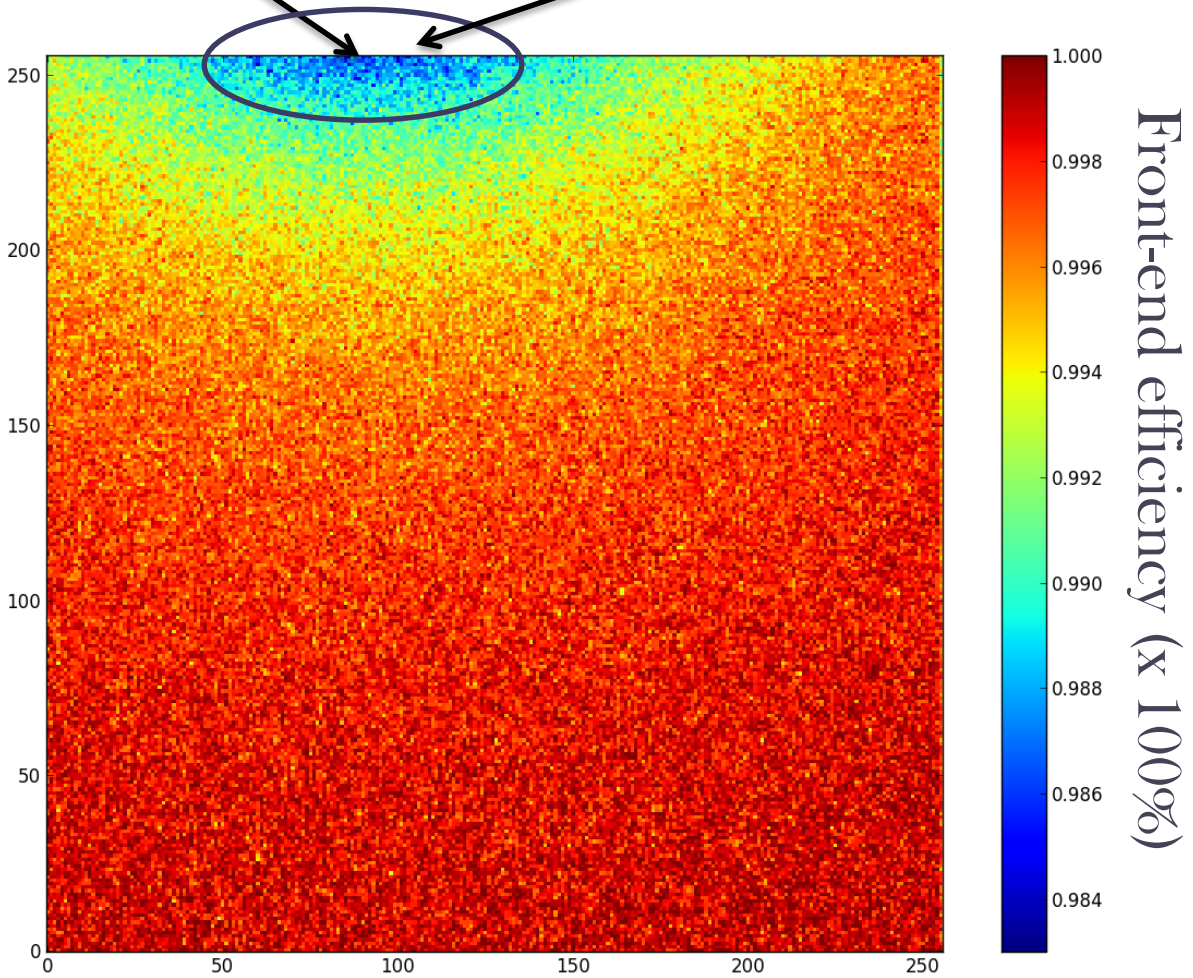
Analog Front-End Amplifier Response



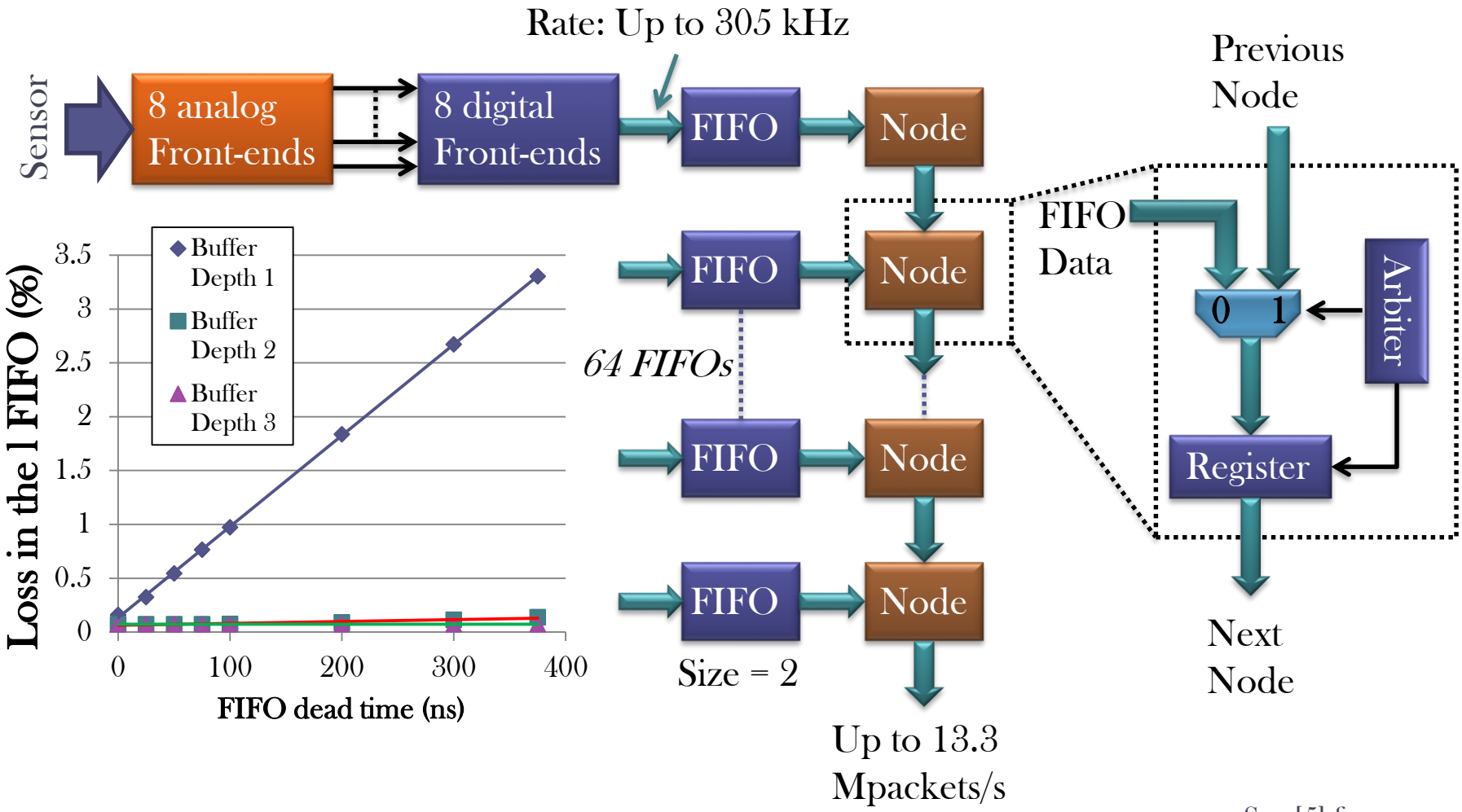
Analog Front-End Pile-Up

Up to 1.6% losses

Rates up to 50 kHz per pixel



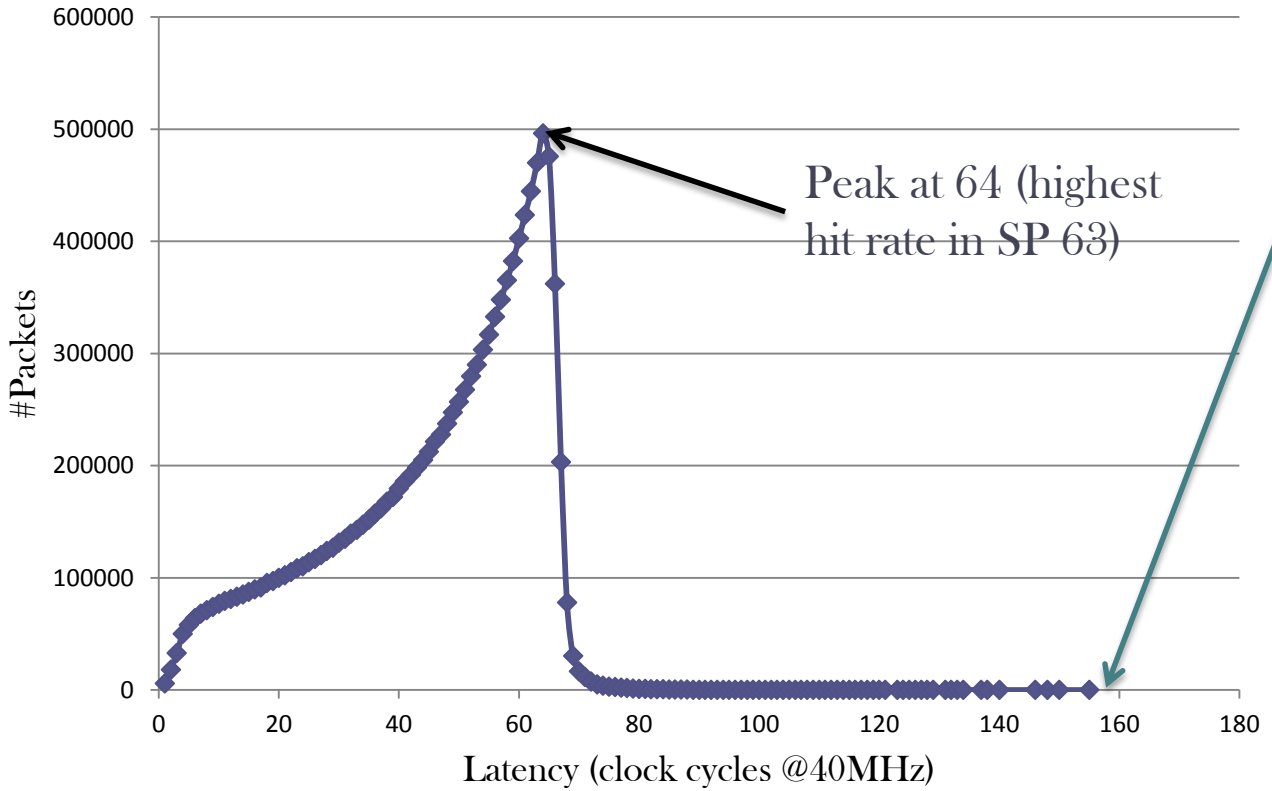
Double Column Architecture



See [5] for more details.

Simulation: Latency & BX ID Length

Trigger-less architecture:
Latency must be < BX ID range. Otherwise ambiguities in BX identification.

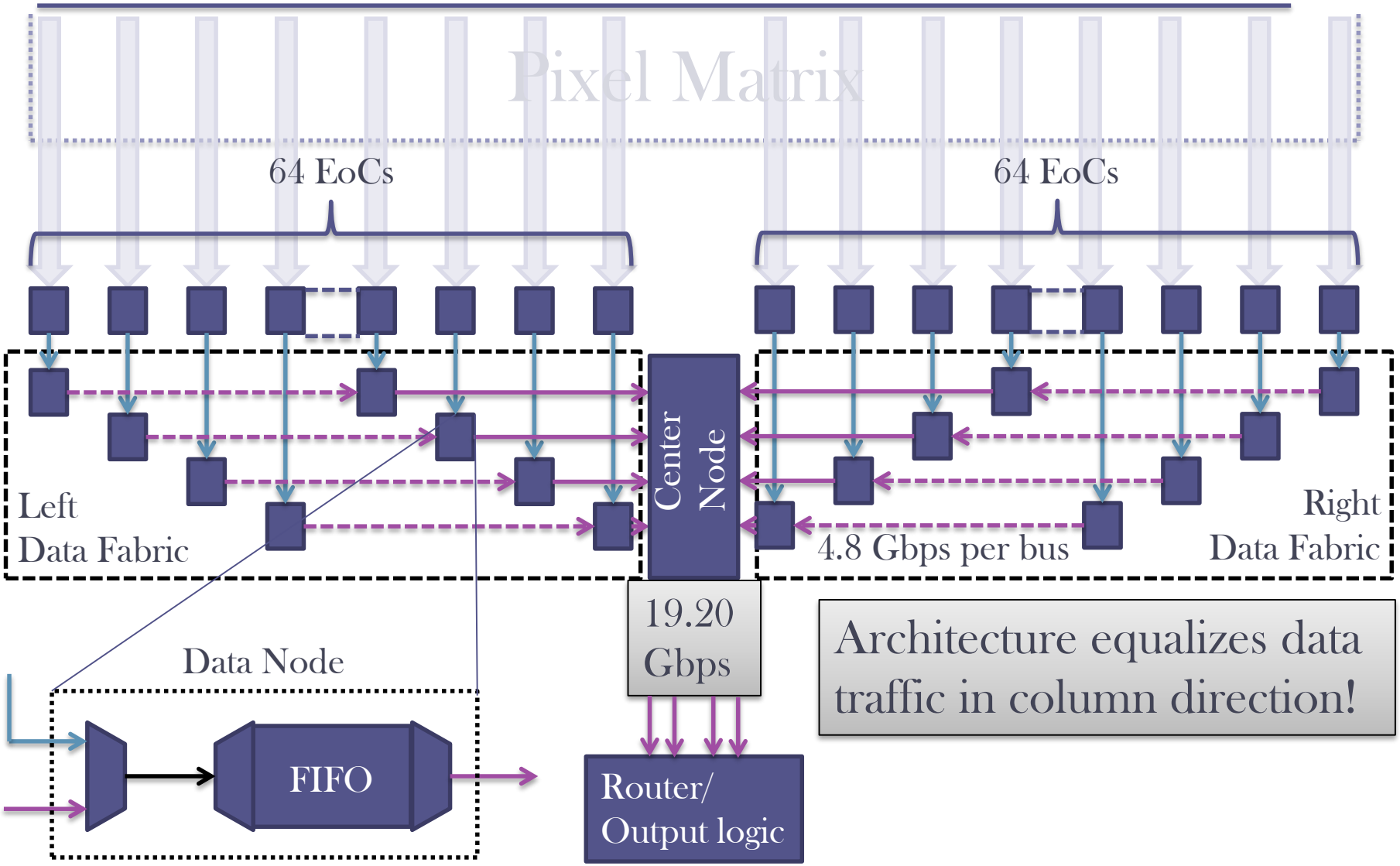


9-bit BX ID (512 clocks) sufficient!

Simulation results:
Efficiency: 99.99%*
Hit rate: 840 Mhits/s
Packet rate: 505 M/s
Data rate: 16.2 Gbps
Hits per packet: 1.66

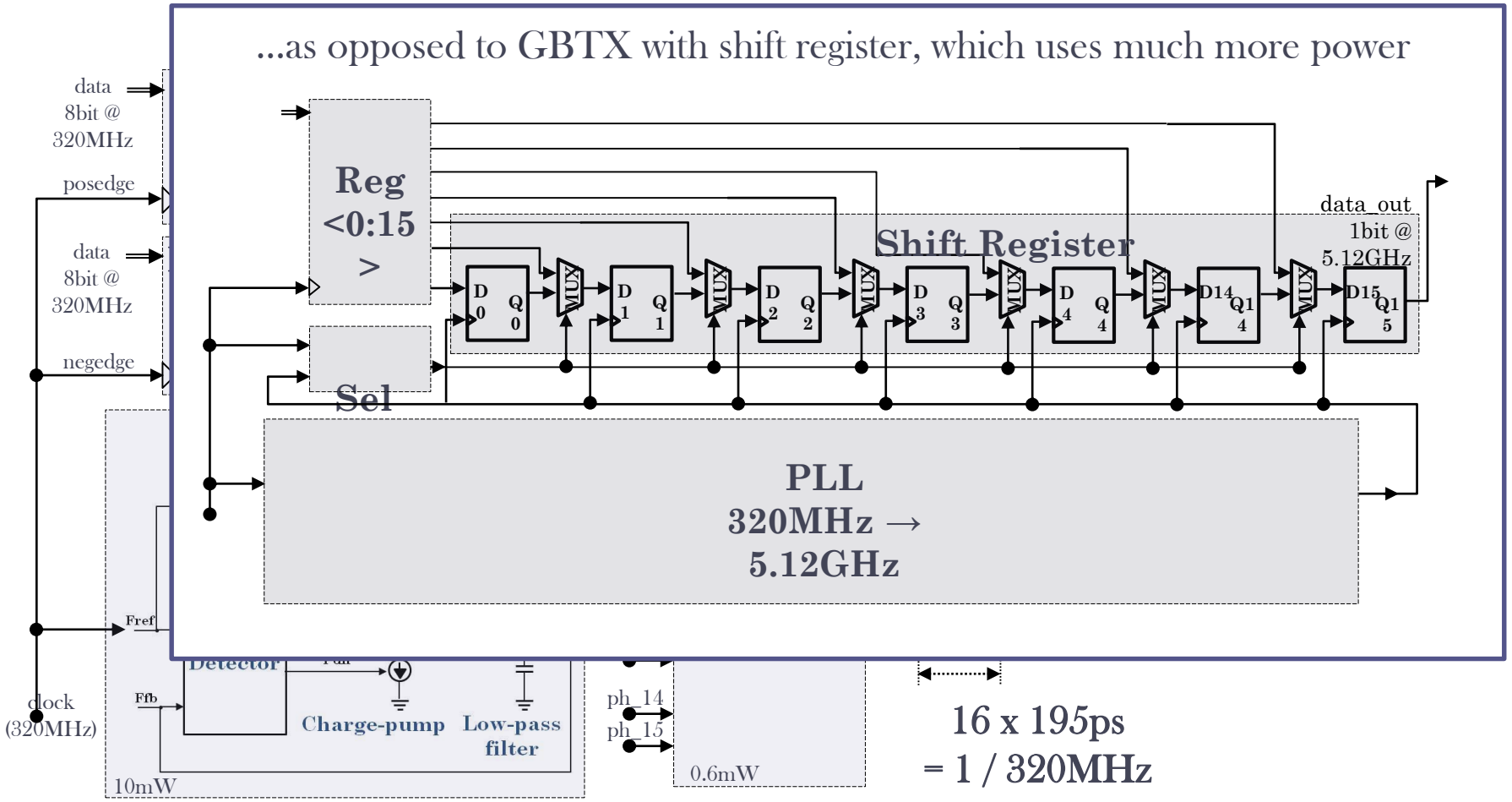
*No analog pile-up included.

End-of-Column (EoC) Data Fabric

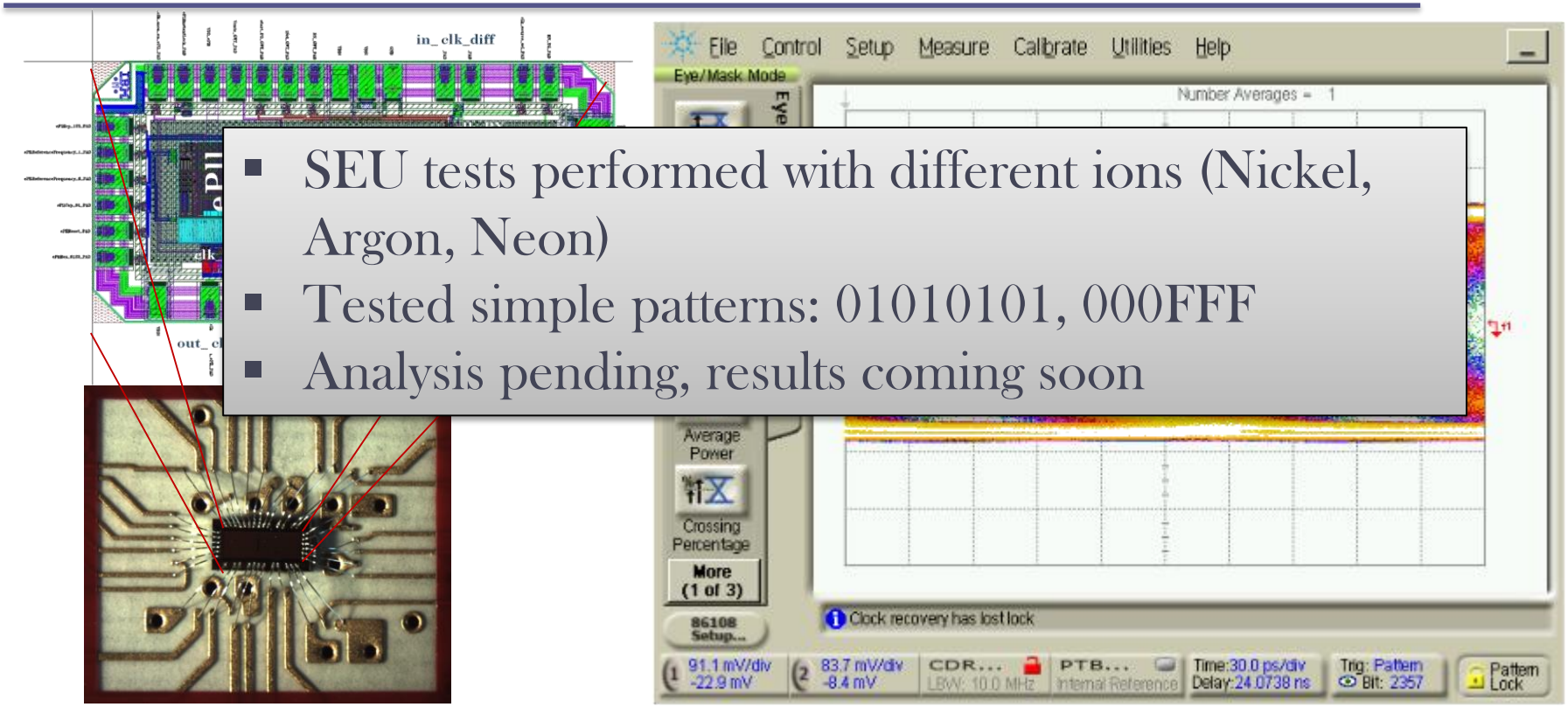


Architecture equalizes data traffic in column direction!

GWT : a 60-mW 5.12 Gbps Serializer/Transmitter



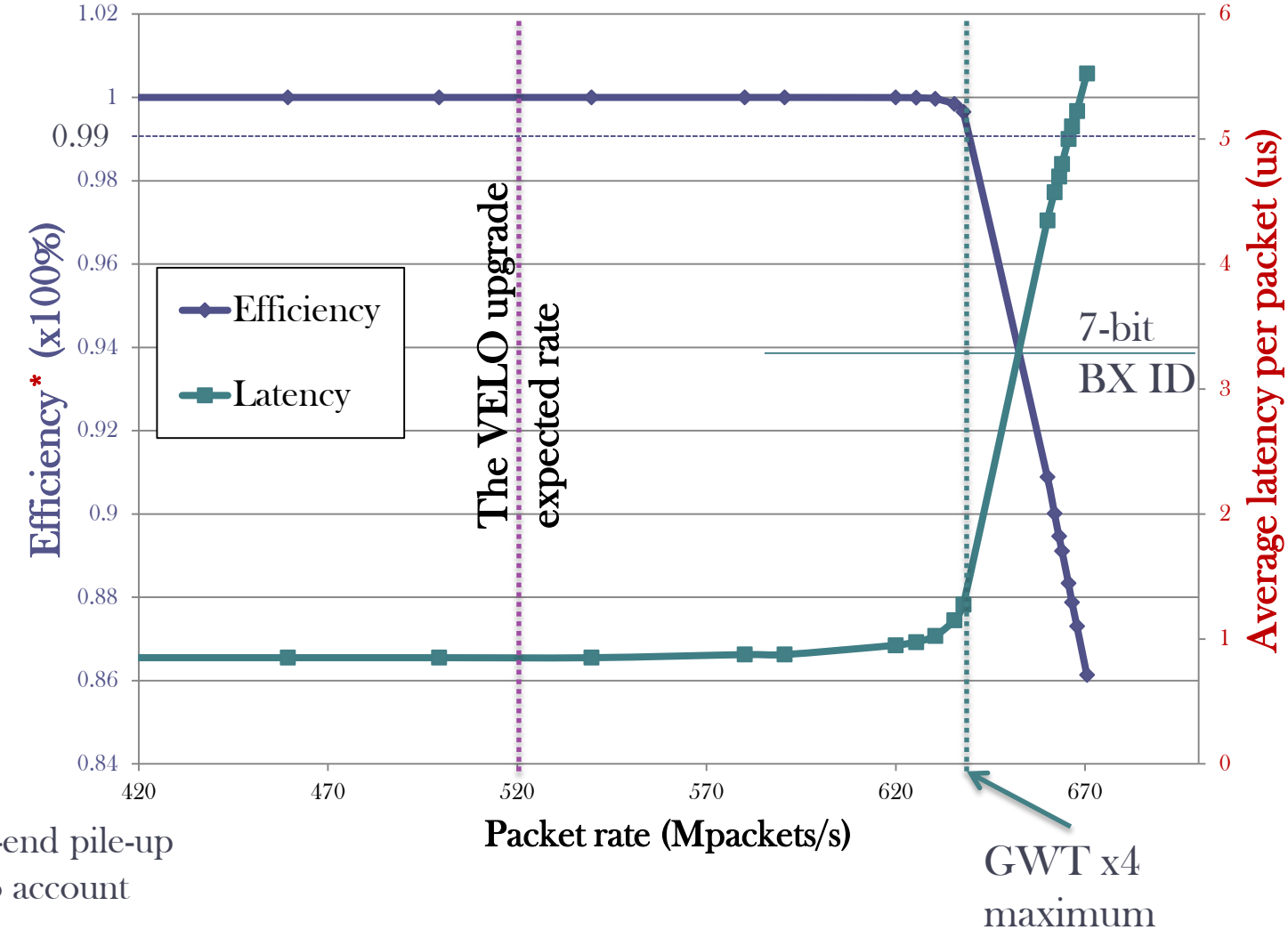
Velo_GWT Test Chip in 130nm CMOS Technology



- SEU tests performed with different ions (Nickel, Argon, Neon)
- Tested simple patterns: 01010101, 000FFF
- Analysis pending, results coming soon

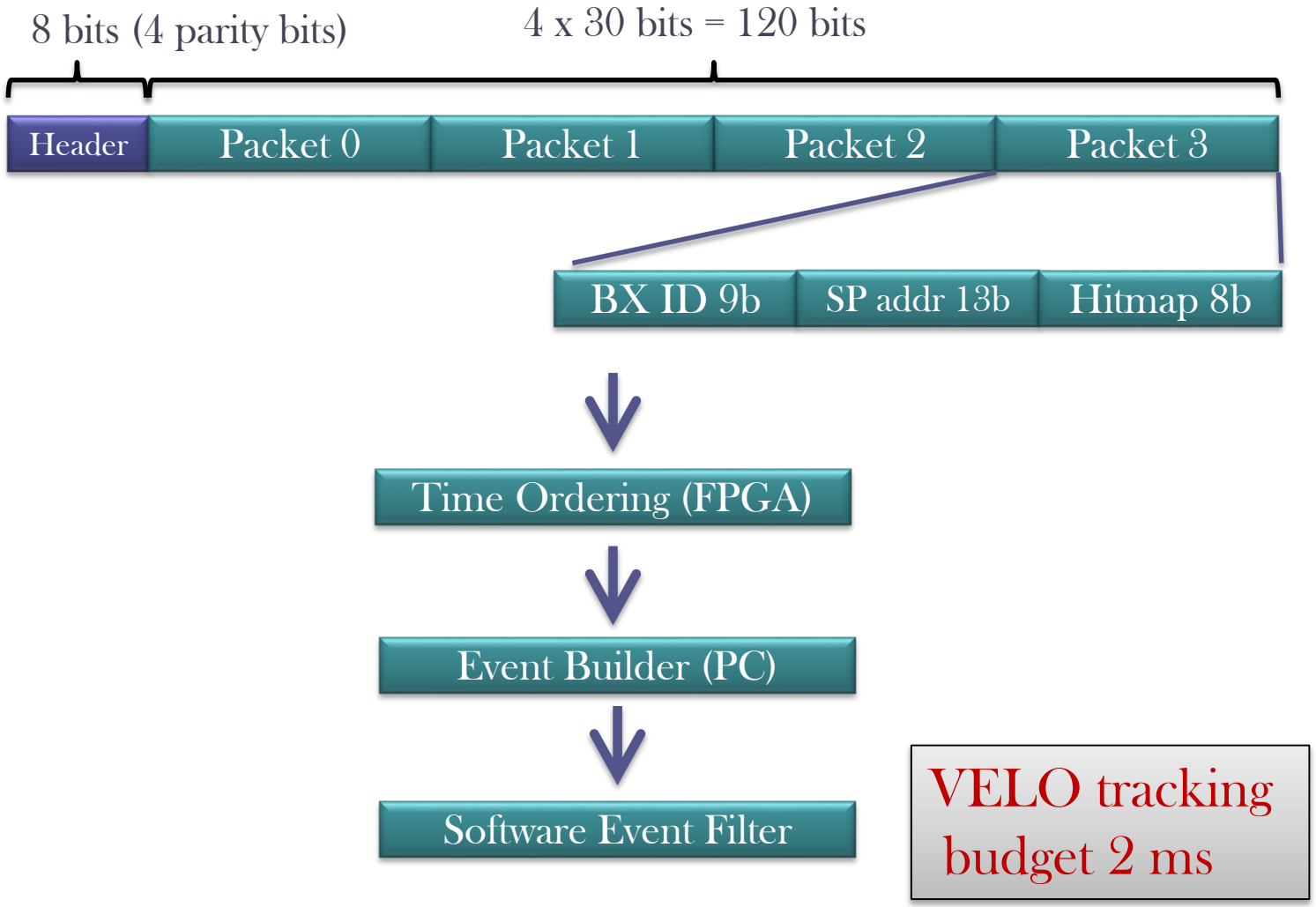
- 1 mm x 2 mm test chip in 130 nm CMOS technology
- Power : 5.12 Gbps serializer: 15 mW, wireline driver: 45 mW
- Eye diagram: +/- 200 mV is 60 ps (pseudo-random pattern)

Simulation: Data transfer efficiency



*no front-end pile-up taken into account

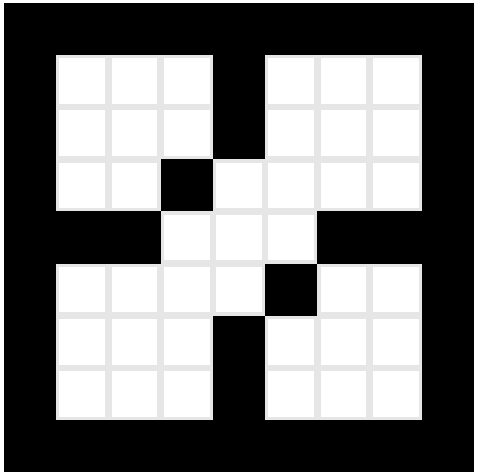
Downstream Data Flow



Diversion: Pixel Clustering

- Clustering on CPU was deemed too slow.
- FPGA implementation *very* complex.
- In fact, CPU clustering is feasible:
  - Algorithm well known in graphics applications.
  - Optimize for isolated Super Pixels flagged by FPGA.

8-way flood fill algorithm as commonly used in computer graphics applications. [6]

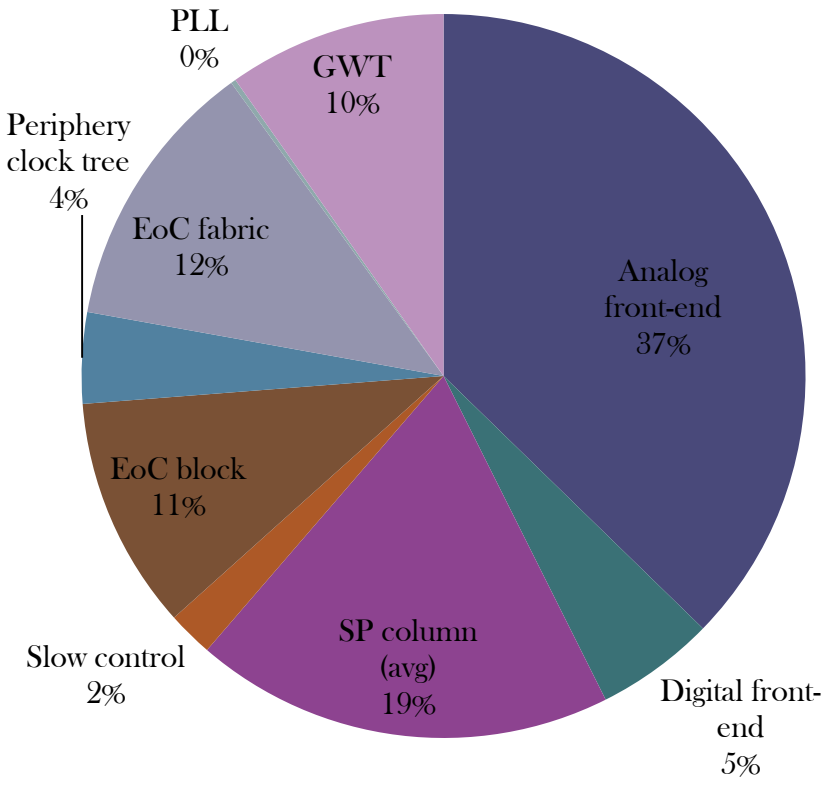


About 10% of VELO tracking

Power Consumption

Block	P (mw)	#Blocks	Total power
Analog front-end	0.014	65536	917.5
Digital front-end	0.002	65536	131.1
SP column (avg)	3.6	128	460.8
Slow control	*50*	*1*	*50 **
EoC block	*2*	*128*	*256 **
Periphery clock tree	*100*	*1*	*100 **
EoC fabric	*300*	*1*	*300 **
PLL	*5.5*	*1*	*5.5 **
GWT	60	4	240
		Total (mW):	2460.9
		W/cm^2	**1.09**

* estimated/budgeted



Summary

- Trigger-less readout ASIC architecture
- Design driven by rate and power requirements
  - Reads out > 900 Mhits/s/ASIC
  - consuming < 1.5 W/cm^2
- VeloPix builds on expertise learned during the Timepix3 design
- GWT serializer (5.12Gbps/60mW) demonstrated to work, SEU tests to be analyzed

References

[1] LHCb VELO Upgrade TDR. CERN LHCC 2013-021. 2013.
[2] L. Eklund, “The LHCb VELO Upgrade”, ICHEP 2014
[3] T. Poikela. “Design and Verification of Digital Architecture of 65K Pixel Readout Chip for High-Energy Physics.”, 2010.
[4] T. Poikela et al. “Timepix3: a 65K channel hybrid pixel readout chip with simultaneous ToA/ToT and sparse readout”, 2014
[5] T. Poikela et al. “Digital column readout architectures for hybrid pixel detector readout chips“, 2014.
[6] "Recursive Flood Fill 8 (aka)" by André Karwath aka Aka - Own work. Licensed under CC BY-SA 2.5 via Wikimedia Commons - http://commons.wikimedia.org/wiki/File:Recursive_Flood_Fill_8_(aka).gif#/media/File:Recursive_Flood_Fill_8_(aka).gif

Why 2x4 super pixel?

Table: Data rates for different super pixel dimensions:

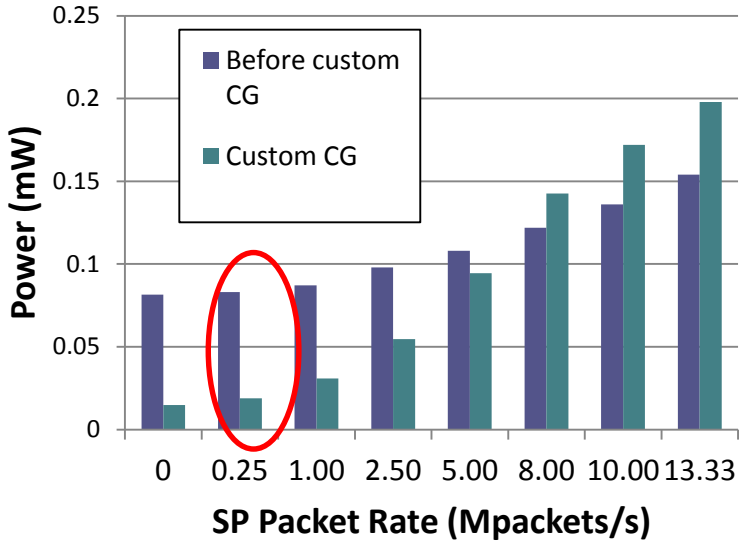
Binary encoded packets (no ToT)			
Super Pixel Geometry	**Data rate (Gbps)**	**Packet size (#bits)**	**Reduction (%)**
256 x 256	14.785	28 + N x 16	38.179
4 x 4	16.477	28 + N x 4	31.105
2 x 4	16.806	28 + N x 3	29.729
2 x 4	16.945	33	29.148
1 x 4	17.758	30	25.748
2 x 2	17.857	30	25.335
1 x 4	18.283	28 + N x 2	23.553
2 x 2	18.373	28 + N x 2	23.177
4 x 4	18.661	40	21.973
1 x 2	19.703	29	17.616
1 x 2	19.878	28 + N x 1	16.884
	23.916	28	0.000

Chosen format

No super pixel grouping

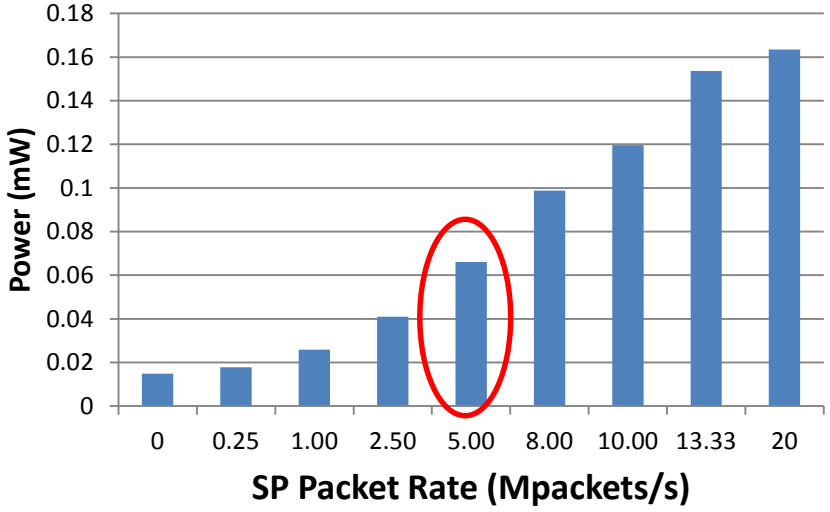
N = number of pixel hits in a packet

Super Pixel Power Estimation



Power for SP hitmap buffers:

- Target rate approx. 300 kHz
- Power approx. 20 uW
- Hand-crafted clock gating (CG) works!



Power for transporting the packets:

- Target rate 5 MHz
- Power 66 uW

128 x 64 = 8192 Super pixels per chip!!