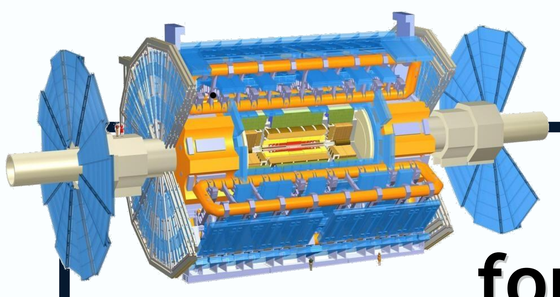

The Serial Link Processor for the Fast TracKer (FTK) processor at ATLAS

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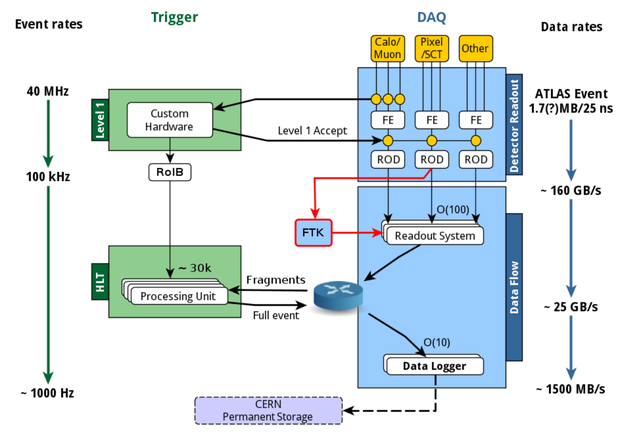
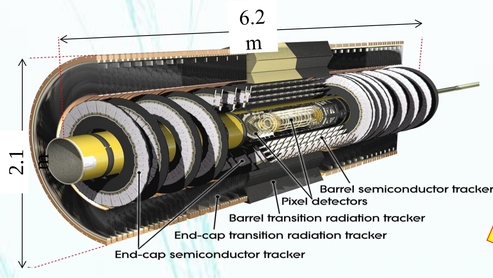
The FTK in the ATLAS Trigger System

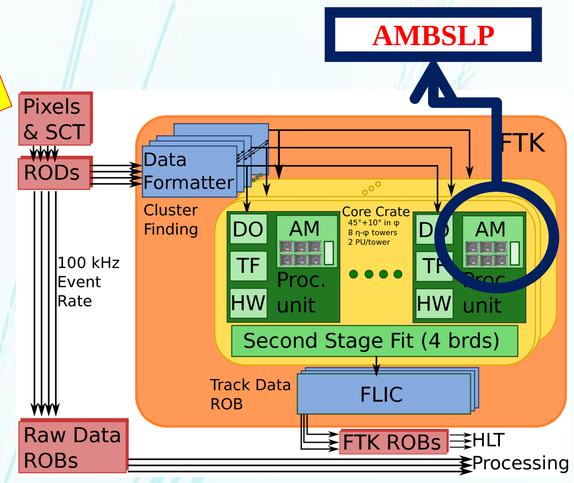
- ATLAS is one of the four experiments that operates along the Large Hadron Collider.
- Due to the large amount of data (2 MB/25ns, 40 MHz event rate) coming from the ATLAS detector, it is mandatory to implement an online event selection system (i.e. Trigger system).
- The ATLAS trigger chain is divided into two subsequent steps;
  - Level 1, based on custom hardware, reduces the event rate to ~100 KHz, within 2.5 μs latency;
  - High Level Trigger (HLT), software based, reduces it further to ~1 KHz;
- Track information is mandatory to stay inside the available bandwidth.
- FTK operates after each Level 1 trigger accept performing full track reconstruction for $|\eta|<2.5$, $P_T>1$ GeV within a latency of 100 μs.



FTK system architecture



- Inner Detector: ~100 million channels of silicon pixel and strip (SCT) detectors and straw drift tubes
- FTK uses pixel and SCT hit information to infer charged particle tracks
- The FTK system receives a copy of data from silicon detectors Read-Out Drivers (RODs)
- ID data are distributed in 64 partially overlapping towers. Each tower identifies a region $|\Delta\eta \times \Delta\varphi| \sim 1.2 \times 30°$.
- Each towers is composed by 8 independent processing pipelines.

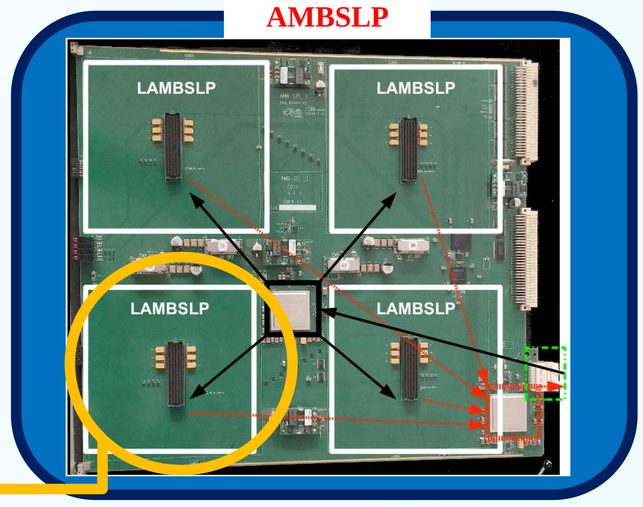


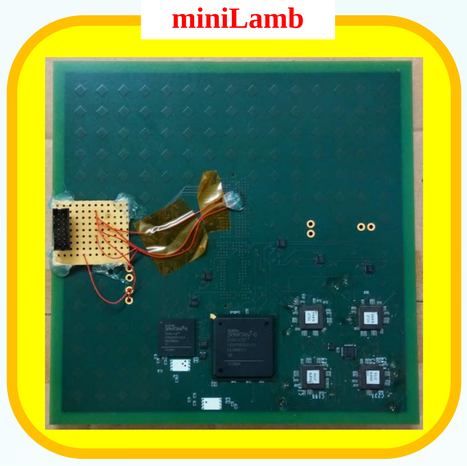
Pattern Recognition using Associative Memory (AM)

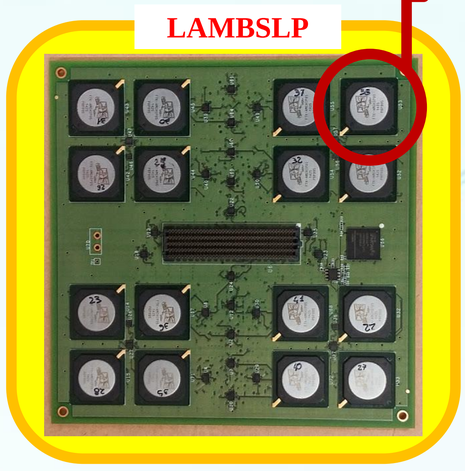
FTK performs the pattern matching using a large bank of pre-computed coarse resolution track trajectories (patterns).
This step is extremely fast thanks to the computational power of the Associative Memory (AM) chip, a dedicated VLSI chip.

The picture shows the last prototype of the AM chip named AMchip05

The AMBSLP and LAMBSLP

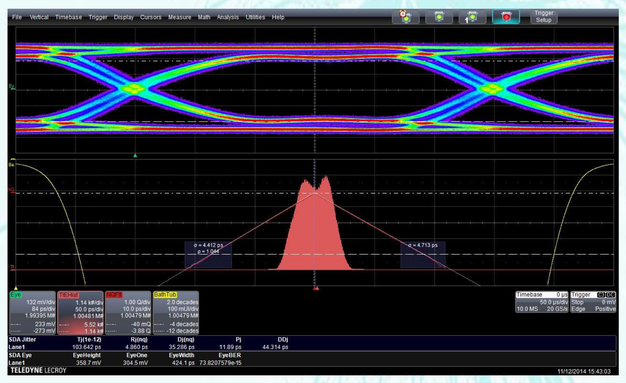






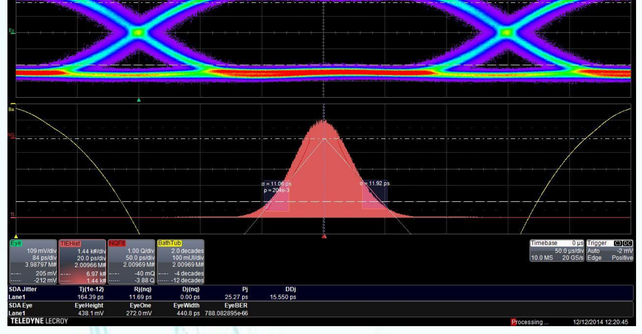
- **The AMBoard (AMBSLP) is a 9U VME board on which 4** mezzanines hosting the AM chips **(LocalAMBSLPS or LAMBSLP) are mounted** . The suffix SLP stands for Serial Link Processor indicating the usage of serial links.
- Two different LAMBSLP designs (miniLamb and LAMBSLP) are used to lodge AM chip prototypes with different footprints (respectively mini@sic with QFN64 and Amchip05 with HS BGA 529).
- FPGAs (squares on AMBSLP photo) and AM chips (circle on LAMBSLP photo) on the boards inter-communicate through LVDS couples (as shown by arrows in the photo). Data are transmitted serially with 8b/10b encoding of 32-Bits data words.
- The main goals of the AM system are:
  - lodge the AM chips;
  - handle the high data rate and the input fan-out required by parallel pattern matching;
  - fed power to the used electronics.
- Latest versions of those boards are provided with an extremely powerful network of 828 2 Gbit/s serial links, giving a **total I/O rate of 56 Gbit/s.**
- The final version of the system will lodge 64 AMchip06 per board. Each chip has an expected power consumption of 3W/chip, **giving total 250 W/board**.

Serial Link quality

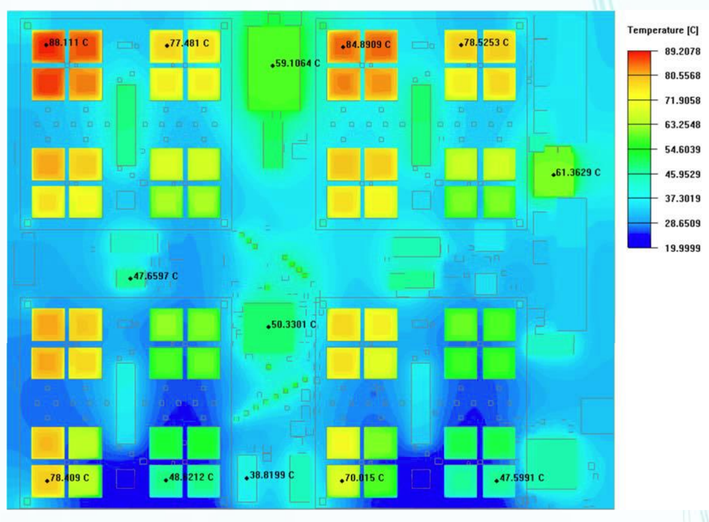


- We show quality measurements on the seiral link of the presented prototypes
- We use Low Voltage Differential **(LVDS) couples with 8b/10b encoding** of data.
- **No error recovery** available.
- Need **of ultra-low Bit Error Rate**.
- **About 200 serial links on each LAMBSLP and 76 serial links on the AMBSLP (max length 60 cm).**
- Possible cross talk issues prompted us to the usage of guard lines connected to ground.

- Additional shielding of planes dedicated to routing with ground planes.
- Need of good simulation of line impedance during design phase.
- Accurate measurement of Bit Error Rate (BER):
  - **Oscilloscope-evaluated BER** ranges between 7 10^{-14} and **10^{-100}**;
  - **Measured upper limit on BER < 10^{-13}**. No error were detected, this measure is limited by the number of transmitted bits.



Cooling studies



- Due to the large required power, cooling capabilities are crucial;
- Thermal simulation of the boards inside the crate accounts for:
  - Position of electronic components;
  - Internal structure of AM chips;
  - Expected airflow.
- Suggested change to optimise cooling distribution:
  - Change in position of DC-DC converters to speed up airflow;
  - Custom fan trays to have enough cooling power.

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