gFEX

the ATLAS Calorimeter Trigger Global Feature Extractor

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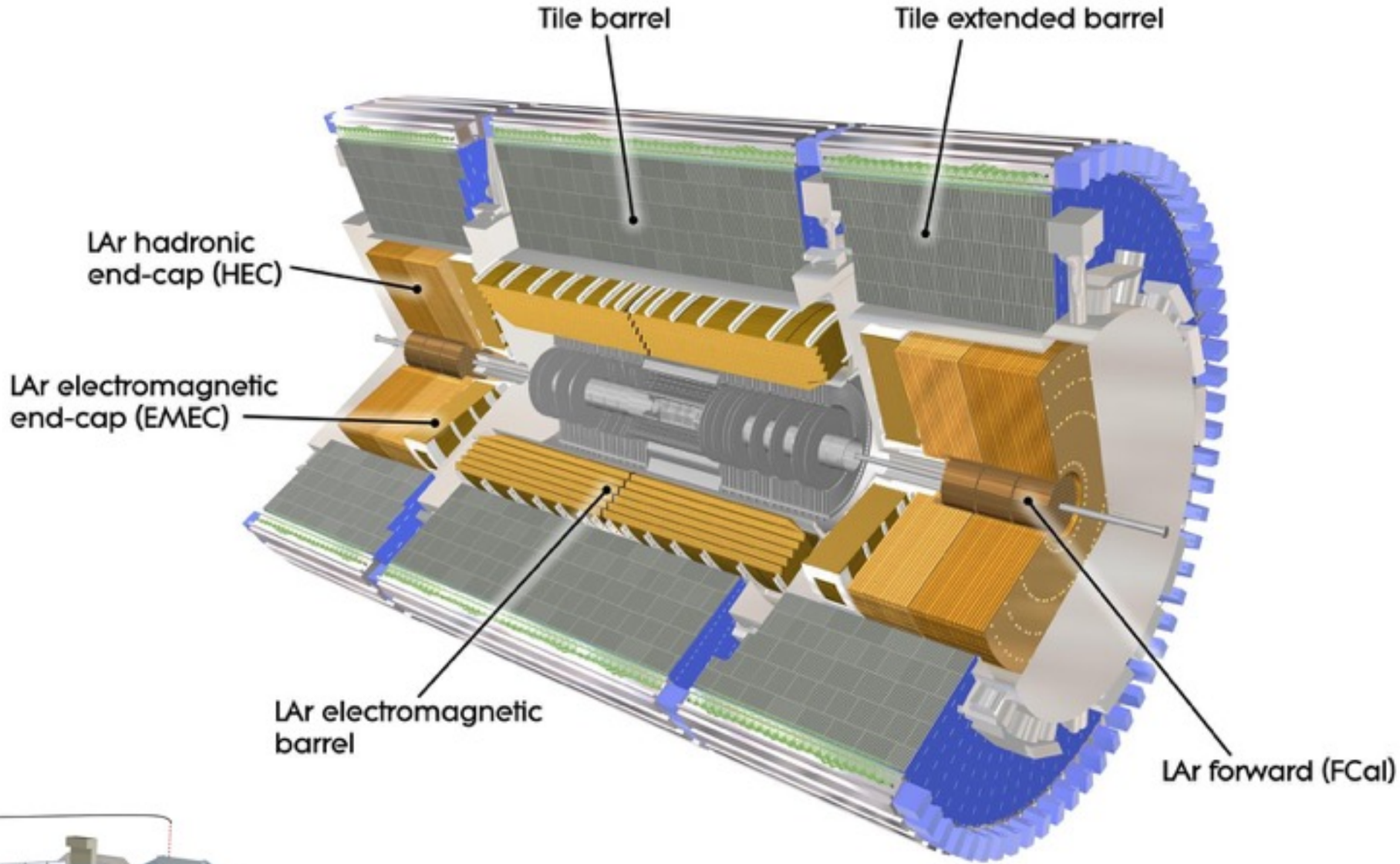
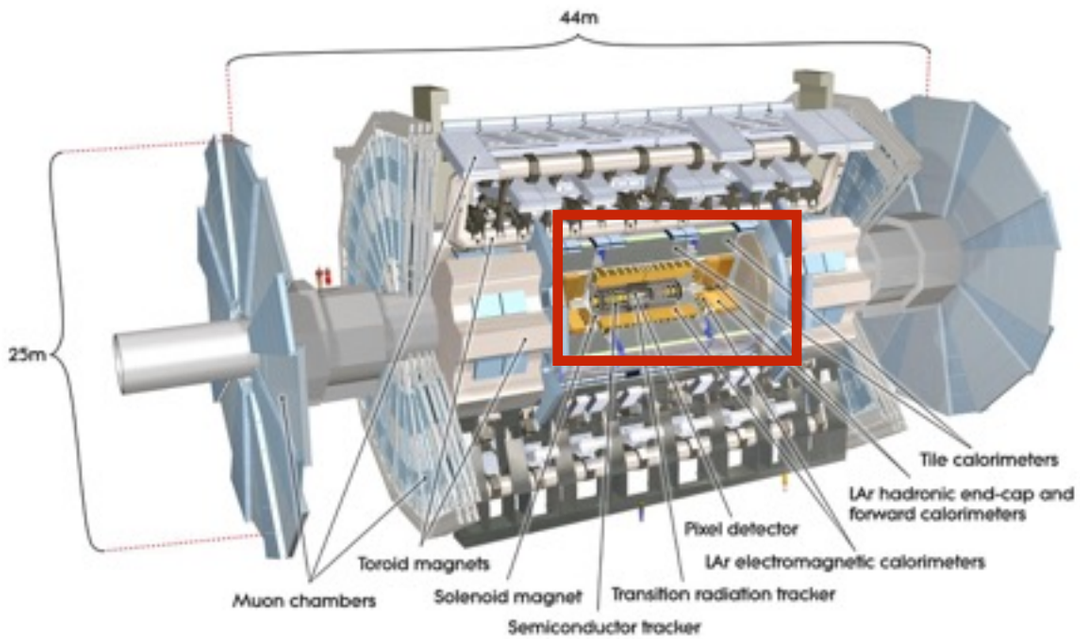
The ATLAS Experiment





Phase I Upgrade

Luminosity ~ 2 x10^{34} $cm^{-2}s^{-1}$

25 ns bunch crossing

Pile up of $<\mu>$~60

Level 1 rate =100 kHz

HLT rate = 1 kHz

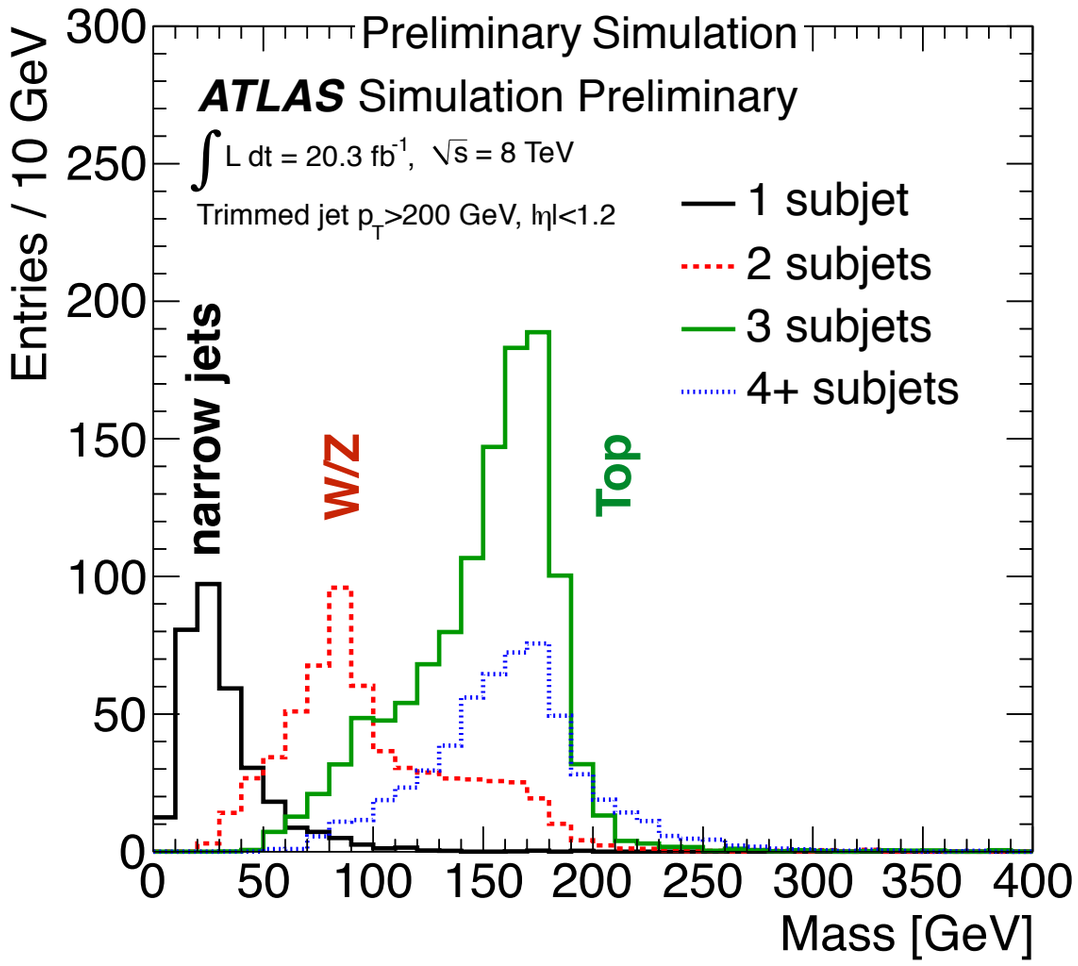
Motivation

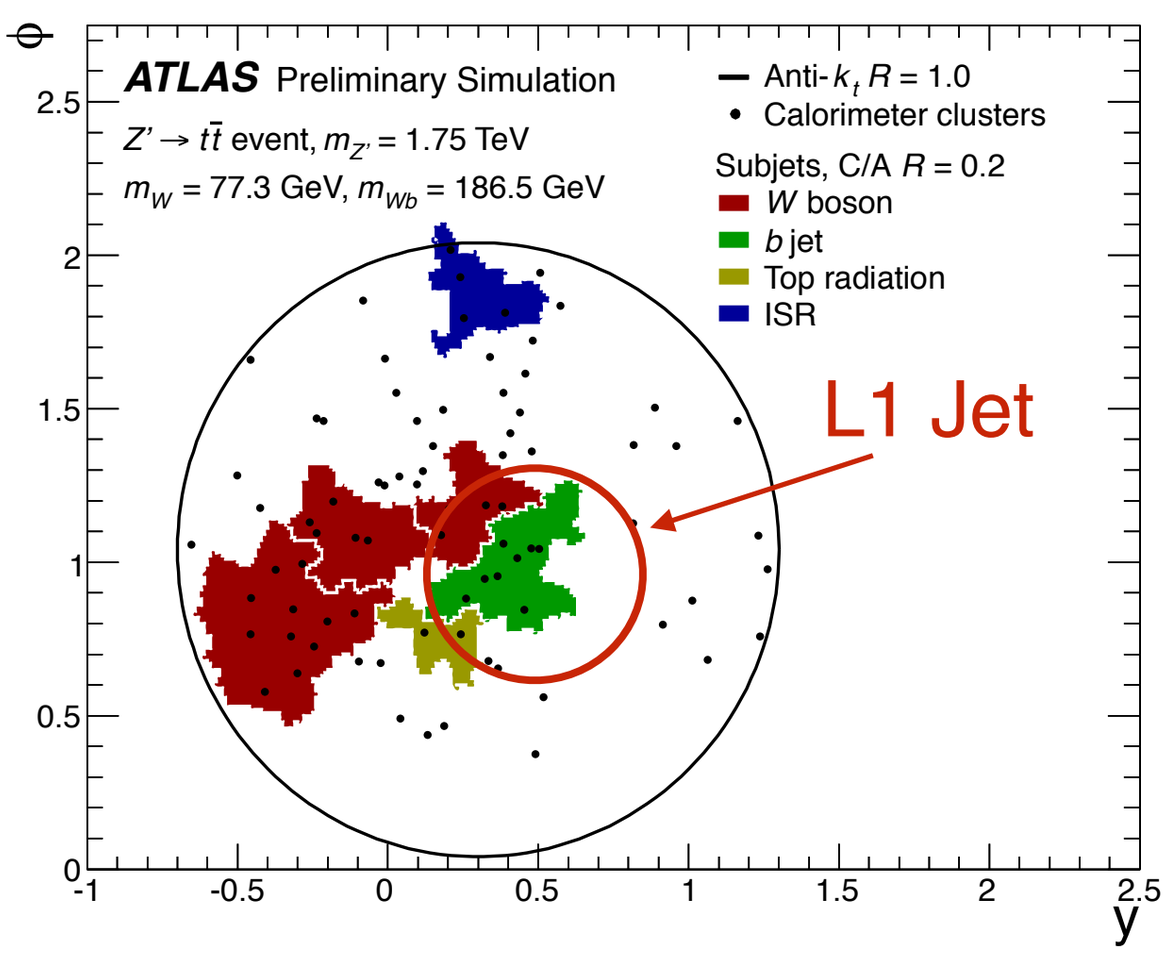
Increase trigger efficiency for *Fat-jets* in ATLAS

- High p_T bosons and fermions are a key component of ATLAS physics.
  - W,Z and H bosons, top quarks and exotic particles.
  - Many analyses with boosted objects.

- Analyses that addresses this kind of physics use large R jets with R > 1.

- The ATLAS Level 1 trigger is designed for narrow jets, with limited acceptance for large objects.

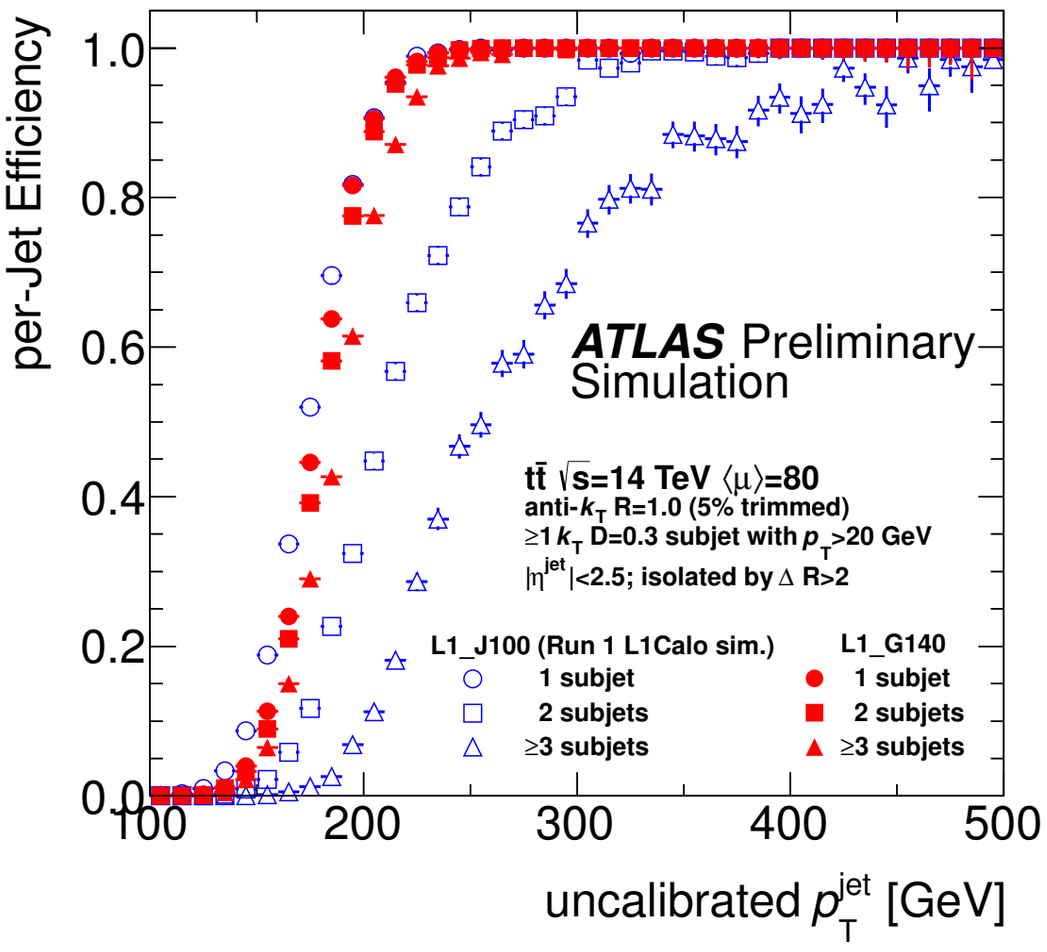




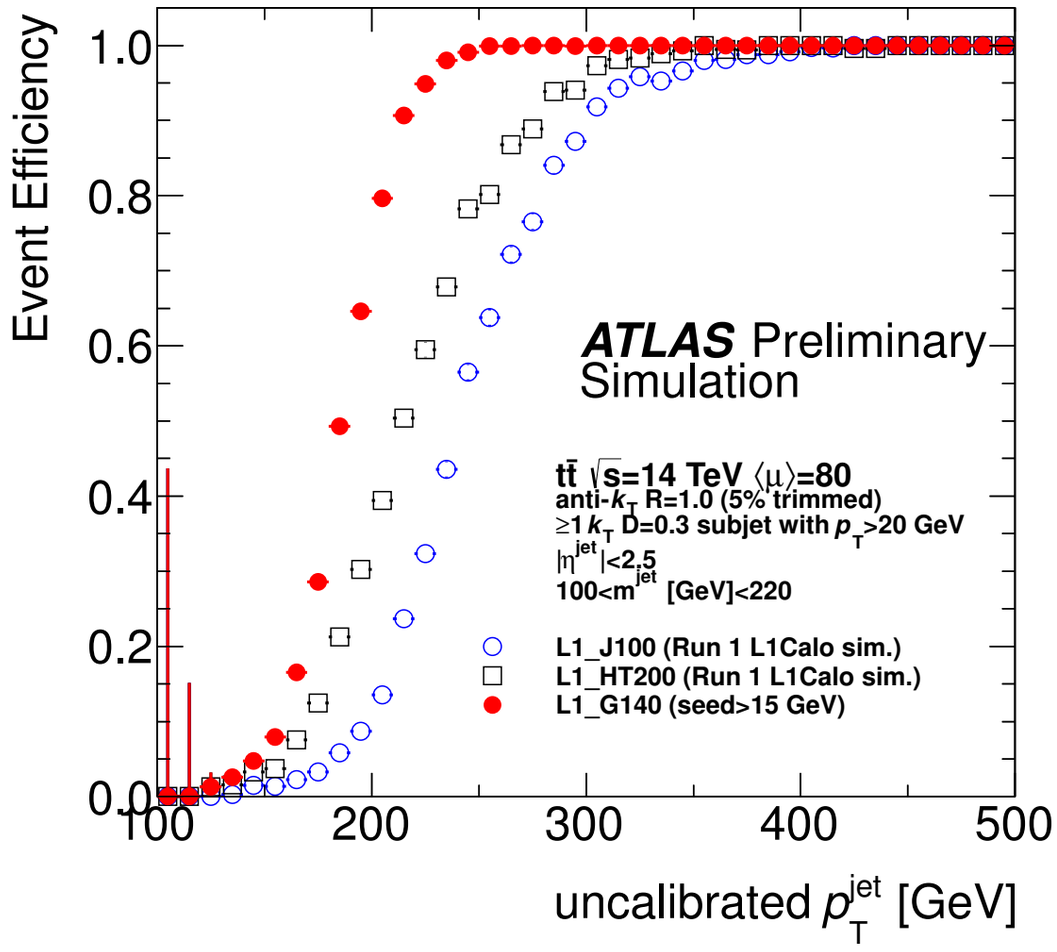
Simulation Studies

Larger trigger acceptance

boosted top



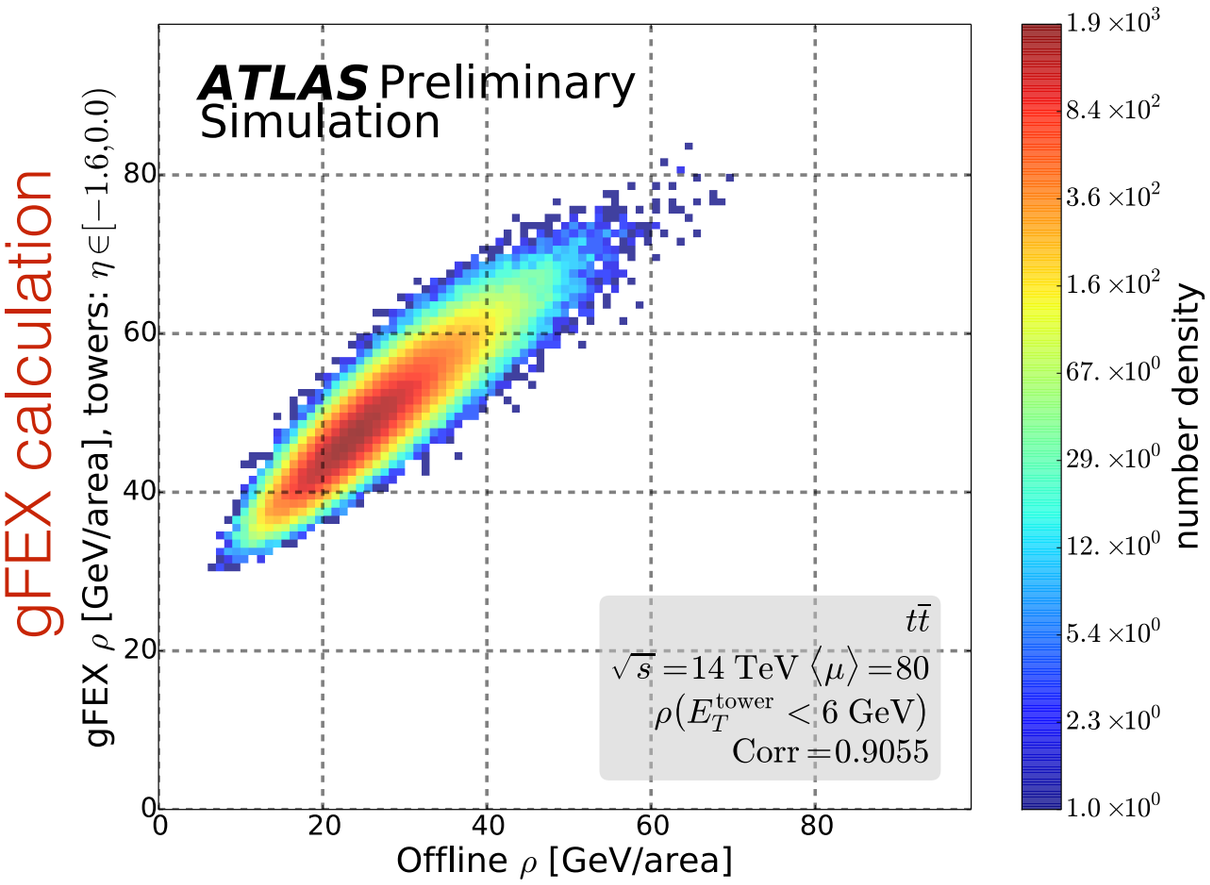
$H \rightarrow b\bar{b}$



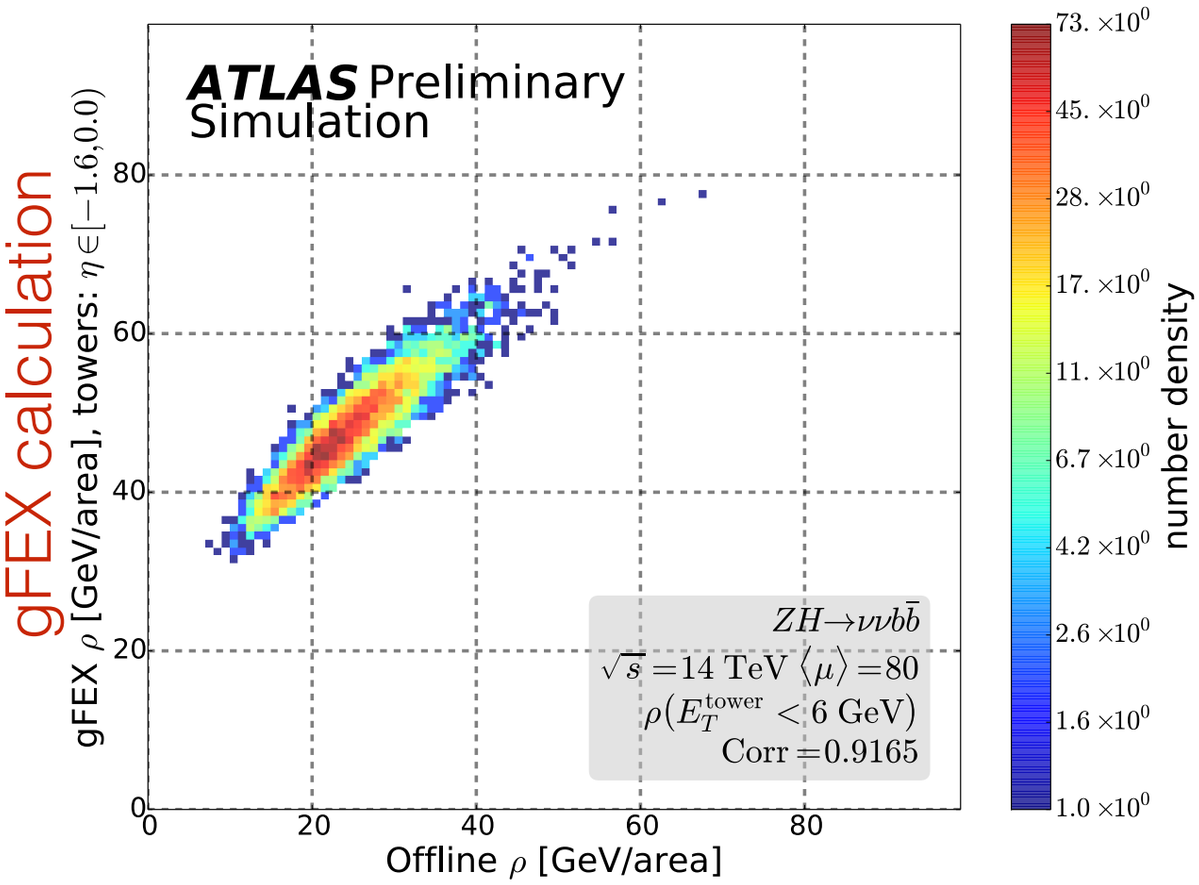
Simulations performed for 14 TeV, and for a $<\mu>$ = 80.

Simulation Studies

Jet energy pile up subtraction



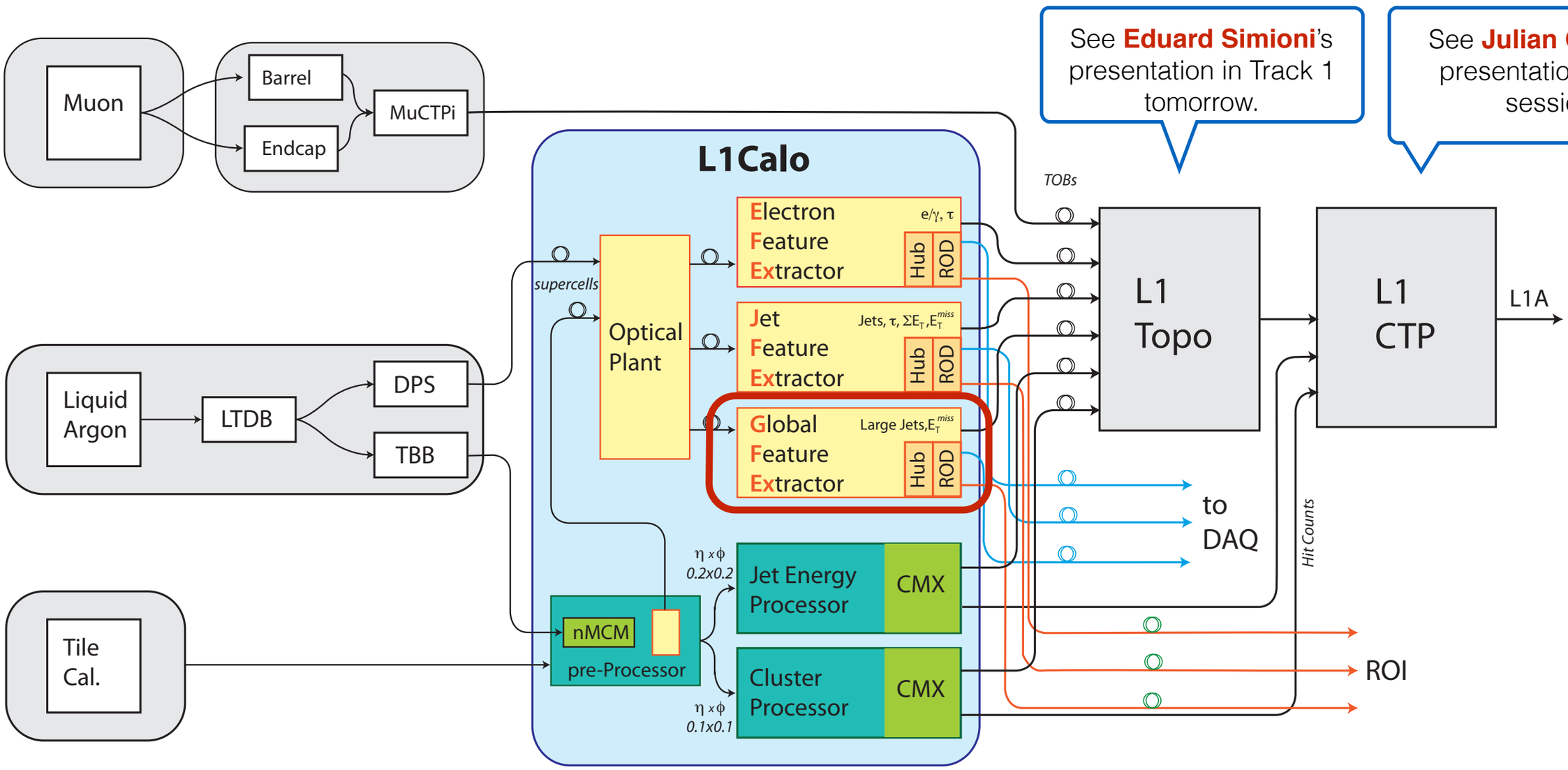
offline calculation



offline calculation

Correlation between the event energy density (x) and estimated by gFEX (y). The correlation is better than 90%.

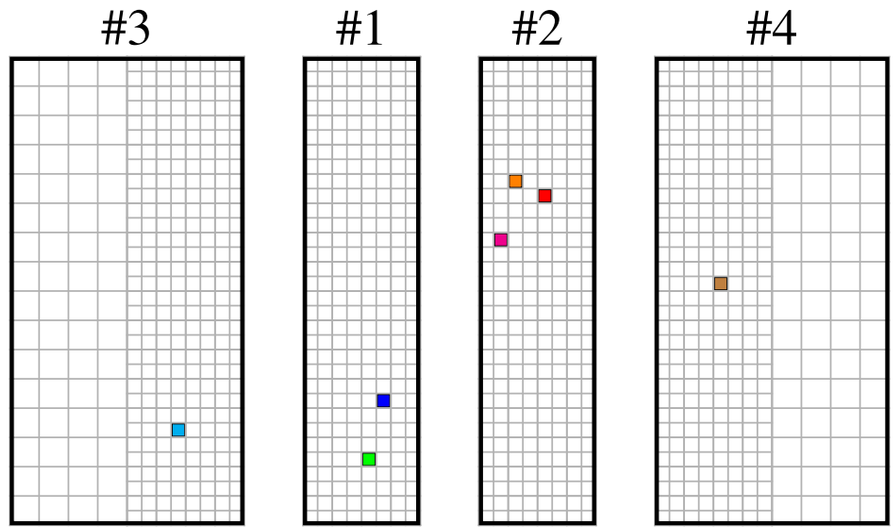
gFEX in ATLAS L1Calo



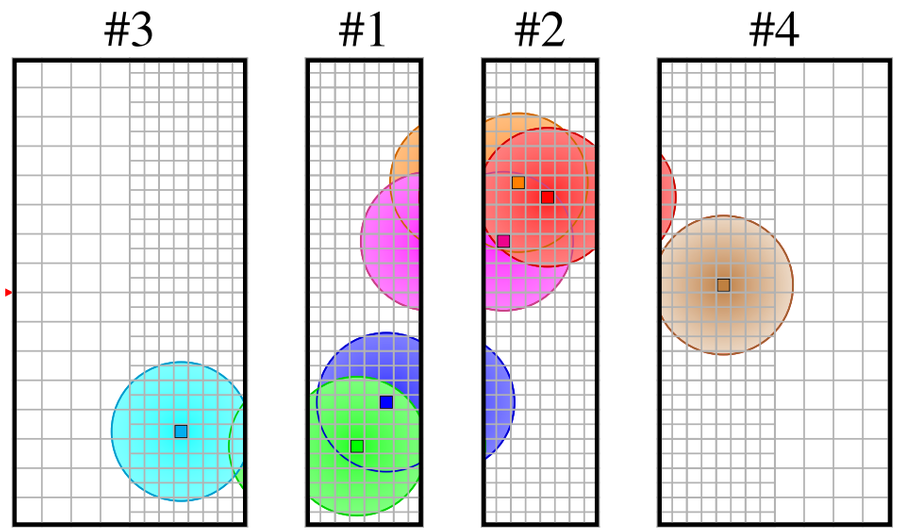
gFEX is a component of the ATLAS L1 Calo system in **Phase I upgrade**. It complements the electron and jet feature extractors. It is a single board system. Both eFEX and jFEX are multi-board systems.

See **Reiner Hauser**'s talk on ATLAS data flow in Track 1, tomorrow.

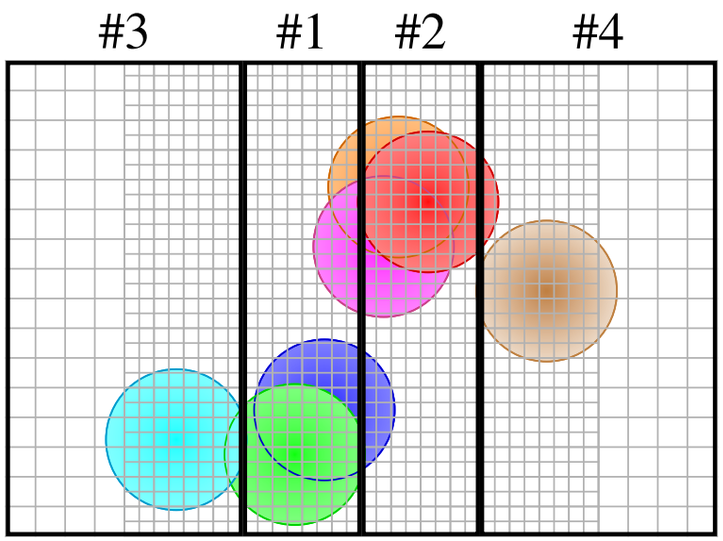
Finding Large Radius Jets



STEP 1 - Find seeds. Seeds are towers with energy above a set threshold.



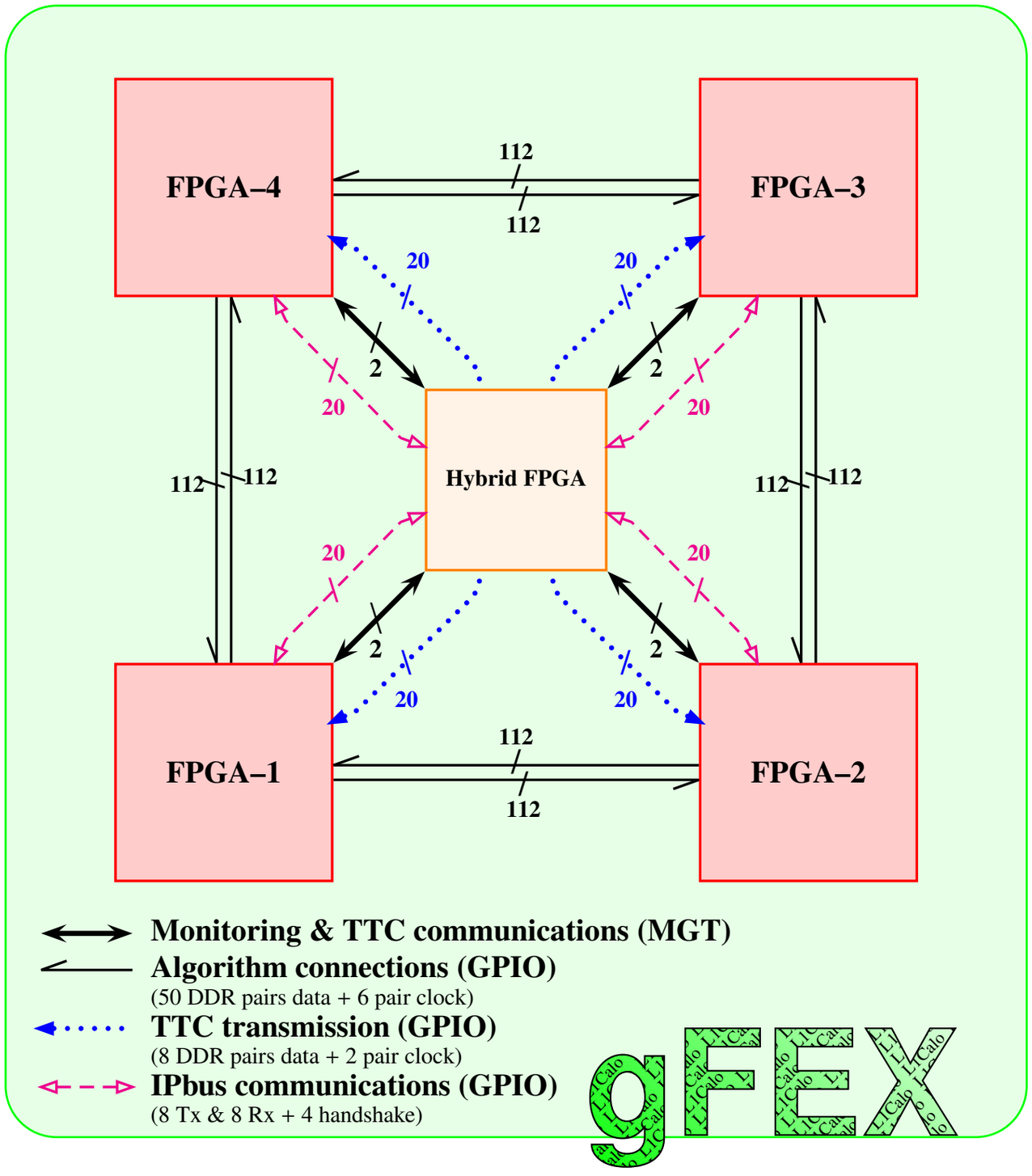
STEP 2 - Sum energy from neighboring towers. Concurrently, estimate pileup energy.



STEP 3 - Subtract pileup energy and “join” results. The final result is stored on processing FPGAs.

325 ns latency.

gFEX Concept

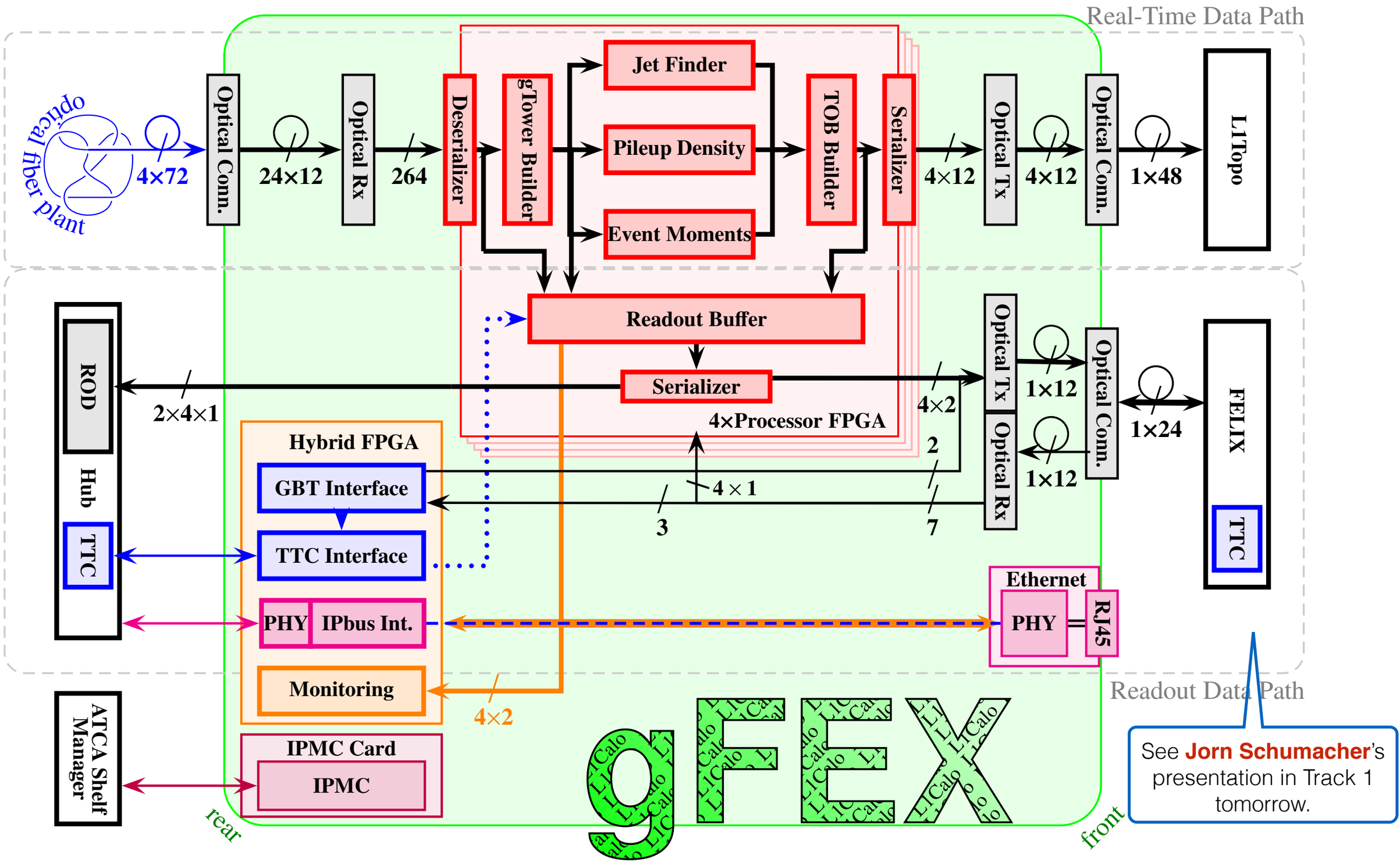


- Coarse granularity data ($\Delta\eta$x$\Delta\varphi$=0.2x0.2) from calorimeters are received by high speed optical links and processed by four large FPGAs.

- The processing FPGAs are monitored and programmed by a Hybrid FPGA (SoC).

- Results are transferred to the next level in L1 trigger.

gFEX: Processing Chain and Interfaces



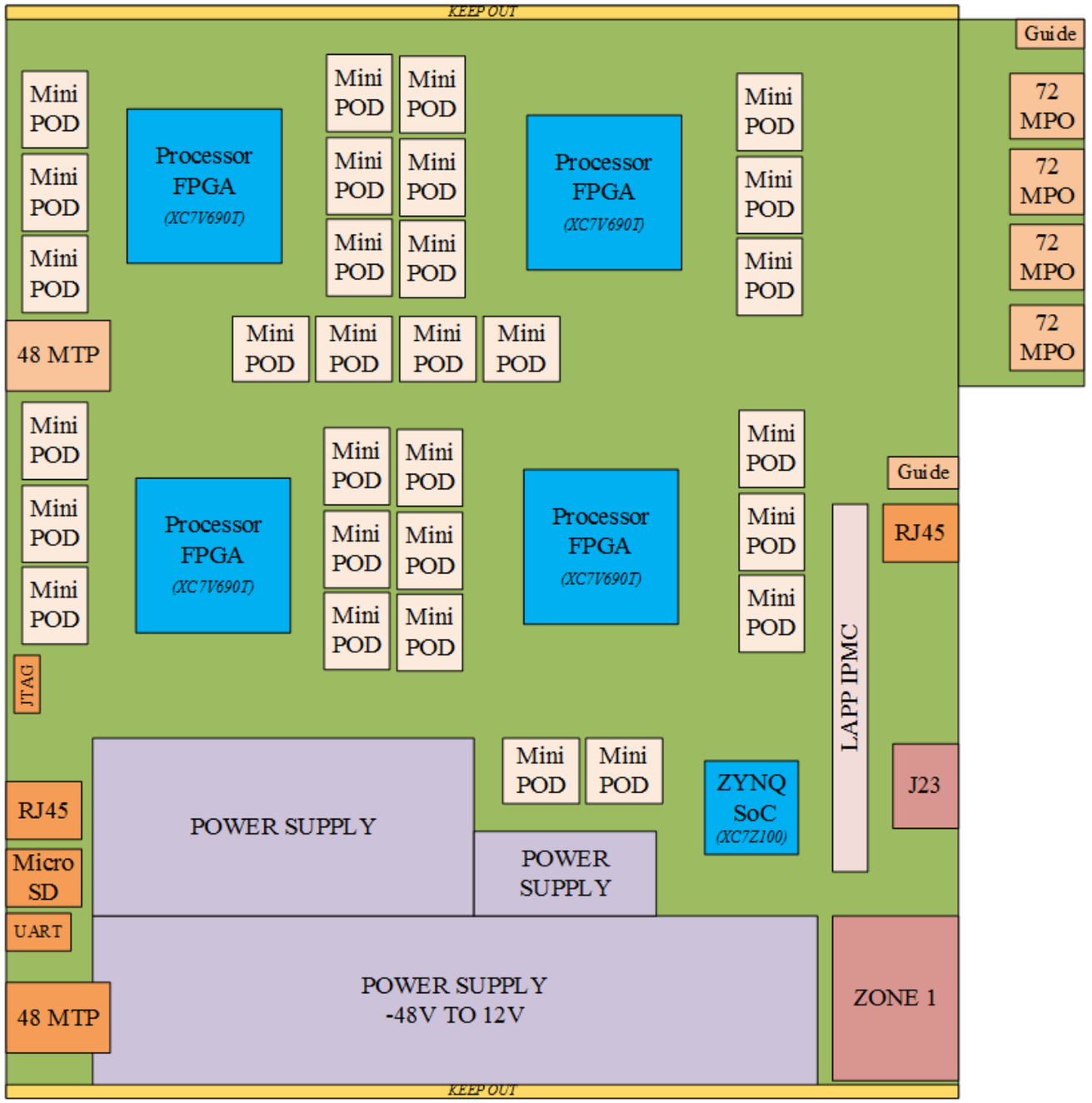
gFEX Floor Plan

1. The baseline FPGA is the **XC7VX690T-FFG1927** speed grade **-3** @ 320 MHz.

2. The SoC is the ZYNQ **XC7Z045-FFG900,** with dual ARM core and Linux OS (PetaLinux).

3. Input/Output
   - 4x 72-fold MPO* connectors (IN)
   - 2x 48 MPO* connectors (OUT)
   - miniPODs for Rx and Tx
   - JTAG, UART, RJ45 (Front)
   - ATCA Zone 1 & J23 ADF+ (Back)

4. The number of **input fibers** is 264 (at 6.4 Gb/s) or 232 (at 11.2 Gb/s).



(*)MPO - Multiple-Fiber Push-On/Pull-off

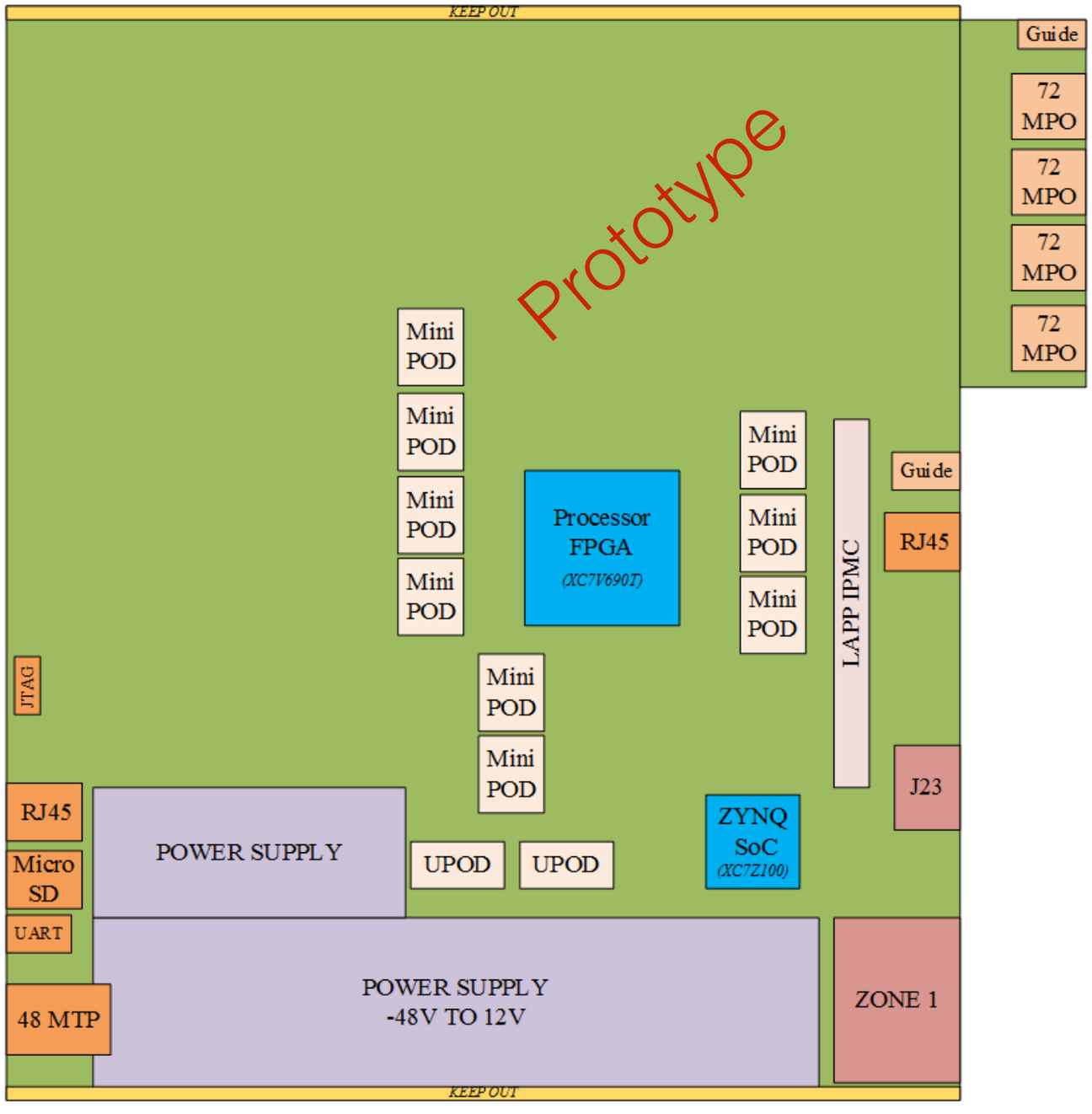
Development Plans

1. gFEX is being developed in stages. The first phase (*ongoing*) is to prototype a board to assure full integration with L1 Calo. In a second stage a board with four FPGAs will be produced.

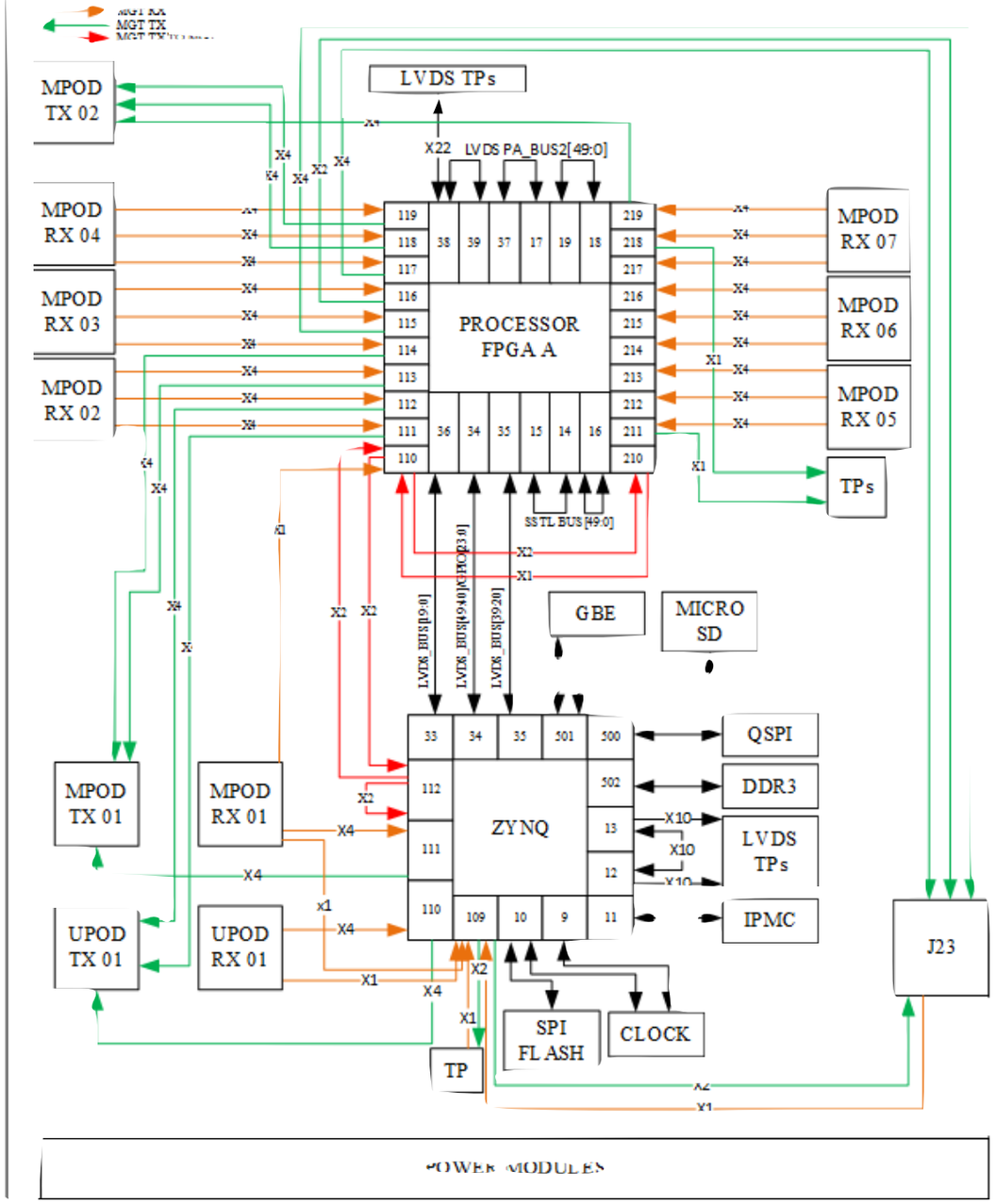
2. High speed optical links will be tested. Supported I/O speeds are 6.4, 9.6, 11.2 and 12.8 Gb/s.

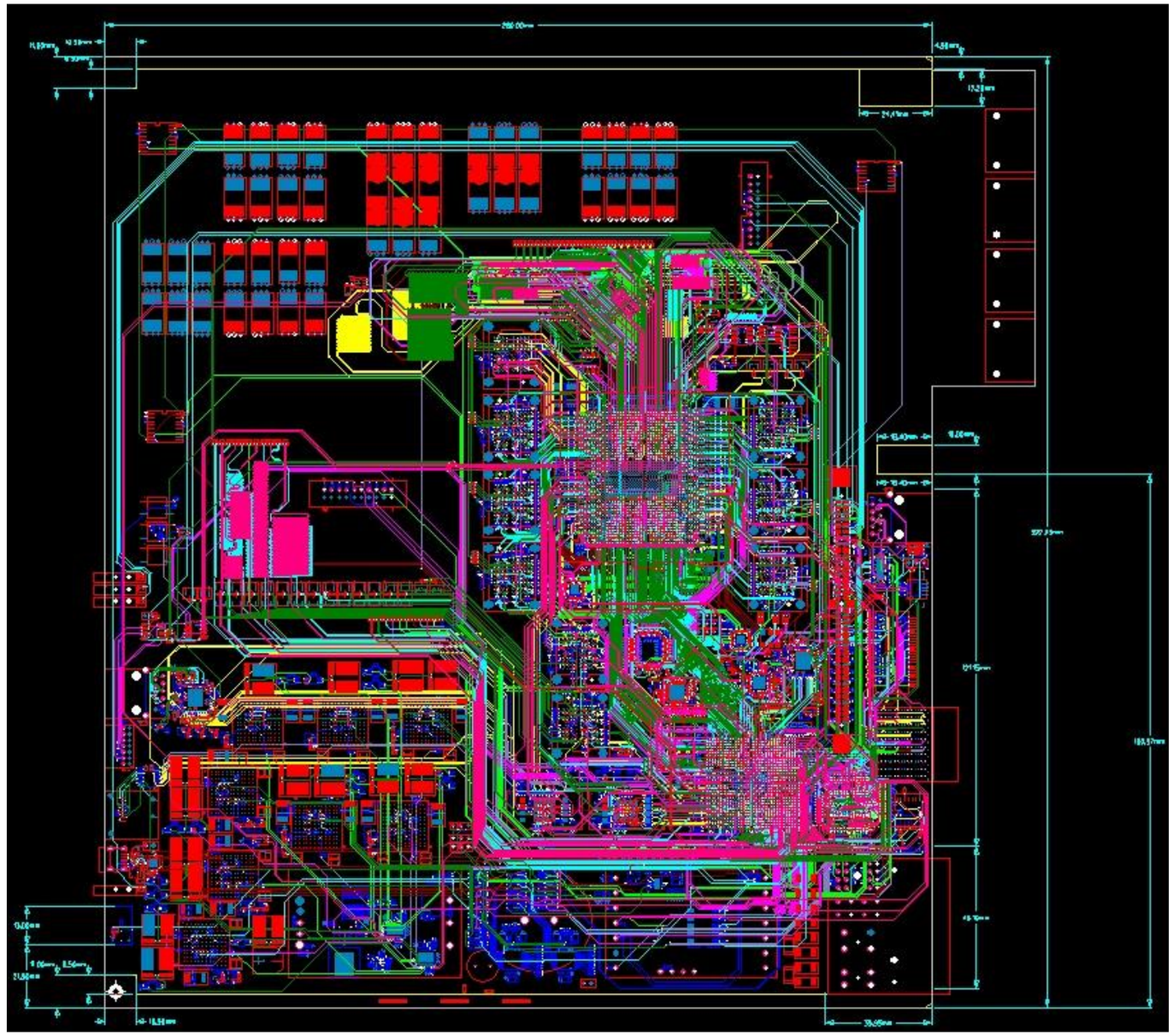
3. Integration and link speed tests will take place at the end of 2015.

4. Firmware for data processing is being developed in parallel using commercial boards.



The Prototype Board





Prototype Schematic and Layout are complete! It is implemented in an ATCA board form factor.

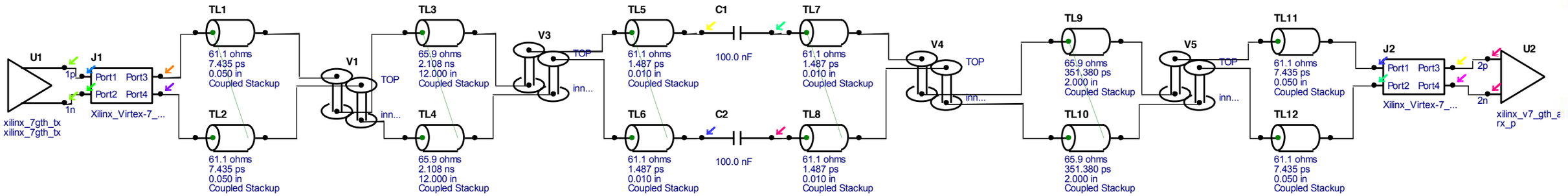
Challenges

1. gFEX will be a 26 layer board, with a total thickness of ~2.6 mm.

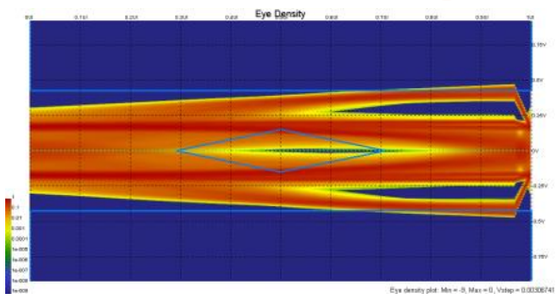
2. The choice of material is critical for the high speed traces within the board. Selected **Megtron 6**.

HyperLynx LineSim v8.2.1

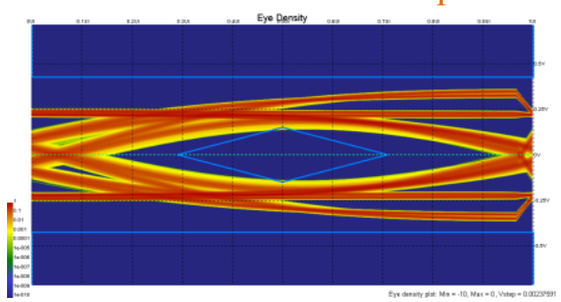
GTH-to-GTH Link simulation



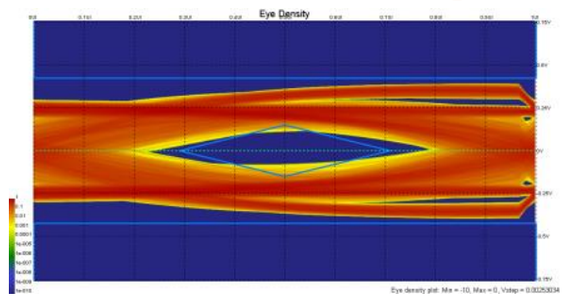
14 inch/FR4/with stub/9.6 Gbps



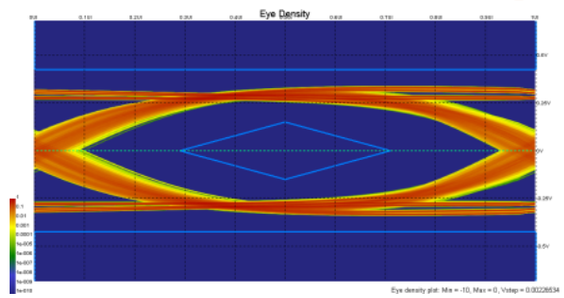
14 inch/FR4/without stub/12.8 Gbps



14 inch/M6/with stub/12.8 Gbps



14 inch/M6/without stub/12.8 Gbps



Summary

The global feature extractor, gFEX, will add to ATLAS the capability to trigger on large radius jets at Level 1.

It is based on FPGA processing. Four large FPGAs will receive coarse data (0.2x0.2) from the EM and HAD calorimeters and select events of interest.

Prototype is now being built. Initial prototype addresses the interfaces with ATLAS L1. After this phase a full processor will be built.

gFEX is processor board that has a large number of high speed I/O lines and could be used in other applications.

Extra Slides

gFEX: number of optical fiber connections

		Link Speed											
		6.4 Gb/s			9.6 Gb/s			11.2 Gb/s			12.8 Gb/s		
Partition	Coverage	gTowers/Fiber	bits/gTower	Fibers	gTowers/Fiber	bits/gTower	Fibers	gTowers/Fiber	bits/gTower	Fibers	gTowers/Fiber	bits/gTower	Fibers
Barrel EM	$\|\eta\| < 1.6$	8	15	64	8	22	64	8	26	64	8	30	64
Tile (Phase I opt.2)	$\|\eta\| < 1.6$	16	?	32	16	?	32	16	?	32	16	?	32
Tile (Phase I opt.3)	$\|\eta\| < 1.6$	12	10	48	12	?	48	12	?	48	12	?	48
Tile (Phase II)	$\|\eta\| < 1.6$	8	15	64	8	22	64	8	26	64	8	30	64
Standard EMEC	$1.6 < \|\eta\| < 2.4$	7	17	32	7	26	32	7	30	32	7	35	32
Special EMEC	$2.4 < \|\eta\| < 3.2$	10	12	32	14	12	24	14	12	24	20	12	16
HEC	$1.5 < \|\eta\| < 3.2$	12	10	48	18	10	32	18	11	32	18	11	32
FCAL 1	$3.1 < \|\eta\| < 4.9$	12	11	12	16	11	8	16	11	8	22	11	6
FCAL 2&3	$3.2 < \|\eta\| < 5.0$	12	11	12	16	11	8	16	11	8	22	11	6
Total (Phase II)				264			232			232			220

gFEX References

Performance Plots (Simulation)

https://twiki.cern.ch/twiki/bin/view/AtlasPublic/JetTriggerPublicResults#Global_Feature_Extraction_gFEX_P

gFEX Prototype Technical Specification

https://edms.cern.ch/file/1425502/1/gFEX.pdf