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High-Luminosity LHC

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ABSTRACT: The ATLAS experiment is a general purpose detector aiming to fully exploit the discovery potential of the Large Hadron Collider (LHC) at CERN. It is foreseen that after several years of successful data-taking, the LHC physics programme will be extended in the so-called High-Luminosity LHC, where the instantaneous luminosity will be increased up to $5 \times 10^{34}\,\mathrm{cm^{-2}\,s^{-1}}$. For ATLAS, an upgrade scenario will imply the complete replacement of its internal tracker, as the existing detector will not provide the required performance due to the cumulated radiation damage and the increase in the detector occupancy. The current baseline layout for the new ATLAS tracker is an all-silicon-based detector, with pixel sensors in the inner layers and silicon micro-strip detectors at intermediate and outer radii.

The *super-module* is an integration concept proposed for the strip region of the future ATLAS tracker, where double-sided stereo silicon micro-strip modules are assembled into a low-mass local support structure. An electrical super-module prototype for eight double-sided strip modules has been constructed. The aim is to exercise the multi-module readout chain and to investigate the noise performance of such a system. In this paper, the main components of the current super-module prototype are described and its electrical performance is presented in detail.

KEYWORDS: Particle tracking detectors; Si microstrip and pad detectors; Performance of High Energy Physics Detectors

Contents

1 Introduction

The ATLAS experiment [1] is a general purpose detector installed at the CERN Large Hadron Collider (LHC). During 2012, the LHC has delivered proton-proton collisions at a centre-of-mass energy of $\sqrt{s} = 8$ TeV, with total integrated and peak luminosities for ATLAS of $\sim21.7\,\mathrm{fb}^{-1}$ and $\sim7.7 \times 10^{33}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$ respectively. A major luminosity upgrade of the LHC (the so-called High Luminosity LHC or HL-LHC) is foreseen for ~2022, where the instantaneous luminosity will reach up to $5 \times 10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$. With a target of collecting a cumulated integrated luminosity of

$3000 \, \text{fb}^{-1}$ after ten years of operation at the HL-LHC, the ATLAS experiment will continue to explore the origin of the electroweak symmetry breaking mechanism at the highest energy frontier. The HL-LHC will allow for a rich physics programme, including high-precision measurements and searches for new physics beyond the Standard Model.

As a consequence of the the increased instantaneous luminosity expected at the HL-LHC, all major ATLAS sub-systems (from the detectors to the trigger and DAQ systems) must be upgraded. In particular, a complete replacement of the ATLAS internal tracker, the Inner Detector (ID), is already anticipated. The current ID combines high resolution discrete silicon detectors (pixel and micro-strips) at the inner and intermediate layers, with a gaseous straw-tubes detector at the largest radii. It is composed of three sub-systems, namely from the inside: the Pixel detector, the Semiconductor Tracker (SCT) and the Transition Radiation Tracker (TRT). A central superconducting solenoid magnet surrounding the TRT provides a 2 T solenoidal magnetic field. Although the ID has been designed to operate ten years at the peak luminosity of $10^{34} \, \text{cm}^{-2} \, \text{s}^{-1}$, its performance will degrade with the cumulated effects of radiation damage and ageing, and it will approach the end of its lifetime by the end of the LHC programme (where the luminosity is expected to reach $2 \times 10^{34} \, \text{cm}^{-2} \, \text{s}^{-1}$). Moreover, due to the very high density of particles that will be produced at the HL-LHC,[1] the current ID would suffer from a large increase in both the integrated radiation damage and the detector occupancy, compromising its tracking capabilities far beyond an acceptable level [2].

Although the final layout has not been fixed yet, most probably the new ATLAS tracker (Inner Tracking Detector or ITK) will be an all-silicon system with new detector technologies and increased granularity [2, 3]. Its design must ensure radiation hardness, low detector occupancy and excellent tracking performance in a high pile-up environment. At present, the ITK baseline layout consists of pixel detectors in the innermost layers and silicon micro-strip detectors at intermediate and outer radii. In the barrel region, at least 4 pixel layers (with a pixel size of $25 \times 150 \, \mu\text{m}^2$ and $50 \times 250 \, \mu\text{m}^2$ in the two inner and two outer pixel layers, respectively) are followed by 5 double-sided stereo silicon micro-strip layers. The innermost 3 strip layers consist of *short-strip* (SS) sensors ($\sim$24 mm strip-length), while *long-strips* (LS) detectors (of $\sim$48 mm strip-length) are used for the two outermost layers. The whole pixel detector would extend up to a radius $R \sim 250$ mm, with the innermost layer being located at $R \sim 33$ mm to be as close as possible to the beam-pipe. The forward region is covered with 6 pixel and 7 strip disks, extending up to $|Z| \sim 1.7$ m and $|Z| \sim 3$ m respectively with equivalent granularities. This layout ensures an 11 hit coverage in the pseudo-rapidity range of $|\eta| < 2.7$ for interactions within $|Z| < 15$ cm.

Concerning the future micro-strip detector, one integration concept for the barrel region is the so-called *stave* concept [4], in which a common mechanical structure integrates the sensors, the electrical lines (bus cable) and the cooling circuit. The stave is a $\sim$1.2 m long object that has a central core composed of a spacing material (carbon-foam or honeycomb) and carbon fiber facings glued on both sides of it. A bus cable for the electrical signals is laminated on top of the facings. Single-sided silicon micro-strip detectors are glued over the bus cable and hybrids carrying the front-end electronics are glued on top of the sensitive side of the sensors.

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[1] Assuming a 25 ns bunch-spacing configuration, it is expected a mean number of interactions per crossing of $\sim$140 and more than 1000 tracks per unit rapidity at an instantaneous luminosity of $5 \times 10^{34} \, \text{cm}^{-2} \, \text{s}^{-1}$.
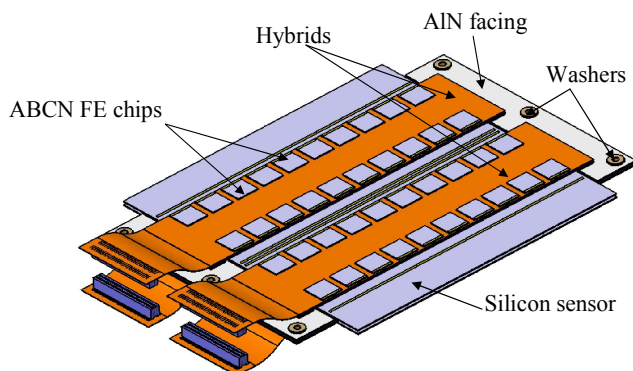
Figure 1. Overview of the main components of the short-strip double-sided module (prototype version using ABCN-25 readout ASICs, see section 2.2).

The *super-module* is another, more conservative, integration concept in which double-sided silicon micro-strip modules are mounted in a light, stable carbon-carbon local support structure. In this case, a module is considered to be the minimal detector unit. The heat generated from the front-end electronics is transferred to the cooling pipes located in the lateral sides of the support frame. The local support is designed to hold at least 12 modules (depending on the layout), enabling a full coverage in both ϕ and Z coordinates (dead-space between adjacent sensors is avoided by staggering the modules along the Z-axis) for the barrel region.

Both approaches allow the end insertion of the support into the overall barrel structure, a solution providing flexibility for integration, commissioning and rework.

This paper is organized as follows. In section 2 the double-sided silicon strip module is introduced. Its main components are briefly described. The super-module electrical prototype, an eight-module setup developed to demonstrate the feasibility of a strip tracker based in the double-sided strip module concept, is presented in section 3. The main electrical interfaces are explained. In section 4, electrical results from the multi-module setup are shown. Prospects for a future module design, using the next generation of readout ASICs, are presented in section 5. Finally, a summary is given in section 6.

2   The double-sided silicon micro-strip module

The double-sided silicon micro-strip module (DSM) [5] is proposed as the minimal detecting unit for the short-strip region of the future ATLAS ITK. Figure 1 shows a schematic layout of the current module design including its main components. The DSM is a top-bottom symmetric object composed of two $\sim 10 \times 10\,\text{cm}^2$ n-on-p silicon micro-strip sensors glued back-to-back to a central Thermo-Pyrolitical-Graphite (TPG) baseboard, four bridged hybrids (each holding 20 readout ASICs arranged in two columns of ten) placed by pairs on both sides of the module, and two aluminium-nitride (AlN) ceramic facing plates located at each far-end of the baseboard. Each hybrid is bridged on top of the AlN facings using a carbon-carbon sheet glued underneath the flex circuit so that the hybrids remain mechanically, electrically and thermally decoupled from the silicon sensors. The TPG provides to the module the mechanical stability and ensures excellent
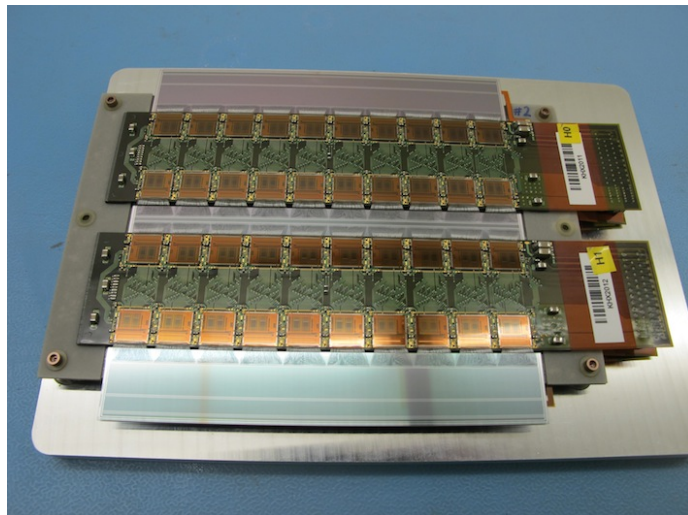
Figure 2. Photograph of a real prototype double-sided module.

thermal contact for optimum dissipation of the heat generated by the front-end electronics. Precision washers accurately position the module on the local support structure. Figure 2 shows a fully-assembled prototype module.

The main advantages of this module design include:

- the two sensors mounted back-to-back allowing an accurate space-point reconstruction with a relative sensor alignment at the micron level. The modules are then centred and aligned precisely on the local support structure.

- independent hybrid and sensor thermal paths and usage of low thermal expansion materials with good thermal conductivity to minimize deformations during temperature cycling.

- optimization of the module design for easy handling during prototyping and quality assurance studies, these being key aspects for a large-scale production.

The thermal and thermo-mechanical performance of the current DSM prototype has been studied in detail with Finite Element Analysis (FEA) simulations under different load cases and convection effects. The reader may refer to [6] for further details.

2.1 Silicon sensor

The detectors currently used in the DSM prototypes are single-sided AC-coupled sensors with n-type readout strips in a p-type silicon bulk [7]. The n-on-p technology benefits from not suffering type-inversion after irradiation in the n-type bulk and the sensors remain operative even if biased under partial-depletion voltage. Figure 3 shows the mask layout of the detector. The sensors, manufactured in a 6-inch (150 mm diameter) wafers by Hamamatsu Photonics, HPK [8], have an area of $97.54 \times 97.54 \, \text{mm}^2$ and a thickness of $320 \, \mu\text{m}$. The distance from the sensitive region to the physical cut edge is $980 \, \mu\text{m}$. The bulk substrate is float zone (FZ) p-type with a crystal orientation $\langle 1\,0\,0 \rangle$. The n^+ implants are $16 \, \mu\text{m}$ wide and are biased through polysilicon resistors and AC-coupled to $22 \, \mu\text{m}$ wide aluminium readout strips. The n^+-strips are isolated by a common p-stop
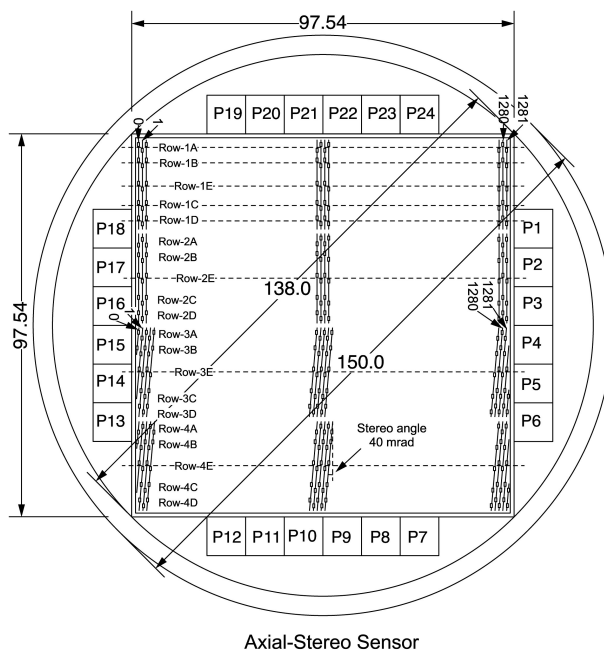
Axial-Stereo Sensor

Figure 3. Mask layout of the short-strip silicon sensor. The main detector (largest area in the mask) is divided into four segments. The top and second from top segments have axial strips; the bottom and second from bottom segments have stereo strips (inclined by an angle of 40 mrad). The 6-inch wafer also contains 24 miniature sensors (P1 to P24) with different isolation structures each (p-stop, p-spray, etc.). The miniature sensors ($100\,mm^2$ total area, 104 axial readout strips with a strip pitch of $74.5\,\mu m$) are used for pre and post-irradiation performance studies.

structure against possible shorts by surface charges. The sensors with p-stop isolation have shown breakdown at higher bias voltages, and also better n^+-strip isolation after irradiation [9], than those with p-spray isolation.

The detector comprises four segments, two with *axial* strips parallel to the sensor edges and two with *stereo* strips inclined by an angle of 40 mrad, being the average strip length and pitch of 2.38 cm and $74.5\,\mu m$ respectively.[2] With 1280 strips per segment, each DSM has a total of 10240 readout strip channels. By integrating both axial and stereo strips in the same wafer, and from the small distance between sensors ($\sim$400 μm from the thickness of the baseboard), true 3D space-points are naturally created by gluing identical but $180°$-rotated wafers on each side of the baseboard. This facilitates the module assembly (an asset during the full-mass module production stage), as there is no need to implement a relative stereo rotation between the two detectors as in the case of using axial-only sensors.

Extensive tests have been performed to study the characteristics of the sensor prototypes both before and after irradiation [10–12]. The sensors are found to satisfy all the electrical pre-irradiation specifications in terms of full depletion voltage (FDV) and leakage current,[3] as well as for coupling capacitance, bias resistance or inter-strip capacitance and resistance. The performance of

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[2]In the case of the modules for the long-strip region, the sensor will have just two segments of longer (4.78 cm) strips, as the requirements in terms of channel occupancy are less stringent.

[3]For a non-irradiated sensor, the FDV is specified to be less than 500 V and the leakage current must not exceed 200 μA at 20°C.
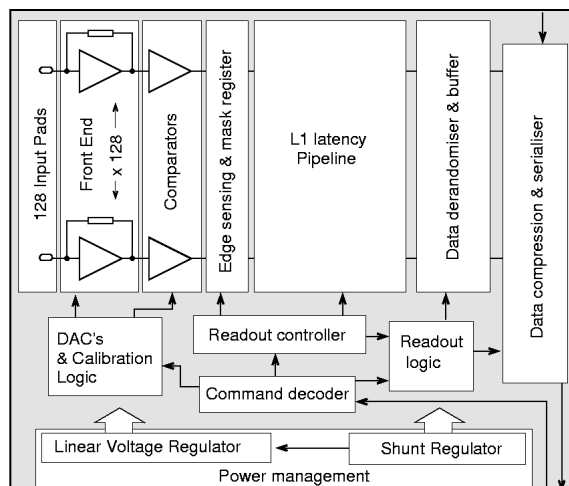
Figure 4. ABCN-25 ASIC block diagram.

$1 \times 1 \, cm^2$ miniature sensors irradiated to the maximum fluences (2×10^{15} 1-MeV-neutrons equivalent n_{eq}/cm^2 for the innermost barrel strip layer, including a safety factor of 2) has been evaluated in terms of surface and bulk damage, charge collection efficiency and signal-to-noise (S/N) ratio. A S/N of at least 23:1 has been measured, well above the 10:1 requirement for an efficient tracking at the HL-LHC.

2.2 Readout ASIC

The current prototype of the readout chip is the 128-channel ATLAS Binary Chip Next (ABCN) produced in $0.25 \, \mu m$ IBM CMOS technology (hence the chip will be referred hereafter as ABCN-25 [13]). Conceptually, it is very similar to the ABCD3TA chips used in the current ATLAS SCT strip tracker [14]. An evolution of this chip using 130 nm IBM CMOS technology (the 256-channel ABCN-13) has been recently submitted for fabrication and is intended for future evolutions of the prototype programme.

A simplified block-diagram of the ABCN-25 chip is shown in figure 4. The chip handles the readout of 128 channels with a binary architecture. The per-channel analogue stage comprises pre-amplification, shaping and differential discrimination. The binary data at the discriminator output is latched at every clock cycle to the input register and then buffered in a 256-cell (6.4 μs) pipeline. Upon the reception of a L1 trigger, the data corresponding to three bunch-crossings is transferred to a second-level derandomizer buffer with 128 bits depth (43 events). Data is then transferred to the readout buffer and compressed according to given selection criteria.

The configuration of the different chip parameters is made using read/write registers. A 128-bit Mask register is used to disable bad or noisy channels to avoid an increased data rate due to false hits. The ABCN-25 chip receives two clock inputs, the main Bunch-Crossing clock (always running at 40 MHz in synchronization with the beam crossing rate) and the readout clock used for data throughput. The front-end (FE) can be configured to operate at two different readout clock frequencies, either 40 or 80 MHz. A maximum data readout speed of 160 Mbits/s can thus be achieved avoiding deadtime. Multiplexing the data of several modules into a single optical link can easily increase the rate to the order of several Gbits/s (with current technologies).

The current powering scheme for the ATLAS SCT is based on parallel powering from off-detector power supplies. The increase in the number of readout channels for the upgraded ITK (an expected increase of a factor of $\sim$10) imposes severe constraints for the future powering strategy. More power must be delivered without increasing the cable density because of the lack of physical space[4] and because of the goal of minimising the material inside the tracker. Two different low-voltage powering schemes are currently being investigated: serial powering and parallel powering using DC-DC voltage converters. In the serial powering scheme, several modules are supplied with a common constant current source and the required voltage levels are provided by shunt and voltage regulators. In the parallel DC-DC scheme, a unique high (typically 10–12 V) input voltage line supplies the modules, and the operating low voltage (typically 2.5 V) is obtained typically through an inductor-based buck converter with a high conversion ratio and high efficiency [15]. The ABCN-25 chip implements a new power management block with two prototypes of distributed shunt regulator circuits for the serial powering scheme, and a low drop voltage regulator to supply the analog front-end voltage from the digital input. The nominal consumption of the analogue front-end is 0.7 mW per channel. The digital supply current typically is $\sim$90 mA at 2.5 V (40 MHz).

Each channel of the front-end has an internal calibration circuit that can be used to inject a test charge into the analogue chain. Upon reception of a specific command, the voltage pulse is generated by a chopper circuit and injected into the channel through a calibration capacitor. Measurements of the basic analogue front-end parameters have been performed by mounting ABCN-25 chips on different test board PCBs and prototype multi-chip flex hybrids. The resulting values for the input noise and gain (without input load), $\sim$400 electrons Equivalent Noise Charge (ENC(e)) and 100 mV/fC respectively, are in excellent agreement with the design values of the ASIC.

2.3 Hybrids

A four-layer copper-polyimide (Cu/PI) flexible circuit hybrid has been designed by KEK [16] and produced by Taiyo Industrial Co. [17]. The current hybrid layout is shown in figure 5. The size of the flex-circuit is $136 \times 28 \, \text{cm}^2$. The first two layers, L1 and L2, carry the main circuit patterns for the front-end chips, including redundancy lines, while layers L3 and L4 are used for respectively the power distribution and grounding. All Cu/PI sheets are made with adhesive-less technology, being the thickness of the polyimide and copper sheet of 25 and 12 μm respectively. Electrical connections among different layers are realized by either through-holes, penetrating all layers, or laser-cut via-holes between two adjacent layers. The usage of the button plating technology (plating in a limited area around the holes instead of having a whole plated surface) allowed to reduce by $\sim 40\%$ the weight of the bare flexible circuit with respect to the standard panel plating technique, achieving a final weight for the hybrid of 1.90 g.

A 400 μm thick and 112 mm wide carbon-carbon (CC) sheet made of uni-directional fibres is glued underneath the flex circuit to bridge the hybrid over the silicon sensor, avoiding any interference with the detector surface and allowing for a separate cooling path. Figure 6 shows photographs of the bare flex circuit top and bottom sides, and after adding the CC sheet on the bottom side. The main functions of the CC bridge are to provide mechanical rigidity to the hybrid, to improve its

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[4]The space available is constrained to the current ATLAS Inner Detector volume, as the calorimeters themselves will not be replaced for the HL-LHC operation.
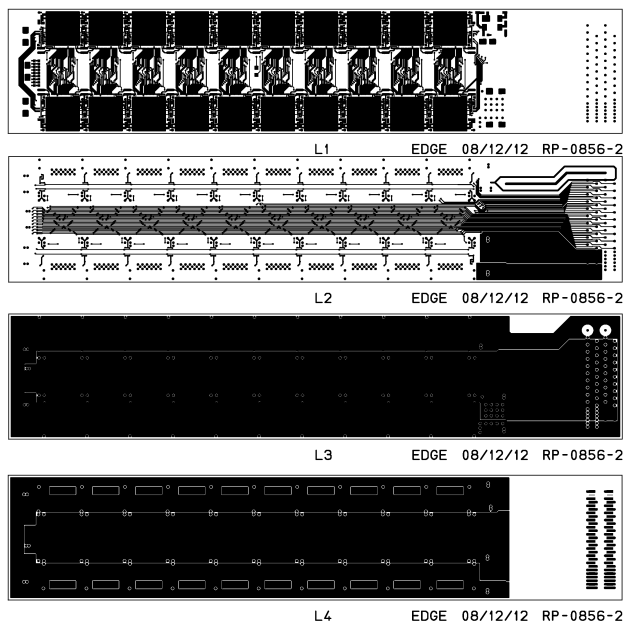
Figure 5. Layout of the KEK hybrid. The four circuit layers are labelled L1 (top) to L4 (bottom).

thermal performance and in addition to reinforce the mechanical rigidity of the module once the hybrids are glued on the AlN facings of the baseboard. Seventeen thermal through-holes are added underneath the analogue part of each ASIC. These vertical copper holes are filled with thermally and electrically conducting glue. This ensures thermal and electrical connections between each chip and the CC bridge. The effective thermal conductivity of these pillars is ~40 W/m K. The large thermal conductivity (~670 W/m K) of the CC-sheet allows the efficient transfer of the heat generated by the readout chips to the heat sink located at the bridge legs. At the last stage of hybrid assembly, a 0.8 mm pitch miniature connector is mounted at one end of the circuit layers to route the LVDS signals towards the data acquisition system. The total weight of the hybrid, including flex-circuit layers and CC-bridge but excluding electrical components (connector, SMDs, ASICs) is 5.0 g, corresponding to 0.20% X_0 equivalent radiation length, normalized to the sensor area.

2.4 Baseboard and AlN facings

The baseboard, currently consisting of a rectangular $127 \times 79 \, \text{mm}^2$ sheet of Thermal Pyrolytical Graphite (TPG), acts as the thermo-mechanical core of the DSM. The TPG is a pyrolitic carbon-based anisotropic material with a high in-plane thermal conductivity of ~1800 W/m·K and low radiation length. As the baseboard is used in direct contact to the silicon sensors, the TPG is coated with a thin film (~20 μm thick) of Parylene allowing for a complete electric insulation with respect to the HV sensor backplane. The Parylene deposition is performed with a chemical vapor deposition technique, and it includes an additional 50–80 μm glue/air matrix layer.

On each side of the baseboard, two ~20 μm thick and 14.5 mm wide aluminium-nitride (AlN) ceramic pieces are glued at the two far-ends. The AlN facings have a relatively high thermal conductivity ~180 W/m·K for an electrical insulating ceramic. Because of the choice of materials with high thermal conductivity (to help in the power dissipation), low thermal expansion coefficient
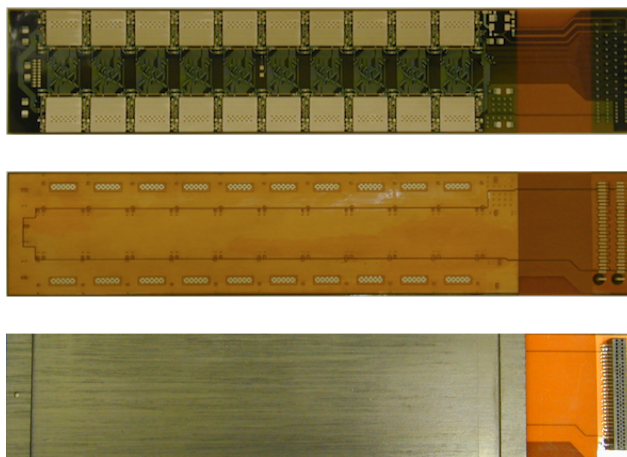
Figure 6. Photographs of the bare flex printed circuit front (top) and back-side (middle), and after mounting the carbon-carbon sheet and the 0.8 mm-pitch miniature Samtec connector (bottom).

and low mass, an optimal heat path, allowing for an efficient flow from the parts acting as heat sources (front-end chips through the hybrid bridge feet, silicon sensors) to the cooling contacts, is ensured. Furthermore, the use of the AlN facings increases the module stiffness that is reinforced later-on once the two silicon detectors are glued to the baseboard and the bridged hybrids are glued on top of the facings during the assembly process of the module.
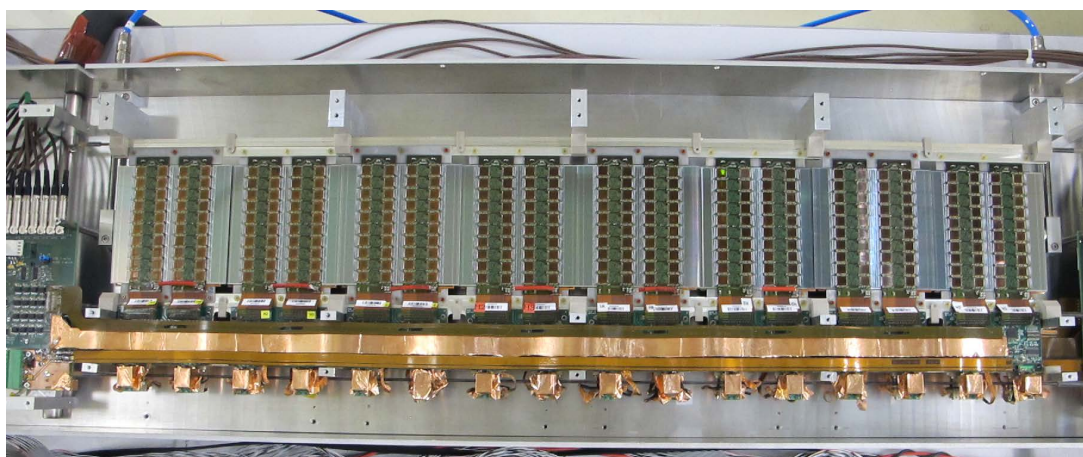
3   The super-module electrical prototype

Based on the double-sided strip module (DSM) concept explained previously, a super-module (SM) electrical prototype has been developed, aimed to demonstrate the feasibility of this tracker design for the HL-LHC and its validity even at the prototype stage. Although the different components are in most cases first prototype versions subject to further future developments, it is important to demonstrate a common readout in a multi-module setup. The identification of the possible issues or drawbacks while assessing the electrical response of such a large system will be helpful to improve future prototypes for an optimum performance. A realistic local-support structure, optimized in terms of component integration, material budget and thermo-mechanical performance (based on detailed FEA simulations), has been developed separately [18].

Several DSMs have already been constructed by the University of Geneva (Switzerland) and KEK (Japan) in a joint R&D programme. Eight of these modules have been installed in the SM electrical prototype, as shown in figure 7. The overall support structure is made in aluminium, with inlets and manifolds for both liquid cooling and dry-air flushing. During operation, the boxed-frame remains closed in all sides to ensure a light-tight environment and minimum relative humidity inside ($\sim$5%). The heat generated from the front-end electronics and the detectors is transferred to the cooling pipes running along the lateral sides of the structure. The silicon modules are mounted with alternating sides and overlapping along the SM-length, emulating a longitudinal overlap along the Z-direction (beam-axis direction) of the mechanical SM structure. The signals required to control the ASICs and the high-voltage lines needed to bias the sensors are driven through dedicated multi-layer service buses (see section 3.1). The digital low-voltage required to power the read-
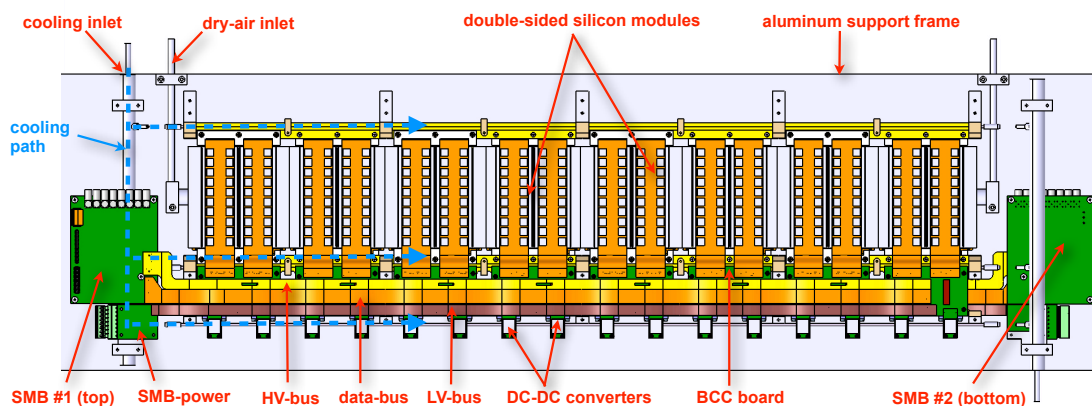
(a)

(b)

Figure 7. (a) Components of the super-module electrical prototype. Only the top-side is shown. The same components (SMB, service buses, BCCs and DC-DC converters) are installed on the bottom side. (b) Photograph of the super-module with eight double-sided modules installed. The total length of the aluminium boxed-frame is ∼110 cm.

out ASICs is provided by prototype DC-DC converters (see section 3.2). The analog voltage for the front-ends is obtained from the digital voltage via the ABCN25 on-chip linear voltage regulators. For each hybrid, a dedicated Buffer-Control-Chip (BCC, see section 3.3) multiplexes the data-signals coming from the two columns of ten ABCN-25 chips into a single data-stream. A Super-Module-Board (SMB, see section 3.4) not only receives each multiplexed data-stream coming from up to 16 BCCs and interfaces them to the external Data Acquisition (DAQ) system (see section 3.6), but it also provides the interface between the different voltage buses and the external power supplies.

3.1 Service buses

The electrical SM comprises two identical sets of a first version prototype service buses (one set is located on each side of the SM). These are ∼765 mm long double copper-layer flexes designed

Table 1. Parameters of the service buses. Thicknesses and widths are given in mm. [†]Data bus trace widths (mm): 0.10 (point-to-point), 0.12 (multi-drop) and 0.20 (rest). [*]LV bus trace widths (mm): 6.8 (10–12 V), 2.2 (3.3 V) and 9.5 (GND).

	HV	Data	LV
Total number of layers	2	2	2
Total number of traces:			
• Layer 1	8	28	2
• Layer 2	8	28	1
Trace width	0.2	0.1 - 0.2[†]	2.2 - 9.5[*]
Cu-layer thickness	0.035	0.035	0.2
Minimum / Maximum bus width	9.6 / 22.3	16.0 / 26.0	10.0 / 10.0

and produced at CERN. Each set is composed of a *High-Voltage (HV) bus*, a *Data bus* and a *Low-Voltage (LV) bus*. The main parameters of the buses are listed in table 1. In most cases, the top layer contains a certain number of traces for the signals and the bottom copper (Cu) layer is usually used as a common ground plane for the given bus. The distance between the two layers is 200 μm.

- The *HV bus* drives the HV supply and return lines for up to 8 silicon sensors.

- The *LV bus* drives the 10–12 V voltage required to operate the DC-DC converters, and the 3.3 V supply for the different components of the BCC board. The 10 mm-wide and 200 μm thick LV bus Cu bottom-plane is a ground plane common to the 10–12 V and 3.3 V supplies, able to stand a maximum current of ∼16 A.

- The *Data bus* has 16 Low Voltage Differential Signaling (LVDS) pair lines (2 per module side, one for each hybrid for the two-column multiplexed data stream) connected point-to-point from each BCC board to the SMB, and three multi-drop LVDS lines from the SMB to each BCC board (for clock and command signals). The widths of the LVDS traces (100 and 120 μm respectively for the point-to-point and the multidrop traces) have been optimized from simulations with Cadence OrCAD Signal Explorer [19] in order to achieve a line impedance of 120 Ω, being the termination resistor of 100 Ω (best results in terms of maximum signal amplitude and minimum reflections). Additional lines (200 μm wide) include a 1-wire bus, the reference voltage for the thermistor located in each hybrid and the corresponding voltage (i.e. temperature) return line.

Both the HV and data-buses are connected to one SMB board via Samtec connectors. Due to the high-current load, the two large traces of the LV-bus are directly soldered to a simple PCB (so called SMB-power board as shown in figure 7).

3.2 DC-DC power converters

The prototype DC-DC power converter used in the electrical SM is the SM01C module developed at CERN [20]. It is a low noise plug-in converter module (see figure 8) based on a buck con-

Figure 8. SM01C DC-DC converter without (left) and with (right) its polyethylene shielding box.
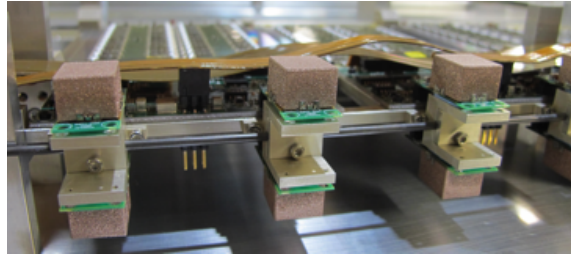

Figure 9. Photograph of several DC-DC converters already mounted in the SM over support-brackets. The cooling circuit, running along the lateral side of the SM frame and going through the interface between top and bottom brackets, is visible.

troller ASIC, and containing a coreless (air-core) toroidal inductor to store the energy in the form of a magnetic field, and to be compatible with the magnetic environment within the tracker. The converter operates with an input voltage of 10–12 V and provides a regulated 2.5 V with a maximum current of 5 A and a nominal conversion efficiency of ∼80% [20], enough to power a fully populated hybrid with 20 ABCN-25 readout ASICs. While the DC-DC converter provides the digital voltage needed to operate the DSM readout chips, the analog voltage for the FE is produced internally by the ABCN-25 on-chip voltage regulator.

In order to limit the effect of electromagnetic emissions from the converter, a polyethylene (PE) shielding box with a 10 μm coated Cu-layer is used (see figure 8, right). The coated PE box was measured to provide an effective shielding effectiveness similar to the one obtained with the baseline shield assembly (35 μm copper foil box), resulting in a magnetic field attenuation of ∼32 dB [20].

The converters are mounted over L-shaped aluminium support-brackets attached to the SM frame. An insulating thermally conducting sheet is placed in between each bracket and the corresponding converter backplane to optimize the heat flow. A cooling circuit runs through the interface between all support-brackets (see figure 9).

3.3 Buffer Control Chip (BCC) board

The BCC board (see figure 10) is a 80×48 mm^2 PCB that serves as the interface between the hybrids and the service buses. It contains two Buffer Control Chip (BCC) ASICs (one per hybrid), packaged in a 7×7 mm^2 LLP48 (Lead-less Lead-frame Package). The BCC is a dedicated ASIC produced by TSMC [21] in a 250 nm technology. Its purpose, limited to prototype studies only, is
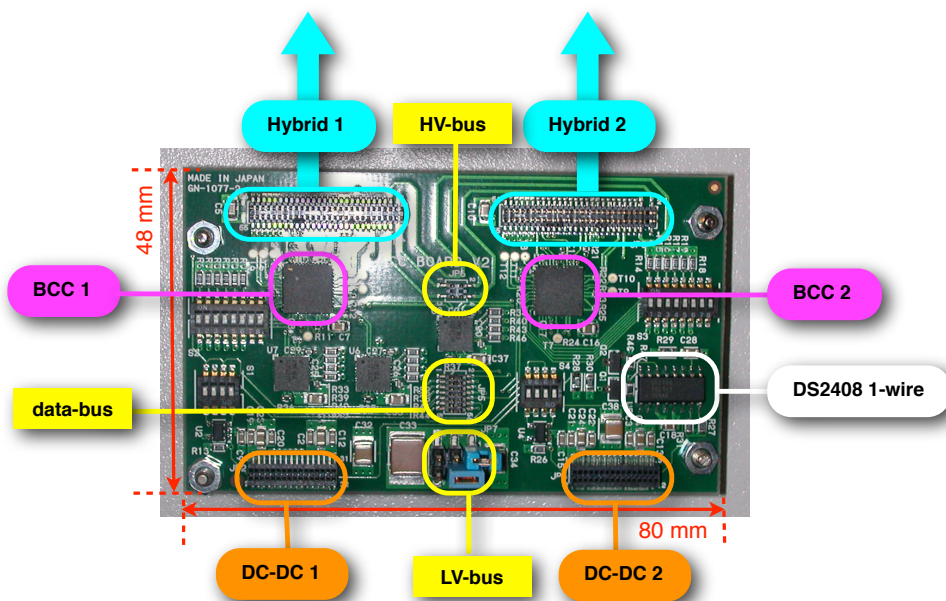
Figure 10. The BCC board, serving for the control and readout of two hybrids. It contains two LLP48-packaged BCC ASICs.

two-fold: multiplexing the data coming from the two columns of ten ABCN-25 ASICs into a single data stream and providing an 80 MHz readout clock through a clock-multiplication circuitry.

The BCC chip receives three LVDS input signals through the multi-drop lines of the Data bus: the main 40 MHz Bunch-Crossing clock, the Command line and the L1R[5] line. Before being distributed to each BCC chip, the clock and command signals pass through LVDS drivers-repeaters (implemented on the BCC board) for an optimum signal quality. Upon reception of a L1 trigger, the readout sequence of the ABCN-25 chips starts sequentially, using a token-passing mechanism for the data transmission. The data coming from each of the two columns of ten ABCN-25 chips is multiplexed by the BCC into a single data-stream at twice the readout clock (maximum rate of 160 Mbps). The multiplexed stream is then transmitted towards the SMB board via the corresponding point-to-point line of the Data bus. The address of each BCC chip is uniquely set via a DIP switch.

The BCC board also implements the required connections for the plugin DC-DC power converters. A DS2408 1-wire chip is used to monitor and control the state line (enable / disable) of each individual DC-DC module through a custom LabVIEW [22] application. A low-power comparator is used to implement a logic circuit that automatically disables the DC-DC converters if the hybrid temperature (as measured with a thermistor located in each hybrid flex) is above a given threshold.

3.4   Super-Module board (SMB)

The Super-Module board (SMB) interfaces the off-detector high and low-voltage power lines and external clock and control signals to the service-buses. A single SMB (see figure 11) serves one side of the SM prototype, i.e., a single-side of up to 8 DSMs.

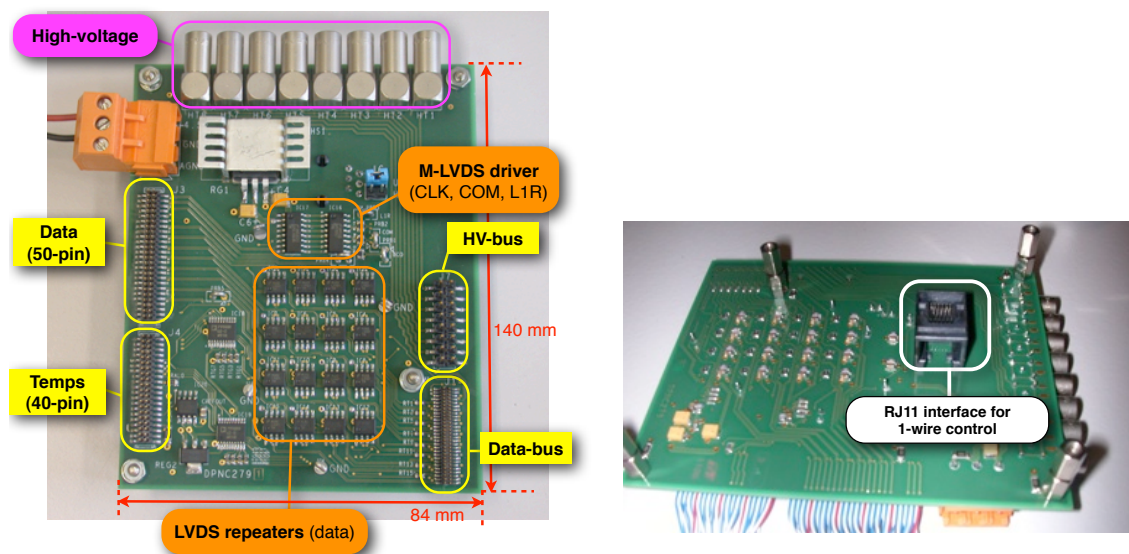[5]A multiplexed signal containing both the L1 trigger and the RESET signals.

Figure 11. The Super-Module board (SMB). The top and bottom-sides of the SMB are shown in the left and right images respectively.

The board contains eight LEMO connectors to drive the HV for the sensor bias. The control and data LVDS signals are interfaced to the external DAQ through 0.050" 40/50-pins connectors. The board implements 16 LVDS buffers, one for each data-line connected point-to-point from each BCC-board to the SMB. Three M-LVDS drivers are used for the multi-drop LVDS signals. The adoption of the M-LVDS driver was motivated by the observed improvement in the quality of the multi-drop signal along the data-bus if compared with standard LVDS repeaters. An RJ11 interface located in the backplane of the SMB is directly connected to the control PC via an iButton USB-bridge [23] to control the 1-Wire® network.

3.5 Power supplies

For the HV power-supply (PS), an ISeg ECH224 [24] crate equipped with two 6U Eurocard format 8-channel HV-modules (EHS-8210n-F) is used. Each HV-module provides 8 independent output channels with controllable voltage and current control. The HV output per channel is made through isolated built-in SHV connectors, adapted to LEMO format connecting to the SMB. A CAN-to-USB interface from *PEAK System* [25] provides one high-speed CAN channel for the control through an external PC via a USB port. A custom LabVIEW application implements the communication with the hardware and is used to monitor the status of the HV-modules and to perform I-V measurements.

The 10–12 V common input line for the DC-DC converters is provided by a commercial TDK-Lambda Genesys power supply [26], a source able to deliver a constant output voltage up to 20 V with a maximum current of 76 A. The PS features voltage protection levels (over and under-voltage limits), an embedded microprocessor controller and voltage (and current) high resolution adjustment by digital encoders. The output load wires are connected to the PS rear panel bus-bars through screwed terminal lugs and routed to a home-made power distribution board with two separated outputs (one for each of the two LV-buses).
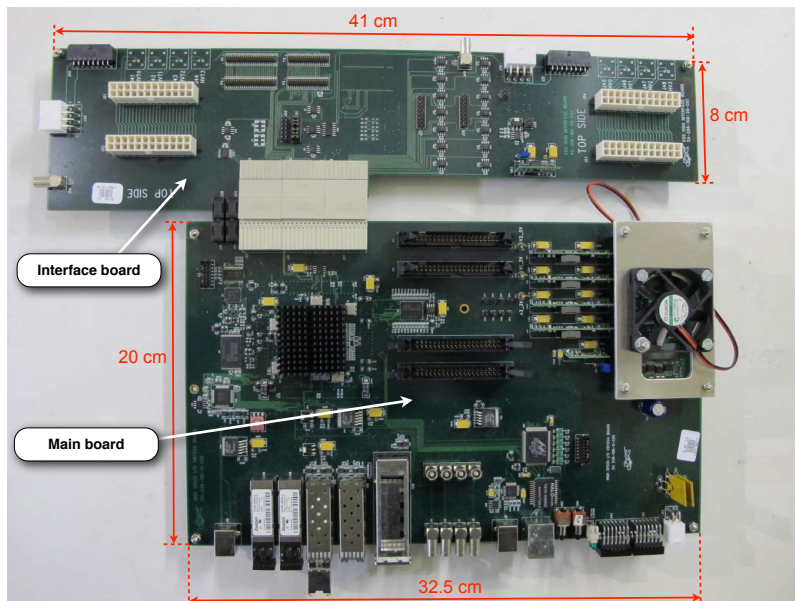
Figure 12. The HSIO main board ($32.5 \times 20 \, \text{cm}^2$) together with its interface card ($41 \times 8 \, \text{cm}^2$).

3.6 Data Acquisition System

The Data Acquisition System (DAQ) used for the results presented in this paper is the so-called High Speed Input Output (HSIO), a generic DAQ developed at SLAC to provide signal processing capabilities for various silicon tracking upgrade projects (Pixel and Strips) in ATLAS. The HSIO DAQ (see figure 12) is composed of a generic main board implementing a Xilinx Virtex 4 Field Programmable Gate Array (FPGA) for data acquisition and processing, and of an Interface Card (Rear Transition Module in the ATCA standard) containing the specific connectors and buffering to interface to the FE electronics via the two SMB boards. Several NIM I/O ports allow to monitor the state of specific LVDS lines, and ADCs are used for the readout of the hybrid thermistors. The analysis software is based on the SCTDAQ package [27], a set of C++ routines and libraries interfaced to the ROOT analysis framework [28] developed in the past for the electrical tests of the current ATLAS SCT modules.

The HSIO system implements 32 MB DDR SDRAM, several standard network connections (RJ45, Giga-Ethernet, SFP, XFP) and USB interface chips. For the communication with the control PC, a small form-factor pluggable (SFP) transceiver module is used with an Ethernet networking cable. The network interface uses raw Ethernet protocol without any UDP or TCP/IP layers on top.

4 Electrical performance

4.1 Leakage current

The IV characteristics of the silicon sensors are measured at different stages of the module assembly process. Figure 13 shows typical IV-curves of one double-sided module prototype. The leakage current is measured as a function of the reverse bias voltage, with probe-needles before bonding and through a dedicated PCB once the module has been completed. The current specification, set
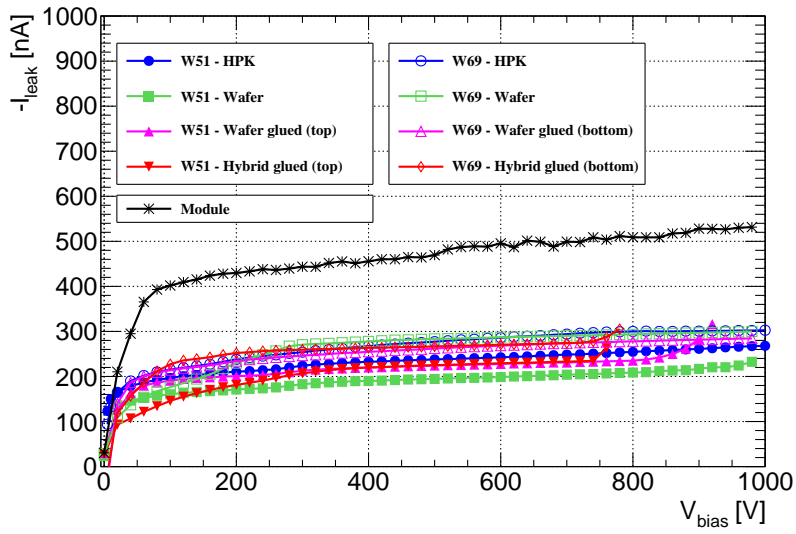
Figure 13. IV characteristics at different stages of the assembly of a typical module (silicon wafers W51 and W69 were used for the top and bottom sides respectively). The leakage current of the module is the sum of that of both sensors.
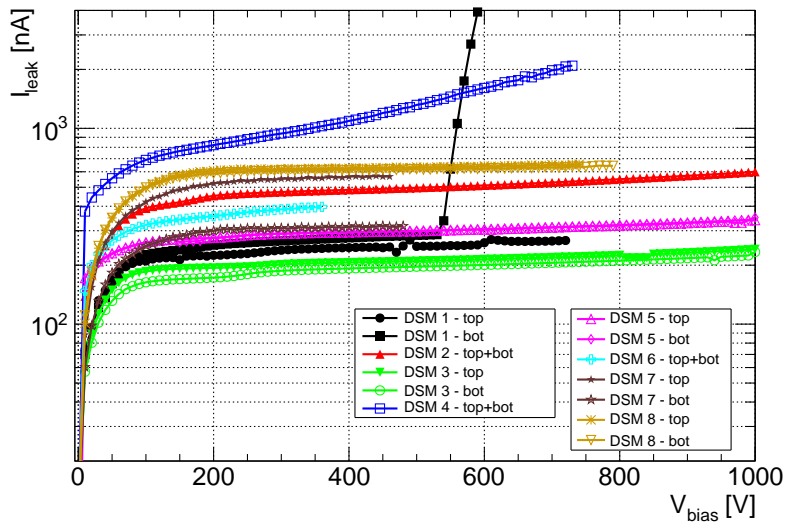

Figure 14. IV characteristics of all eight double-sided modules installed into the SM protoype.

with large margin, is that the leakage current must not exceed $200\,\mu A$ for a bias voltage of $600\,V$ ($20\,°C$). The results for the bare sensors are in good agreement with the measurements performed by the fabricant [8], all of them well below the current limit. No significant increase of current is observed after gluing the sensor to the baseboard.

Figure 14 shows the IV characteristics of all eight double-sided modules after being installed into the SM electrical prototype. The high-voltage is driven by the HV-bus through the SMB cards. In some cases an electrical coupling is observed between both sensors of the same module, the source of which could not yet be identified. As mentioned in section 2.4, the TPG baseboard is

Figure 15. R&S® HZ-14 probe set (left) and operating principle of the field-measurement (right).

coated with a thin Parylene coating with an additional glue/air matrix layer for electrical insulation. Although having local defects (pin-holes) that could create electrical insulation weaknesses can not be excluded (e.g. due to some surface damage handling or encapsulated carbon debris), that possibility is thought to be unlikely. In any case, a common bias of the two sensors does not represent an issue for the module electrical performance.

In future module designs, several possibilities are currently being investigated, *e.g* increasing the thickness of the Parylene coating, combining the HV supply to both sensors of the same module or even several sensors from different modules (in order to further reduce the number of required HV-lines).

4.2 Study of electromagnetic interference emissions

Since the SM prototype remains a complex system with many electrical components susceptible to transmit externally generated noise, it remains of particular importance to minimize the electromagnetic interference (EMI) from the High-Frequency (HF) emissions from both the surrounding equipment and the DC-DC power converters in the system under test. Several measurements have been performed with a ZVL-6 Rohde & Schwarz [29] (R&S) analyzer, together with the R&S®HZ-14 probe set (see figure 15, left) for electric and magnetic near-field measurements. The H-field passive probe used covers the frequency range 9 kHz to 30 MHz. It has a directivity loop antenna and it is electrically shielded so that capacitive coupling is suppressed and the electric fields are rejected. The omnidirectional capacitively coupled active E-field probe covers the entire frequency range.

The principle of the measurement of the magnetic field is sketched in figure 15 (right). A time-varying current in the conductor under test will cause a small amount of power to be radiated, the power being proportional to the current and the dimensions of the conductor itself. The radiated magnetic field (H) passing though the end-face of the probe generates a voltage at the probe output. The voltage is proportional to the change of magnetic flux though the circuit loop, thus allowing to measure the component of the field that is perpendicular to the probe end-face. An average antenna-factor has been used for the range of frequencies of interest (between 1 and 10 MHz).

Radiations from the DC-DC power converters. The SM01C DC-DC power converter comprises an air-core toroidal inductor to store the energy. Although most of the field is well confined
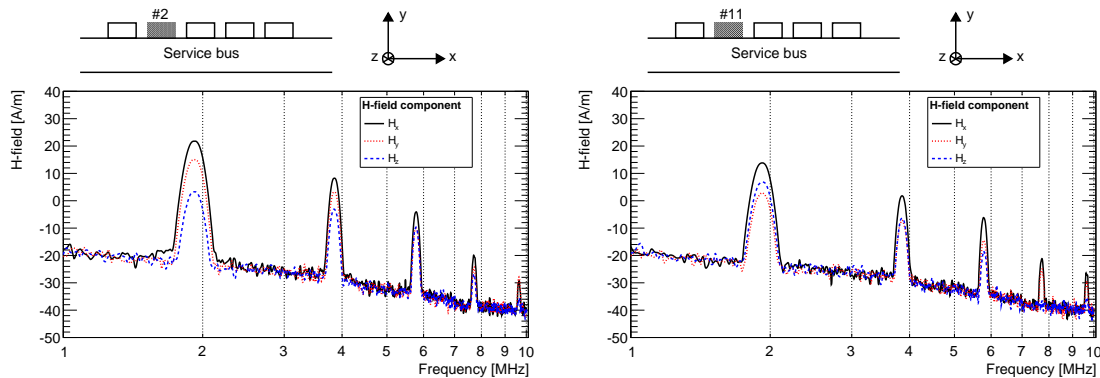
Figure 16. Components of the $\vec{H}$-field as a function of frequency as measured on top of two DC-DC power converters (each with its shielding box). DC-DC #2 and #11 ae shown on the left and right plots, respectively. In each case, the the top schema shows the definition of the coordinate system (the *z*-axis points inwards, perpendicularly to the plane of the page).

within the coil volume, there is a parasitic magnetic field emitted through the central hole of the toroid [30] (equivalent to a single-turn coil of diameter equal to the central toroidal hole). The shielding-box around the toroid allows to efficiently reduce the radiated emissions without affecting the inductance. Figure 16 shows the three components of the $\vec{H}$ field as a function of frequency as measured on top of two random DC-DC converters. The orientation of the probe was changed to measure qualitatively the different components of the $\vec{H}$-field. As expected, the field peaks at every harmonic of the 2 MHz carrier of the DC-DC converter.

Figure 17 shows for all DC-DC power converters the three different components of the *H*-field and the total magnitude $|\vec{H}| = \sqrt{H_x^2 + H_y^2 + H_z^2}$ as measured as the amplitude of the first harmonic peak ($\sim$2 MHz).

Two different configurations are compared to check the effect of surrounding converters: all 16 converters of either the top or bottom-sides of the Super-Module (SM) enabled, and all 32 converters enabled. Although no conclusive statement can be raised with respect to the dominant field-component, as both the orientation of the air-core toroid inside each DC-DC converter[6] and the orientation of the probe itself[7] have a direct impact in the measurements, it can be seen that some DC-DC power converters have a stronger emission than others. In general the H_x and H_y components are higher than H_z. There are no significant changes in the radiated fields when all 32 converters are enabled, if compared with the case when 16 converters are enabled.

Common-mode conducted noise. Due to the compact topology of the service buses it was not possible to measure the individual contribution of each DC-DC power converter in the SM except by modifying the LV-bus. Figure 18 shows the overall common-mode conducted noise from the TDK-Lambda power-supply (PS) used to provide the 10–12 V input line required by DC-DC power converters. The measurement is performed at the input of the SM with a common-mode

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[6]Every inductor in the DC-DC power converter can have a slightly different tilting angle with respect to its supporting PCB (see figure 8a).

[7]Despite the authors took care of always trying to achieve the same spatial orientation of the probe, a small deviation with respect to any of the three directions can lead to a non-maximal coupling of the field.
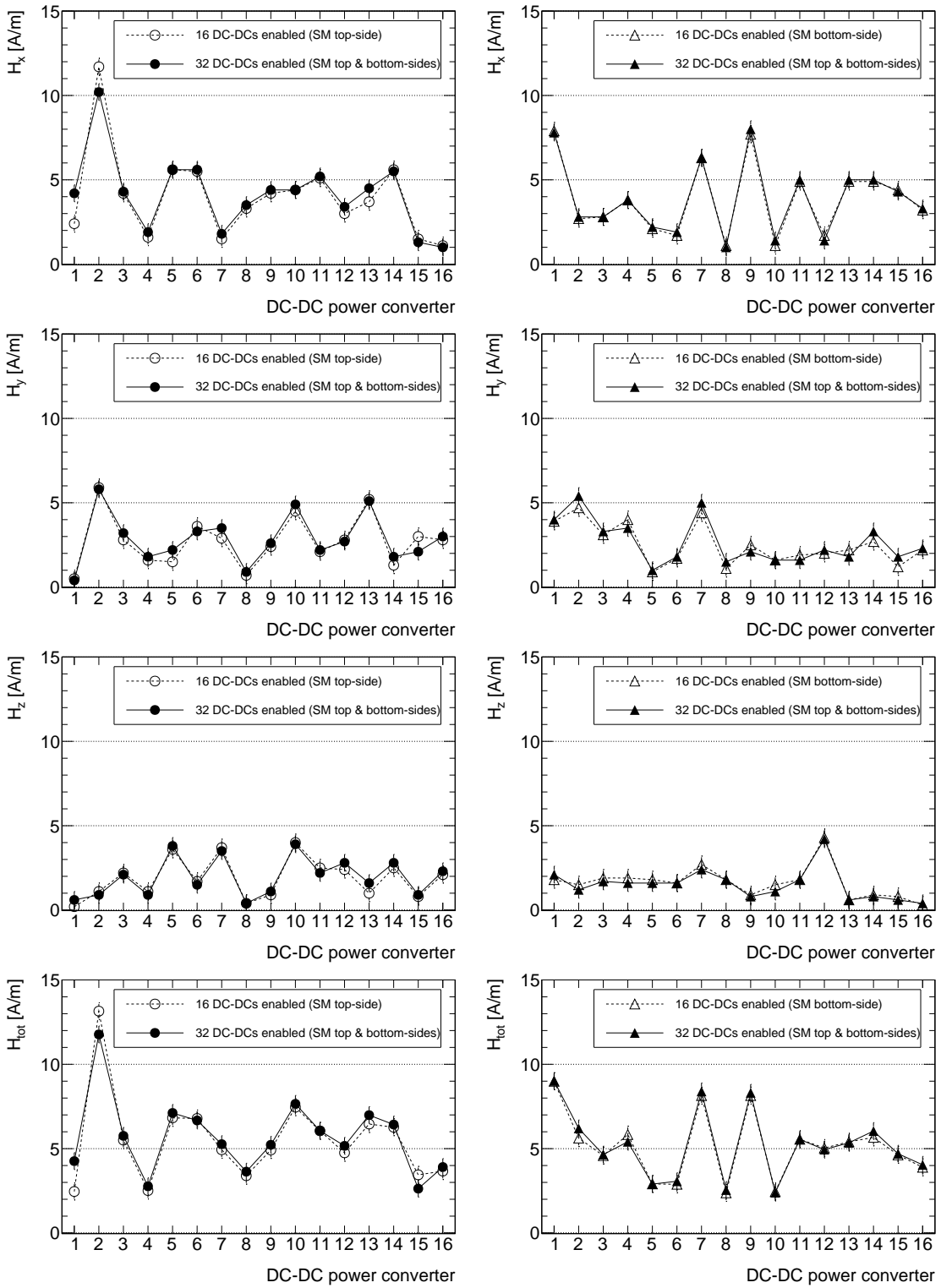
Figure 17. Amplitude for all DC-DC power converters of the different components of the $\vec{H}$-field, H_x (top), H_y (middle-top) and H_z (middle-bottom), as measured at the first harmonic-peak. The magnitude of the total field $|\vec{H}| = \sqrt{H_x^2 + H_y^2 + H_z^2}$ is shown in the bottom-plot. Two cases are compared: when all 16 DC-DC power converters (open markers) of a given SM-side are enabled (SM top and bottom-sides shown on the left and right hand-side plots, respectively), and when all 32 DC-DC power converters are enabled (filled-markers).

Table 2. Configurations used to study the common-mode conducted noise from the Low-Voltage Power-Supply (LV PS) used for the supply of the DC-DC power converters.

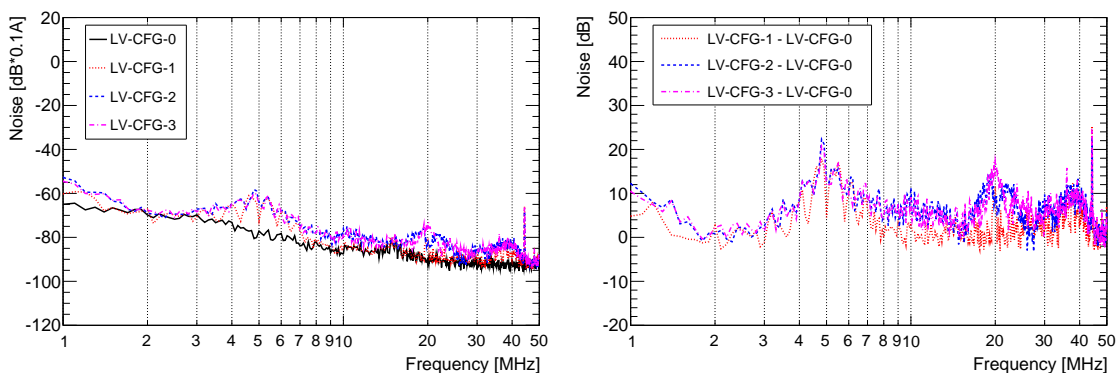| LV configuration	Description
LV-CFG-0	LV PS switched OFF
LV-CFG-1	LV PS switched ON, output OFF
LV-CFG-2	LV PS switched ON, output ON, all 32 DC-DC power converters disabled
LV-CFG-3	LV PS switched ON, output ON, all 32 DC-DC power converters enabled

Figure 18. Common mode conducted noise (left) from the LV PS used for the supply of the DC-DC power converters for different configurations (left) and difference of configurations LV-CFG-1 to LV-CFG-3 with respect to LV-CFG-0 (right). See table 2 for a description of the corresponding configurations.

current probe encircling all the LV wires entering into the SMB-power board. The four different configurations listed in table 2 are compared. A significant increase of the noise can be observed around 5 MHz just when the PS is switched-on (but still without driving any current, and the output switched-off). Several additional noisy peaks are visisble at ∼ 20 MHz and ∼45 MHz. Enabling the DC-DC power converters does not produce a noise increase, so the input-filter located in each DC-DC is found to be adequate in this respect.
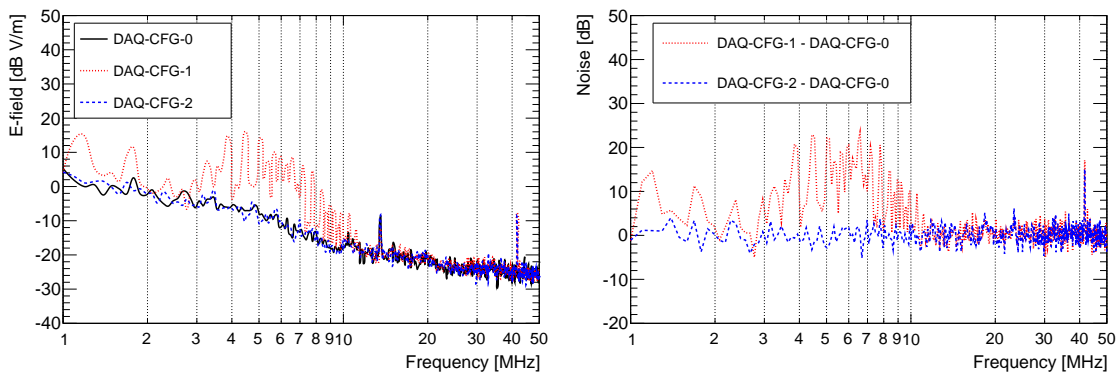
Electric field. Figure 19 shows the electric field as measured on a particular strip module flex hybrid, for different configurations of the HSIO DAQ as summarized in table 3. The main HSIO DAQ board contains some internal DC-DC front-end converters that appear quite noisy between 1 and 10 MHz. An external noise at ∼13.5 MHz, for which the source could not be identified, is also visible. When the DAQ is powered-on, a spike at ∼42 MHz is visible, corresponding to the 40 MHz data-bus clock signal. The measurements presented in the following sections were performed after by-passing the HSIO DAQ internal converters with an external laboratory-standard power-supply.

4.3 Principle of the front-end calibration

The electrical performance of the strip module is evaluated by analyzing the data coming from parameter scans. In a scan, a parameter is varied according to a defined range and step. The most commonly used is the *threshold scan*: the discriminator threshold is varied and a fixed calibration

Table 3. Configurations set to study the electric field on a particular flex hybrid.

DAQ configuration	Description
DAQ-CFG-0	HSIO DAQ switched OFF
DAQ-CFG-1	HSIO DAQ switched ON, internal 12 V converters
DAQ-CFG-2	HSIO DAQ switched ON, external 12 V supply

Figure 19. Electric field as measured in a strip-module flex hybrid for different DAQ configurations (left) and difference of configurations DAQ-CFG-1 and DAQ-CFG-2 with respect to DAQ-CFG-0 (right). See table 3 for a description of the corresponding configurations.

charge is sent many times at each threshold point. The hit occupancy (normalized count rate) is then determined as the fraction of input signal pulses exceeding the threshold. Although ideally the hit occupancy would follow a step function, in reality the distribution is smeared by the electronic noise. Figure 20 illustrates a threshold scan in which a calibration pulse is convoluted with a Gaussian-distributed electronic noise.

Assuming the input charge distribution is described by a Gaussian probability distribution function $f(x)$ of mean μ and variance σ^2, with x being the calibration signal amplitude, then the probability $p(\tau)$ that the signal is larger than a given threshold τ is:

$$p(\tau) = \int_\tau^\infty f(x)\,dx \propto \int_\tau^\infty \exp\left[-\frac{(x-\mu)^2}{2\sigma^2}\right] dx \propto \operatorname{erfc}\left(\frac{\tau-\mu}{\sqrt{2}\sigma}\right)$$

where erfc is the complementary error function. The resulting occupancy-versus-threshold curve is hence called an *s-curve*, as due to the characteristic S-shape of the erfc function. The threshold at which the occupancy is 50% is called the vt_{50} point, and it corresponds to the input charge amplitude (i.e. the mean value of the Gaussian distribution). The width of the distribution gives a measurement of the noise amplitude at the discriminator output. The threshold difference between the 16% and 84% hit occupancies corresponds to 2σ.

4.3.1 Calibration delay

The calibration of the FE of the ABCN-25 ASIC is performed by injecting test charges into the analog circuitry. Each of the 128 channels has an internal calibration capacitor connected to its in-
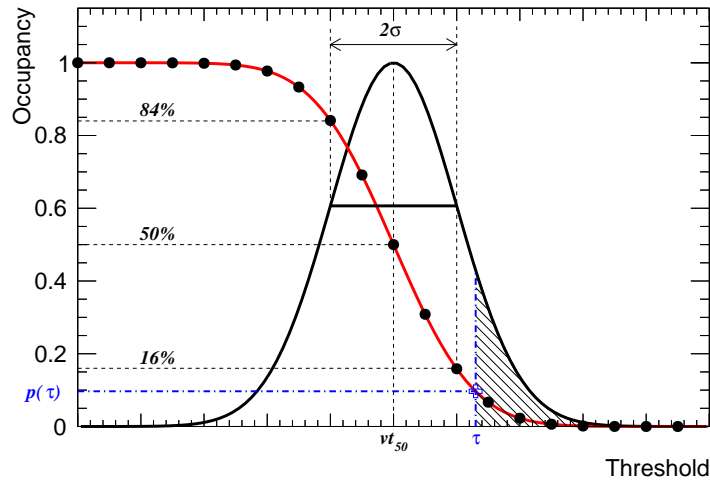
Figure 20. Illustration of threshold scan. The threshold is varied in steps and a calibration pulse is injected a certain number of times at each threshold point. The total input signal results from the convolution of the calibration pulse and some electronic noise that is described by a Gaussian distribution function. For a given threshold τ, the hit occupancy corresponds to the fraction of signals above the threshold (dashed area). vt_{50} is the threshold for which the occupancy is 50%.

put. A specific command triggers the generation of a pulse that simulates a hit in a strip (equivalent to the charge collected after the passage of a charged particle through the silicon sensor). Both the amplitude and the delay of the calibration pulse with respect to the clock phase (the relative delay of the rising edges) are controlled by a specific register (CalDelay) of the ABCN-25 ASIC. Within the chip there are a total of four calibration lines; every fourth strip is connected to same line, so that 32 channels can be tested simultaneously. The preamplifier-shaper circuit delivers a signal with a peaking time of 25 ns (including the effect of charge collection time), which is enough to ensure that the discriminator timewalk is less than 16 ns [13].

The optimization of the delay between the calibration charge and the clock is achieved by computing the channel occupancy for different settings of the CalDelay register. Figure 21 shows an example for a single channel. The optimum delay corresponds to the DAC value for which the sampling is done at the maximum of the signal (maximum occupancy at the plateau). A unique delay is set in a chip-basis corresponding to the mean of the distribution of the optimum delays for all channels within that chip.

4.3.2 Single channel threshold correction

The discriminator is used to discard signals with an amplitude not exceeding a given threshold. The threshold is common for all channels within the ABCN-25 ASIC, and it is set as a differential voltage adjustable by an internal DAC with 8-bit resolution. To compensate for channel-to-channel threshold variations (each channel has a particular offset of its discriminator with respect to the common chip threshold), a 5-bit DAC (TrimDAC) is used to set an individual threshold correction for each channel, guaranteeing uniformity across the chip. The TrimDAC has eight selectable voltage ranges, with 32 steps (or settings) available within a given range. It is expected that the
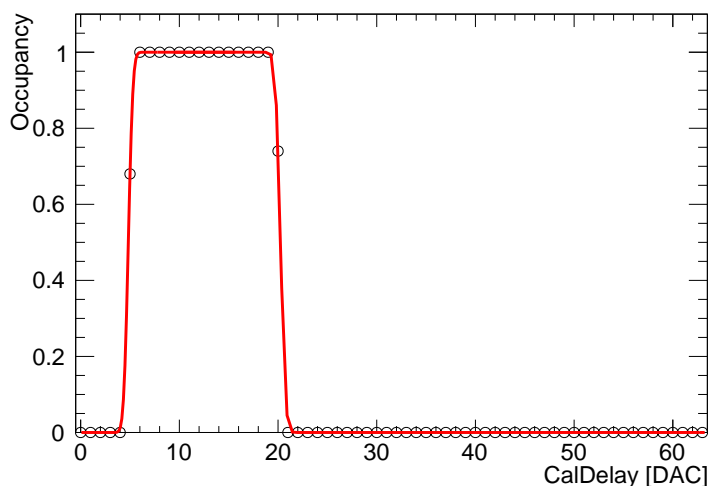
Figure 21. Occupancy as a function of the calibration delay setting (DAC units) for a single channel. Each DAC unit corresponds to 1 ns.

TrimDAC would be adjusted to higher ranges along the life of the experiment, to compensate for the increase of the offset spread induced by radiation damage to both detectors and electronics.

The trimming procedure aims to determine the individual channel threshold correction settings. For each channel and for all ranges, a fixed calibration charge is injected into the analog circuit and threshold scans are taken for different settings of the TrimDAC. The vt_{50} thresholds are extracted by fitting the s-curves and then a linear fit is performed to the vt_{50} versus trim-setting. For several threshold targets, the number of *trimmable* channels is computed. A channel is said to be trimmable if the setting that needs to be applied to correct for the offset with respect to the target lies in the available range of the DAC. Typically the target is chosen as the minimum value for which a maximum number of trimmable channels within a given column is found. Once the target selected, the individual channel threshold correction (*i.e*, a specific step of the TrimDAC for the selected range) is computed. Figure 22 shows a threshold scan for a column of ten chips before and after applying the trimming procedure. An excellent threshold uniformity is achieved after trimming. Figure 23 shows, for a particular chip, the resulting s-curves after projection of the occupancy to the threshold axis in the threshold-scan plot (Figure 22). Typically, the threshold spread is reduced from 7–8 mV to 1–2 mV after the trimming corrections are applied.

4.4 Gain and noise

The gain and noise at each strip-channel discriminator input can be determined by performing threshold scans for different input charges injected through the internal ABCN-25 FE calibration circuit. In the case of injecting three input charges (so-called *Three-Point-Gain* test), for each readout channel a linear fit is performed to the vt_{50} threshold points versus charge, so that the slope and intercept of the fit correspond respectively to the gain and threshold offset. As the readout chips produce a signal proportional to the input charge, the 50% threshold values increase with higher amplitudes of the calibration charge. The standard deviation of the s-curve is an effective measurement of the noise at the discriminator output for that charge. The input noise, typically
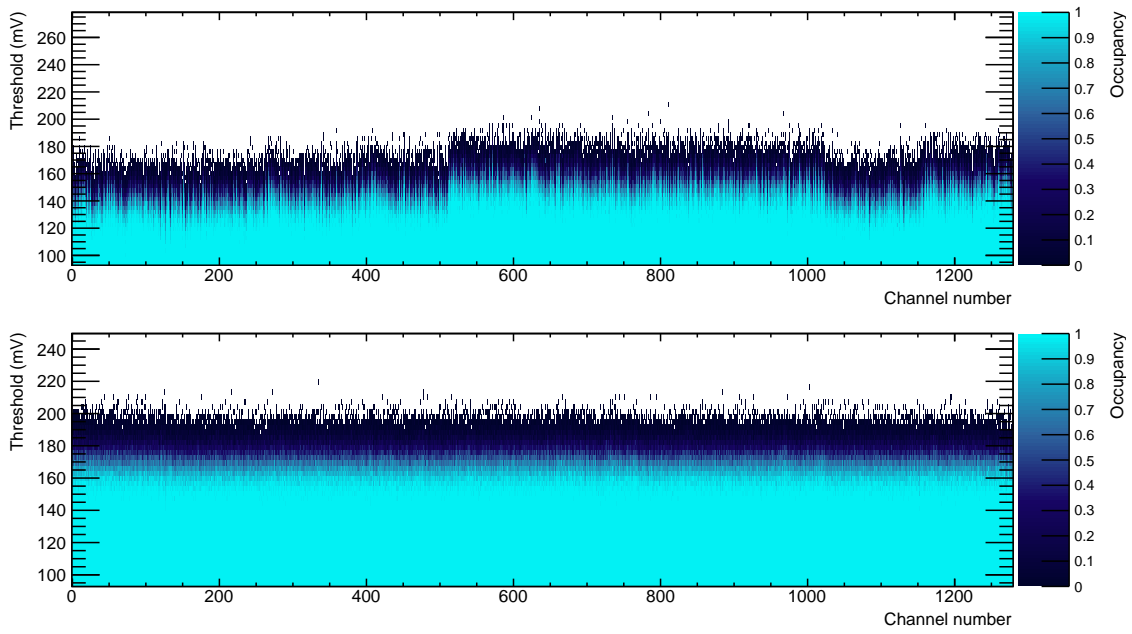
Figure 22. Threshold scan for 1 fC input charge for all 1280 channels of one column of ten chips, before (top) and after (bottom) trimming. The horizontal axis is the channel number, the left-vertical axis is the threshold [mV] and the right-vertical color-scale is the channel occupancy.
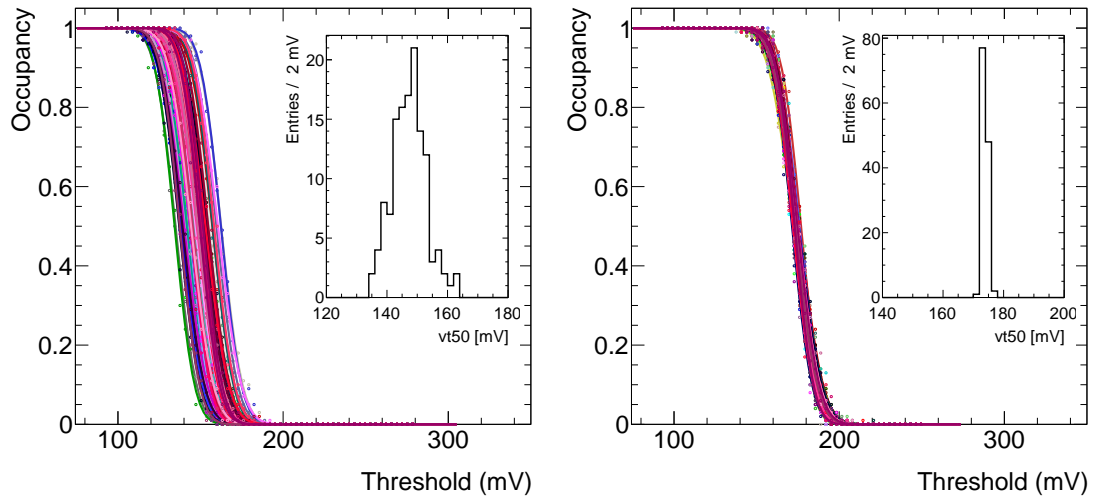

Figure 23. S-curves for all 128 channels of a chip before (left) and after (right) applying the individual channel threshold correction. The measurements correspond to a threshold scan for a 1 fC input charge. The data-points are fit to a complementary error function. In each case, the inset shows the distribution of the vt_{50} point obtained from the S-curves.

given in electrons Equivalent Noise Charge (ENC(e)), is simply calculated as the output noise divided by the amplifier gain. Figure 24 shows an example of the resulting distributions of gain, threshold offset, output noise and input noise for all channels within a single column of ten ABCN-

Table 4. Different operating configurations used to test the electrical Super-Module.

Run configuration	Description	# DC-DCs power converters enabled
RUN-CFG-0	- A single side of each module tested individually	2
RUN-CFG-1-top	- 8 module-sides (SM top-side) tested simultaneously - DC-DC power converters on opposite sides disabled	16
RUN-CFG-1-bot	- 8 module-sides (SM bottom-side) tested simultaneously - DC-DC power converters on opposite sides disabled	16
RUN-CFG-2	- 8 module-sides (SM top and bottom-sides) tested simultaneously - DC-DC power converters on opposite sides enabled	32

25 ASICs after trimming. The uniformity of gain and noise is very good. The average gain is in very good agreement with the nominal ABCN-25 design value of 100 mV/fC, and the input noise matches very well the expected $\sim$600 ENC(e) (from the current short-strip input capacitance).

Figure 25 shows the input noise as a function of temperature for two different hybrids. The chiller temperature was varied from 28 °C to -4 °C (in steps of 4 °C). Enough time was allowed to reach a steady thermal equilibrium. The temperature of each hybrid was measured via its corresponding thermistor. In each case, the input noise is obtained from a *Three-Point-Gain* test and it corresponds to the mean value of a Gaussian fit to the average of that of the two hybrid columns. The vertical error bar at each data point corresponds to the standard deviation of a Gaussian fit to the noise distribution for the corresponding hybrid. A linear fit indicates a small dependence of the noise with respect to the temperature, with a variation of $\sim$ 1.4 ENC(e) / °C. Similar results are obtained for other hybrids. As the maximum temperature variation accross hybrids is $\sim$15 °C, any temperature-dependence of the noise is well covered by the noise uncertainty (typically $\sim$25–30 ENC(e)), and no temperature-dependent correction was applied in subsequent tests.

Figure 26 shows the input noise as a function of the bias voltage of the sensors for all eight double-sided modules. In each case, results for the module top-side silicon sensor are shown. As expected, the noise is larger for low bias voltages, and decreases with increasing bias. A plateau is reached when full depletion is achieved ($\sim$200 V). Unless stated otherwise, the results shown in the following correspond to a sensor bias voltage of 250 V.

Figure 27 shows the average gain and input noise for all eight-modules installed in the SM prototype. Three different cases are compared as summarized in table 4. The results show that there is not a significant noise increase while comparing cases from RUN-CFG-0 and from RUN-CFG-1-top/bot, so that radiated fields from surrounding DC-DC converters have only a small impact on the sensors located *on the same side of the SM-prototype*. However, while testing 8 single-side modules with the DC-DC power converters of the opposite sides being enabled (RUN-CFG-2), the noise increases significantly, in the range of [$\sim$10 ENC(e); $\sim$60 ENC(e)]. The gain is consistent with the design values in all cases.

There is particular case (module 6) which presents a large noise increase that can't be correlated with any particularly noisy DC-DC converter. Therefore, while testing a large number of single-side modules does not cause any significant degradation in the noise performance of the
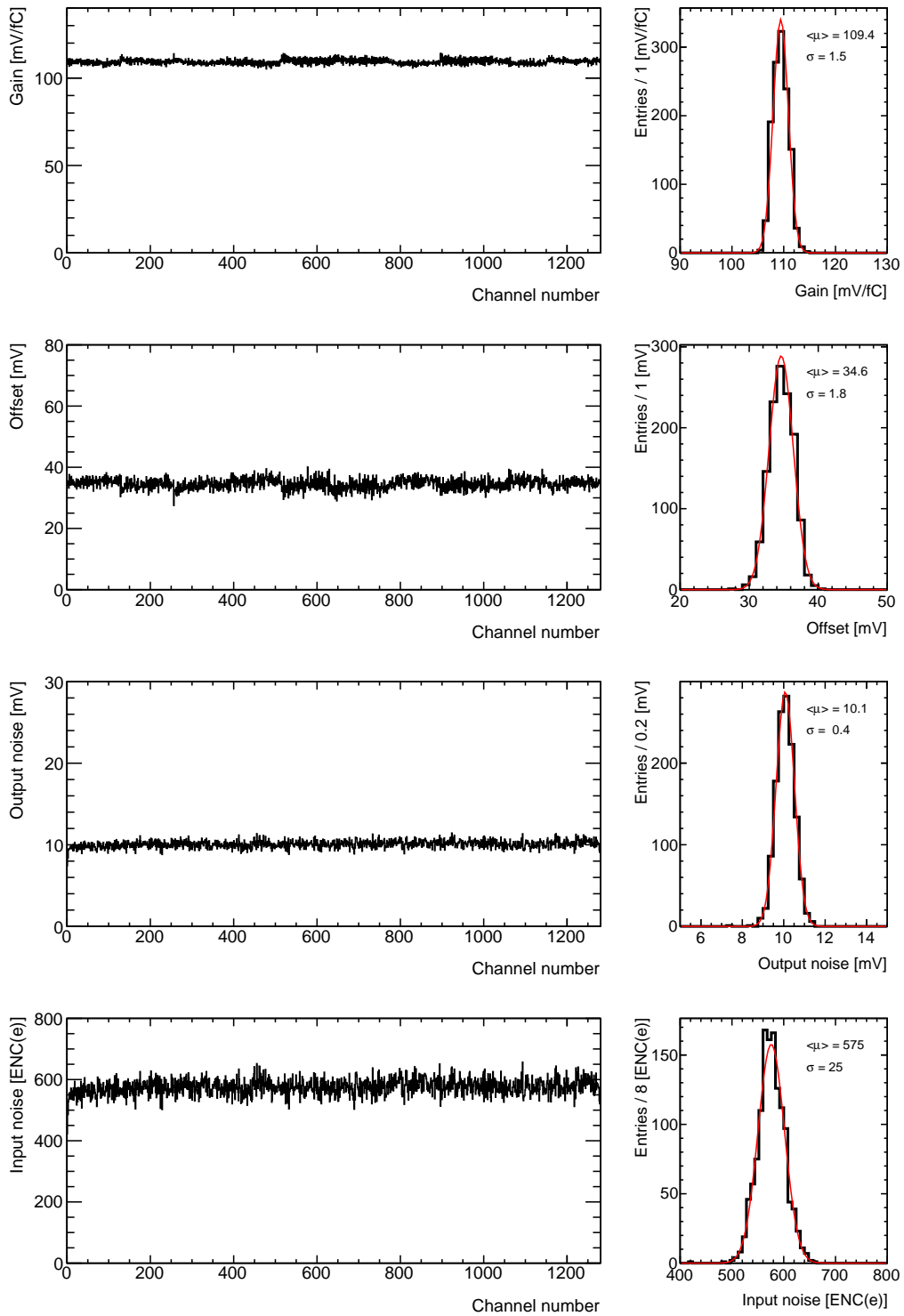
Figure 24. From top to bottom: distribution of gain, threshold offset, output noise and input noise as obtained from a *Three-Point-Gain* test for 0.5 fC, 0.75 fC and 1.0 fC input charges (see text for details). The left plots show the distributions as a function of all 1280 channels within a single hybrid column (ten readout ASICs). The right plots show the corresponding histograms. The mean $\langle \mu \rangle$ and sigma σ of a Guassian fit to the histogrammed distributions are also shown. The silicon sensor was biased at 250 V.
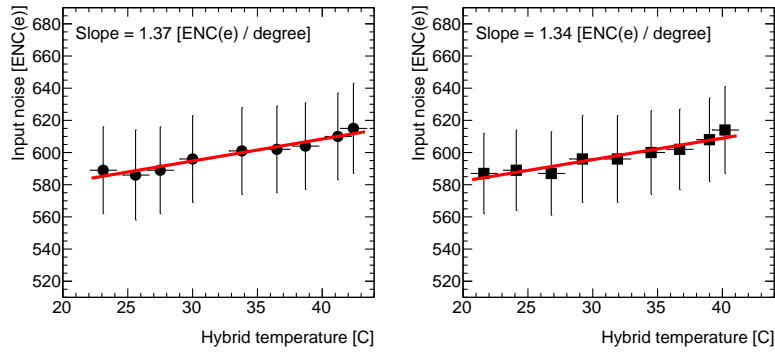
Figure 25. Input noise as a function of hybrid temperature, for two different hybrids. In each case, the average noise of the two chip columns is shown.
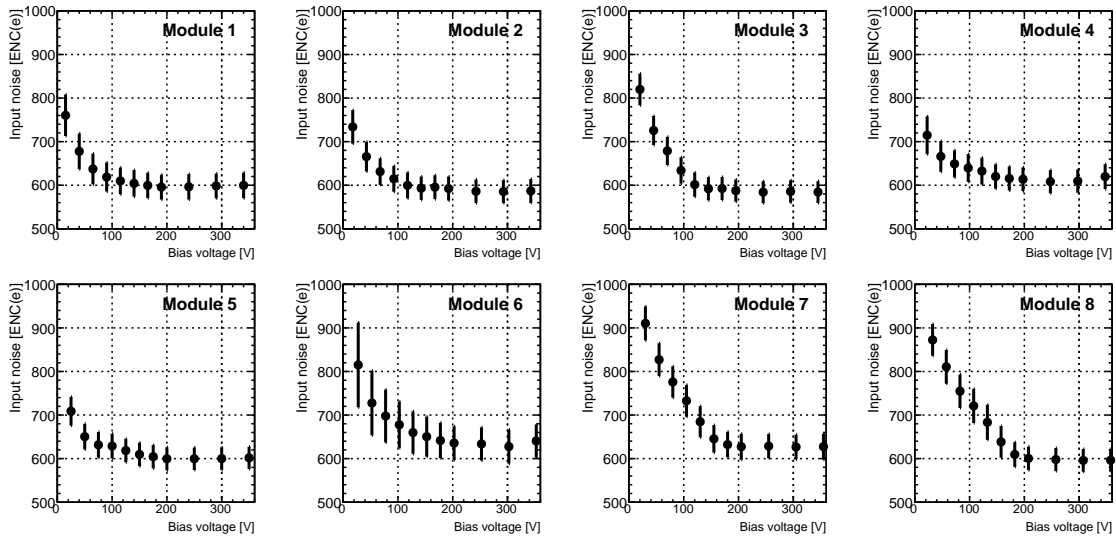
Figure 26. Input noise as a function of bias voltage for all eight modules (top-side sensor). In each case, the average noise of the two hybrids of the module top-side is shown.

system, there is a clear interplay between top and bottom-sides of the SM-prototype that requires further investigation.

4.5 Noise occupancy

The *noise occupancy* (NO) is defined as the probability for a strip to give a hit in a certain event only due to noise. The NO is determined by performing a threshold scan without any input charge being injected into the analog stage. The number of triggers sent is raised progressively with increasing thresholds. Figure 28 shows a typical threshold scan obtained from a NO test.

Figure 29 shows for all eight modules the projection to the treshold axis of a treshold scan obtained from a NO test. The configurations RUN-CFG-1-top/bot and RUN-CFG-2 as described in the previous section are compared. It is observed that in most cases there is not a significant increase in the noise occupancy when enabling all 32 DC-DC power converters (RUN-CFG-2). The threshold at which the hybrids are typically trimmed, and corresponding to 1 fC charge (this
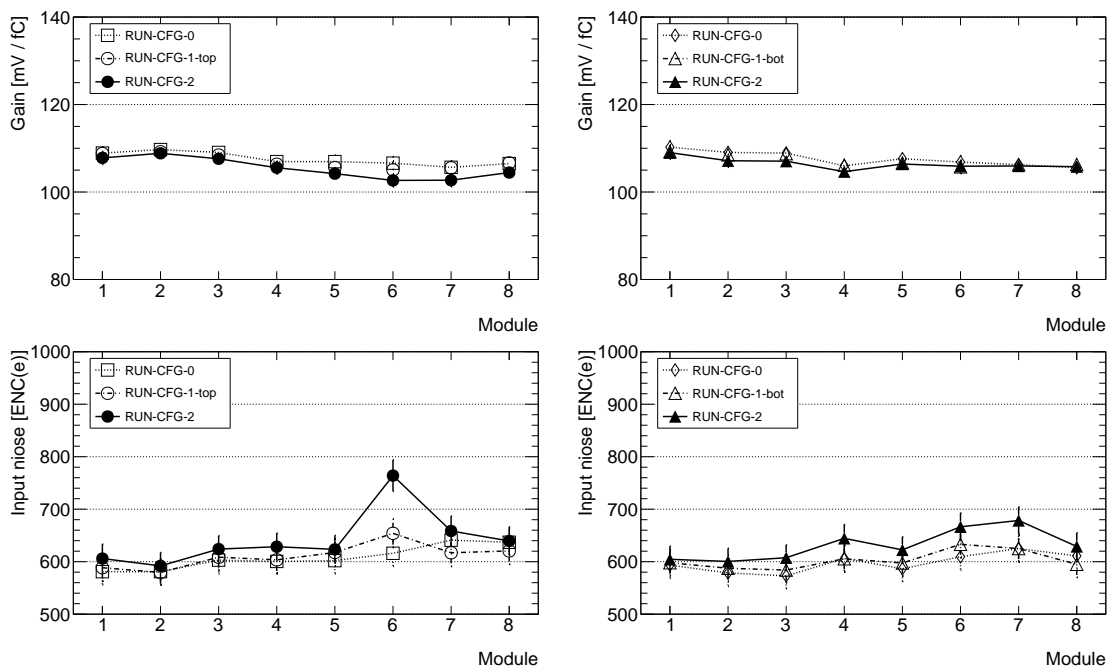
Figure 27. Gain (top) and input noise (bottom) for all eight strip-modules. See table 4 for the different configurations being compared. The vertical error bar at each data point corresponds to the standard deviation of a Gaussian fit to the noise distribution for the two hybrids of a given sensor.
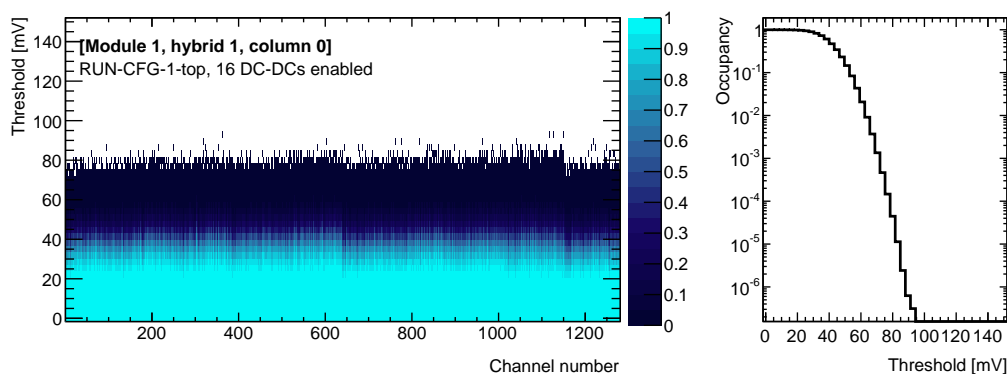

Figure 28. Threshold scan from a Noise Occupacy test (left) and projection to the threshold axis (right) for all channels of a column of ten chips of a given hybrid.

is the threshold at which unirradiated modules are expected to be operated in the future tracker), is ∼130–150 mV. The occupancies typically reach 10^{-8} around 100 mV (in the worst case scenario when all 32 DC-DC power converters converters are enabled). The bottom-side of module 7 shows a significant increase in the occupancy in RUN-CFG-2. Figure 30 shows the corresponding threshold scan for ten chips of a hybrid located in that side. A large common-mode noise can be clearly observed, probably originated from the coupled effect of the top and bottom-side DC-DC converters.
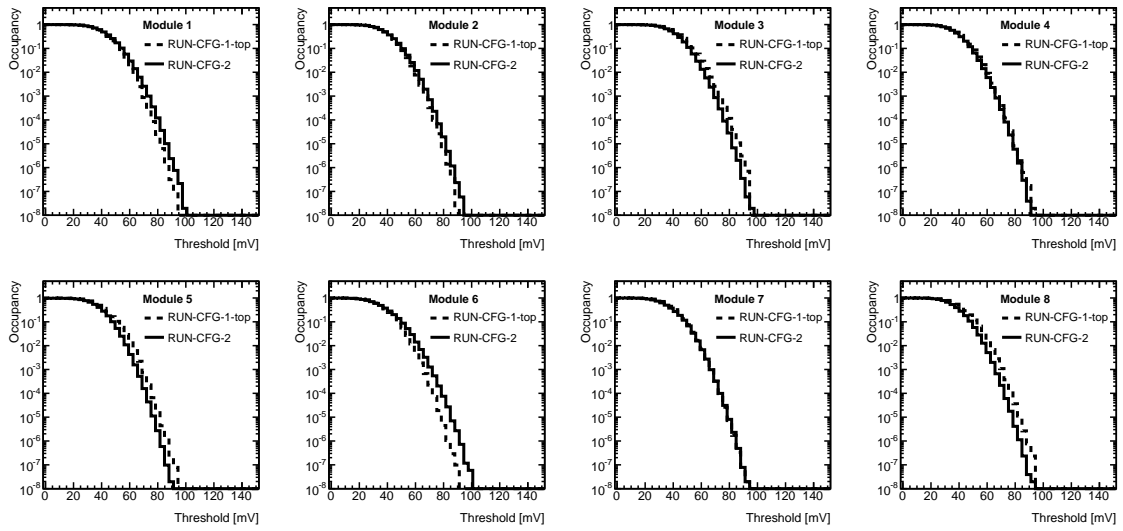
(a) Comparison of the NO as obtained with configurations RUN-CFG-1-top and RUN-CFG-2.
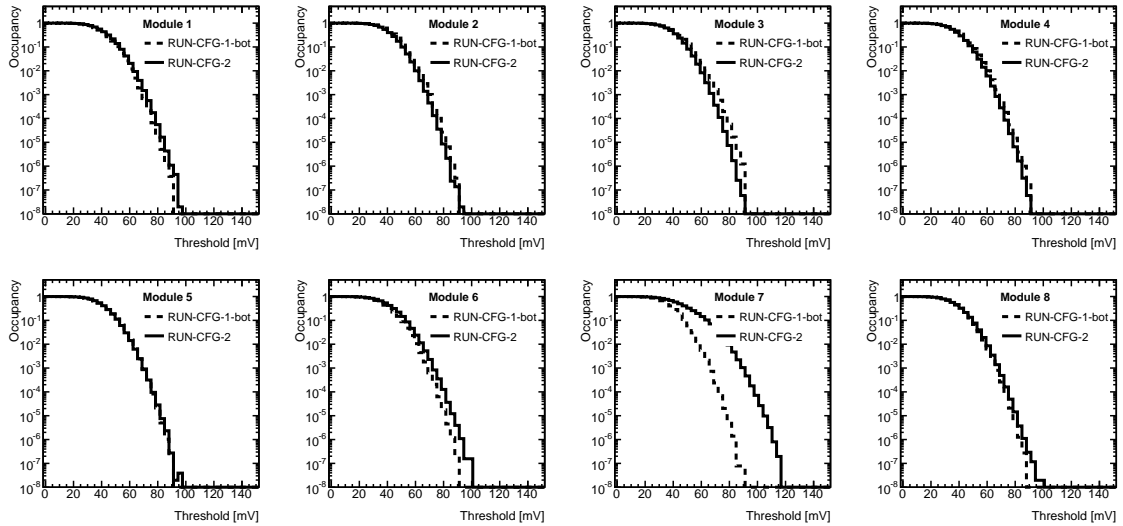
(b) Comparison of the NO as obtained with configurations RUN-CFG-1-bot and RUN-CFG-2.

Figure 29. Noise occupancy for all eight double-sided strip-modules. See table 4 for the different configurations being compared. For each module, the average occupancy of the two same-side hybrids is shown.

4.6   Double-trigger noise

During the aforementioned *Three-Point-Gain* test (section 4.4), the input noise is accurately determined from calibration charges injected into the analog FE with the ABCN-25 internal calibration circuit. The delay between the test charges and the clock is optimized to sample at the maximum of the signal. However, during real operating conditions of the tracker, the trigger is random and noise pick-up can occur for closely spaced triggers. In the so-called *Double-Trigger-Noise* (DTN) test, two triggers, separated by a specified number of clock periods are sent to the modules. The
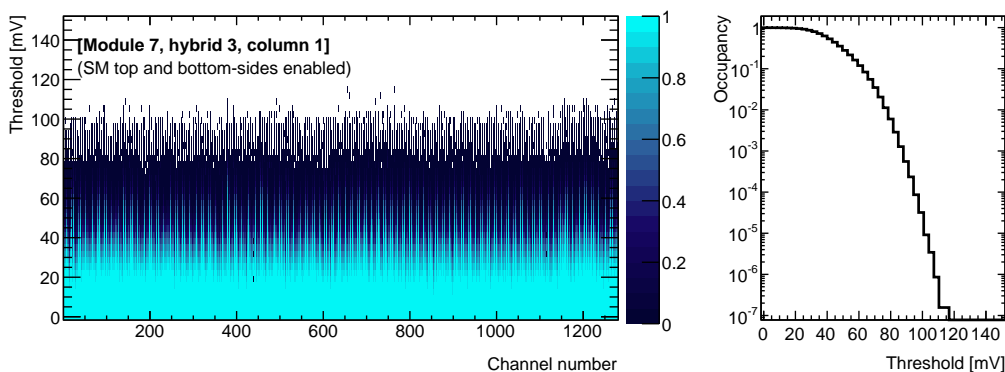
Figure 30. Threshold scan from a Noise Occupacy test (left) and projection to the threshold axis (right) for all channels of a column of ten chips of module 7, hybrid 3, column 0. During this test, all 32 DC-DC power converters were enabled.

first event is rejected and the second is being readout. For a spacing close or equal to the pipeline length, the second event records the occupancy of the module as the readout cycle of the first event starts [31].

Figure 31 shows the results of a DTN test for three different thresholds corresponding to 1.0 fC, 0.75 fC and 0.50 fC charges. The spacing between the two triggers was varied from 120 to 150 clock periods, centered around the pipeline length. In each case, the total number of hits recorded in the two hybrids of the corresponding module-side is shown. Ideally, as no charge is injected the total number of hits should be zero for all thresholds. This is the case for almost all modules for thresholds corresponding to 1 fC and 0.75 fC. However, for RUN-CFG-2 (32 DC-DC converters enabled) and a threshold corresponding to 0.50 fC, a large increase in the number of hits is observed, clearly indicating common-mode noise pick-up by the system. Figure 32 shows some particular examples for modules 1 and 6. In the case of module 7, the same common-mode pick-up as recorded during the NO test (see figure 30) was observed.

5   Prospects of a future module design

The results presented in the paper are from a module design based in the ABCN-25 readout ASIC. The total radiation length of the current prototype is 2.44% X_0, with a total estimated weight of 58.7 g [6]. For a hybrid fully populated (including SMD components and ASICs), the calculated radiation length is 0.33% X_0 with a total estimated weight of 7.1 g. A stuffed-hybrid with SMD components but without readout ASICs is estimated to weight 5.9 g. The measured weights of hybrids and modules agree with the calculations within 1% and 3% respectively. The two micro-strip sensors and the 80 ABCN-25 ASICs represent respectively 28% and 7% out of the total module material budget. The four stuffed hybrids (without ASICs, including passive components and the carbon-carbon bridges), correspond to 1.04% X_0, which is almost 43% of the total of the module. The TPG baseboard and the facings represent respectively 13% and 5% of the total material budget.

A new version of the ABCN chip, with 256 channels, has been submitted in 130 nm CMOS technology (so-called ABCN-13). A new module design is already in progress, mainly focused on
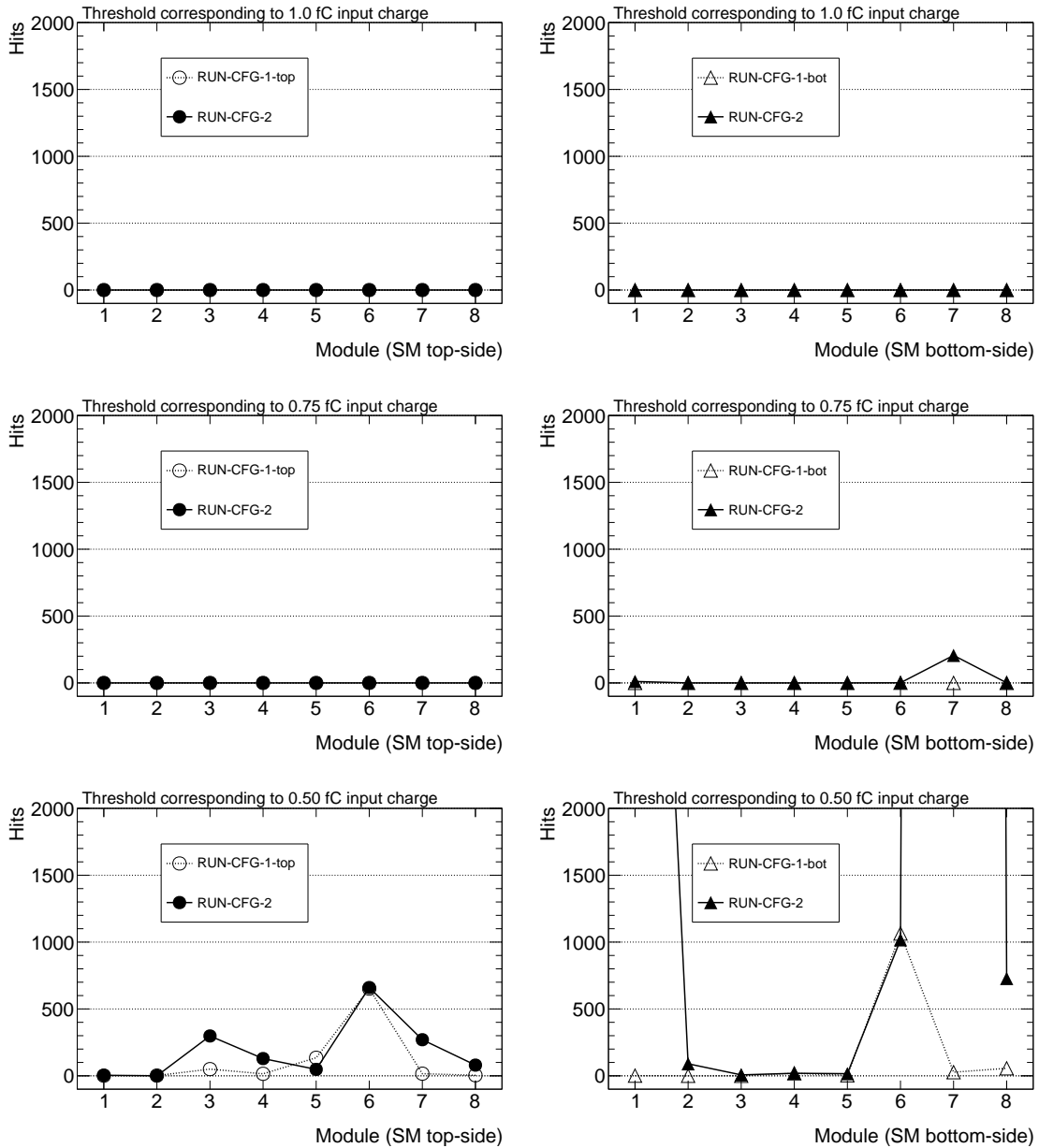
Figure 31. Results from the *Double-Trigger-Noise* test. Results for thresholds corresponding to 1.0 fC (top), 0.75 fC (middle) and 0.50 fC (bottom) charges are shown. In each plot, the *y*-axis shows the sum of hits for the two-hybrids of the corresponding module-side. See table 4 for the different configurations being compared. In the bottom-right plot, the results for modules 1 and 7 are out-of-scale.

the hybrid layout adapted to the new readout electronics and including a single DC-DC powering unit per module-side. The design evolution will continue to pursue a minimal material budget while ensuring excellent thermal management and optimal electrical performance. Figure 33 shows the future double-sided module design based in the ABCN-13 ASIC. Because of the increased number of channels in the chip, the hybrid witdth can be reduced by a factor of ~ 2. If the hybrid width is 12 mm wide, the weight of hybrid excluding electrical components is 1.9 g and 0.08% X_0
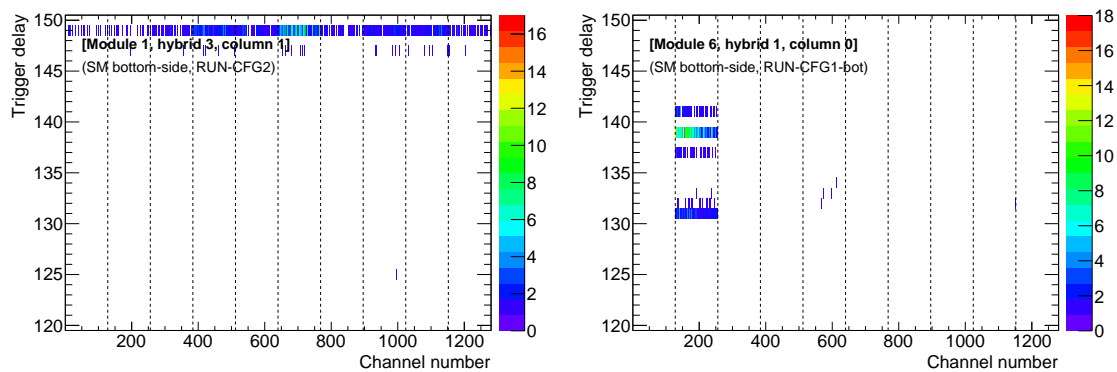
Figure 32. Particular examples from a DTN test for a threshold corresponding to 0.50 fC input charge. Two columns of ten chips of two different modules (module 1, hybrid 3, column 1, and module 6, hybrid 1, column 0) are shown. The *y* and *z* axes show respectively the time spacing (in 25 ns units) between the two triggers sent and the number of hits recorded from the second trigger. In the left-plot, a coherent common-mode noise is observed for all channels for a particular trigger spacing; in the right-plot, the noise pick-up is concentrated in a particular readout chip (128 channels) for several different delays.
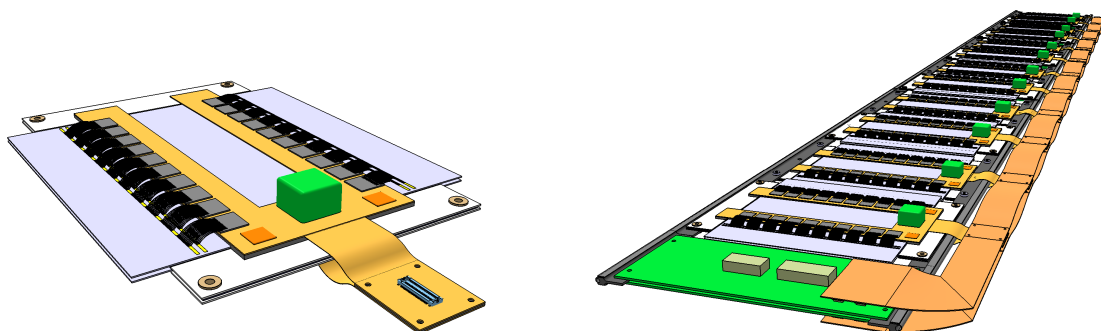

Figure 33. Module design concept with 256-channel ABCN-13 readout ASICs and shielded DC-DC power unit (left) and integration and overlapping of 12 double sided module together with the service bus and the SMC card at the two sides (right).

equivalent radiation length, normalized to the sensor area. The two per-module hybrids will have a common electrical supply with a U-shape connection holding the DC-DC power unit, the latter being integrated close to the ASIC columns and to the module facings to optimize the heat-exchange to the cooling plates. The interconnection of the module will be made with one pigtail per side that will directly connect to a service bus running along the Super-Module. As a consequence, the total radiation length of the new module is expected to be $\sim 1.6\%$ X_0 or less. A new very compact and low-mass service bus will be developed. The current design prospects foresees a significant width reduction by implementing all electrical lines within 20 mm. A second-generation local support structures will be fabricated, together with their services. The total radiation length of the new local supports including the service bus would be $\sim 0.6\%$ X_0 or less.

6 Summary

A super-module electrical prototype for eight double-sided silicon strip modules has been presented. Each silicon module is composed by two n-on-p silicon micro-strip sensors glued back-to-back to a central baseboard and four bridged kapton-flex hybrids each with twenty 128 channels ABCN-25 readout ASICs. The eight modules have been installed in an aluminimum support structure that includes a cooling circuit, two sets of multi-layer service buses, two SMB boards and 16 BCC boards. The low-voltage supply to the chips is ensured by DC-DC power converters (one converter per hybrid). The structure replicates the electrical and cooling aspects of the corresponding SM mechanical design.

The electrical performance of the super-module has been thoroughly tested. The simultaneous multi-module readout has been successfully proven. Extensive tests have been carried out in order to study the relative influence of high-frequency EMI emissions from the surrounding equipment and the DC-DC converters into the system. Several potential sources of EMI noise were identified. Results in terms of leakage current, gain, noise, noise occupancy and common-mode noise pickup have been shown. The gain is in very good agreement with the design value of the readout chip. In the worst case scenario with all 32 DC-DC converters enabled, a degradation of the electrical performance in terms of noise is observed if compared when testing the modules either individually or while testing a single-side of the super-module alone (16 DC-DC converters). The noise at the discriminator input lies in most cases in the range [600; 700] ENC(e). The noise occupancy does not show significant changes. A significant noise pick-up is observed from the double-trigger noise test, indicating that the system is not completely inmune to radiated and conducted noise. There is a certain interplay between the two super-module sides that is currently under investigation. Adding additional ground connections to the module hybrids and a redesign of the service buses is expected to further improve the overall electrical performance. These issues will be effectively addressed in a next module design based in the new version of the readout chip (ABCN-13).

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