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Miscellaneous

Readout electronics for the Silicon micro-strip detector of the ILD concept

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Readout electronics for the Silicon micro-strip detector of the ILD concept

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INTRODUCTION: Silicon strip readout ASICs and system overview

- Micro-strip silicon detector (50µm pitch, 300µm wide, variable length): Si sensor for the tracker in the future ILC. Usually, 256 Si-µstrips/module.
- Multiple channels are interrogated by a single multichannel chip.
- Figure 1 shows the typical structure of a readout system also presented in previous works (ABCD3T, APV25, Beetle chip, MX6, VA1, KPiX or SiTRK)
  - Pre-amplifier (CSA): integrates the generated charge (e/h pairs)
  - Shaper: LPF + HPF (order 1), filters noise and produces a slower pulse.
  - Pipeline: The shaped pulse is stored for later A/D conversion at low speed.
  - Sparsifier: Hit detection. Usually composed by a comparator.
  - ADC: Included in advanced readout systems.

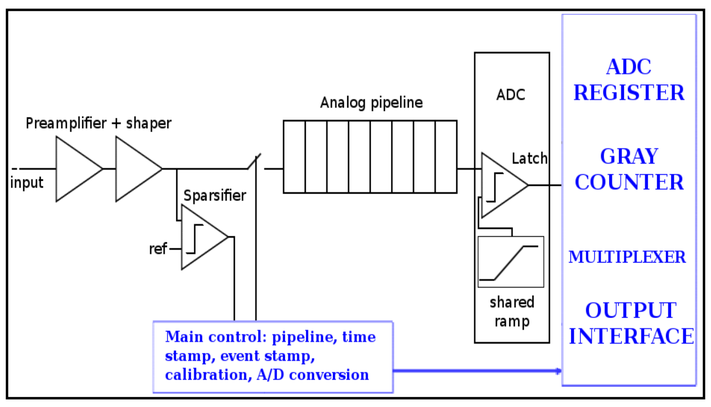

Figure 1: Silicon strip detector ASIC internal structure

Mixed-signal ASIC:

- ASIC detectors includes 16 ~ 256 channels, where each channel has both analog and digital circuits (the analog part is complex).
- Low power and low noise design requirements.

Purpose of this work:

- Analog behavioural description of blocks at the required level of detail.
- Schematic design of the input stage (pre-amp and shaper)
- Noise study

Verilog-AMS blocks for channel description

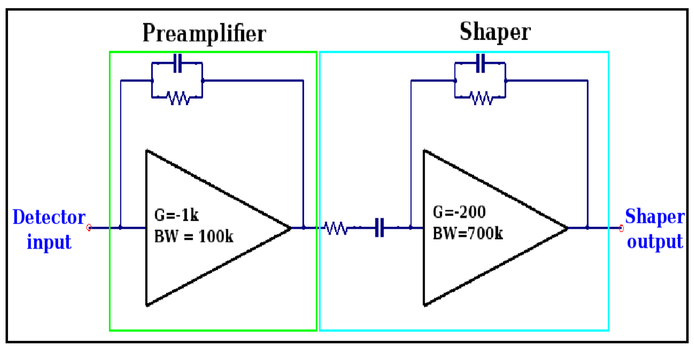

Figure 2: Preamplifier – shaper simulated circuits

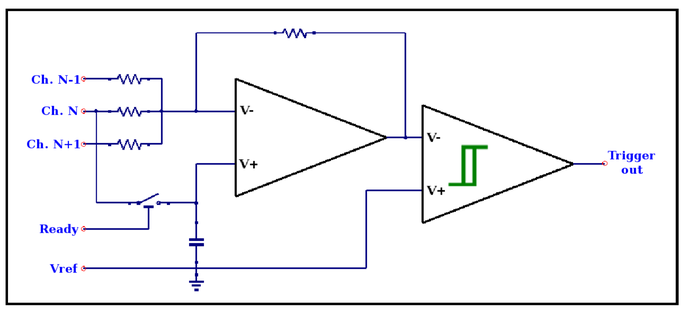

Figure 3: Sparsifier simulated circuit.

- Detector model
- Pre-amp and Shaper
- Sparsifier composed by an OPAMP & Schmitt trigger (3 adjacent channels compared against a reference).
- Analog pipeline + ADC (12 bits)
- Used to define key parameters of each module.

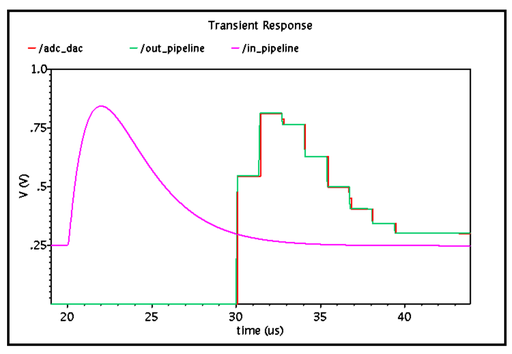

Figure 4: Shaper (magenta), Pipeline (green), ADC-DAC quantization (green).

Pre-Amp design in TSMC 65nm

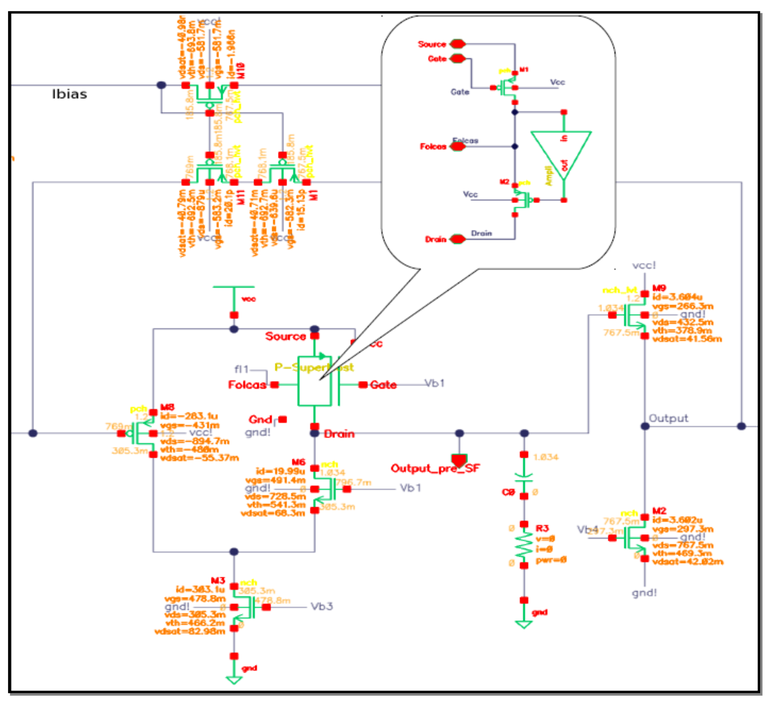

Figure 5: CSA: Folded cascode with gain-boosting.

- Power supply: 1.2 V
- Power consumption < 380 uW
- Full scale: 100 MIP (1 MIP = 24000 e-)
- Amplifier:
  - Gain ~ 69 dB
  - 3 dB-BW ~ 55 kHz
  - PM ~ 66º
- Main noise contribution of the circuit.
- Equivalent Noise Charge: ENC = a + b C_d (where C_d is the capacitor of the detector)
- Optimum L and Ibias to maintain the noise below 500 e-

Shaper design in TSMC 65 nm

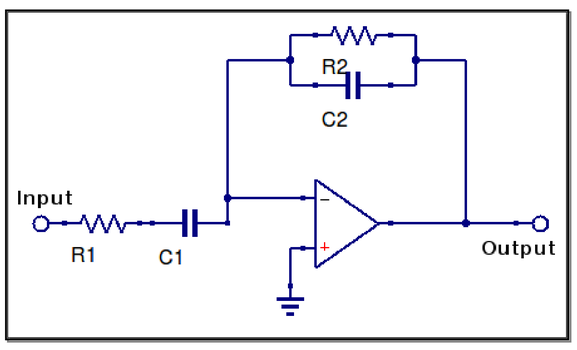

Figure 6: Schematic of the shaper

- Folded cascode
- Power supply: 1.2 V
- Power consumption 120 uW
- Amplifier:
  - Gain ~ 60 dB
  - 3 dB-BW ~ 90 kHz
  - PM ~ 63º

	sensor thickness	A	B	Noise at 20pF
Poly. resistors	300µm	260e-	4.9e-/pF	350e-
	200µm	188e-	4.5e-/pF	272e-
Current mirror based	300µm	180e-	7.7e-/pF	326e-
	200µm	228e-	7.7e-/pF	374e-
MOSFET based	300µm	148e-	6.3e-/pF	266e-
	200µm	129e-	5.5e-/pF	233.1e-

Table I: Noise comparison for each configuration

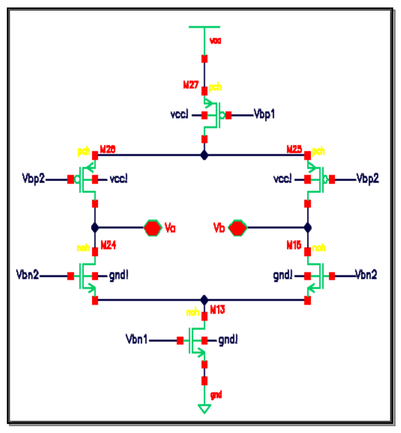

Figure 7: Schematic of an active resistor solution

Shaper feedback resistor:

- Polysilicon resistor
  - Large area
- Active resistor:
  - Single transistor (only suitable for small $|V_{DS}|$ variations)
  - Other options explored (figure 7) but the noise is too high (about 6 times the thermal noise)
  - Resistor demagnification

Pre-amp and Shaper noise problems due to non-ideal current biasing

- Scaling up I_{bias} from a reference current source vastly increases the noise
- Current references with lower current relation implies higher consumption but lower noise
- Introducing a filter in the reference current reduces the power spectral density (PSD)

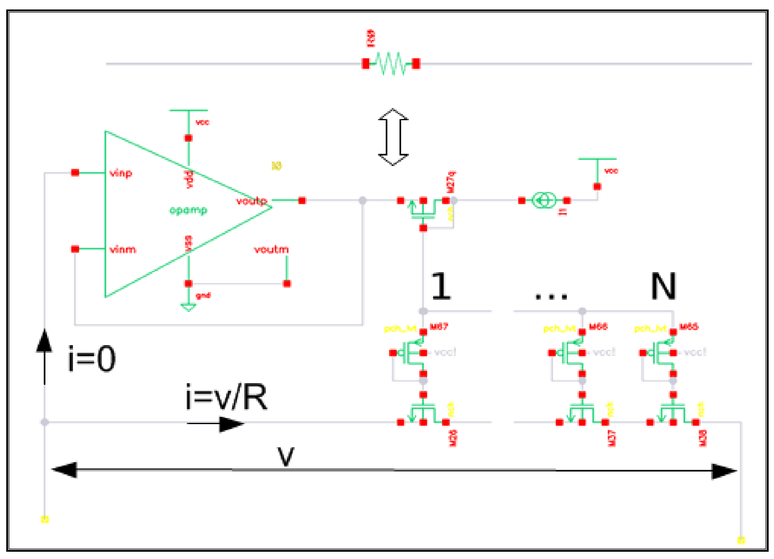

Figure 8: Schematic of the designed Shaper

- The voltage in the resistor is divided with N transistors.
- ~ GΩ equivalent resistor.
- VGATE ~ constant (gate is capacity-coupled to source)

CONCLUSIONS

1. A top-down design flow based on behavioural models is applied to this ASIC design.
2. The entire channel can be simulated at behavioural level.
   - It is quite fast to get an entire channel model and simulation.
   - Parameters of different modules can be explored for optimum performances (such as the influence of the integration time to the shaper output).
3. Pre-amp and shaper schematics designed with TSMC 65 nm
   - Designed to reduce noise, area and power consumption
   - Solved issues related to use non-ideal sources
4. Noise comparison to previous works presented in Table II.

Front-end	A (e-)	B(e-/pF)	Shaping time
APV25	246	36	50 ns
MX6	340	20	
VA1	200	8	1µs
Beetle	303	33,6	25 ns
KPix	300	35	
This des., polysilicon	260	4.9	2µs
This des., current scaling	180	7,7	2µs
This des., quasi-floating gate	148	6,3	2µs

Table II: Noise comparison to previous works

ACKNOWLEDGEMENTS

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