AIDA

Advanced European Infrastructures for Detectors at Accelerators

Presentation

Second generation DAQ for CALICE beam tests

Boudry, V (CNRS)

29 September 2011

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Second generation DAQ for CALICE test beam

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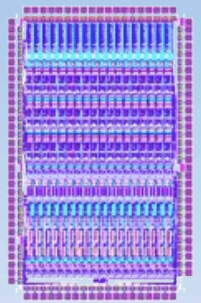
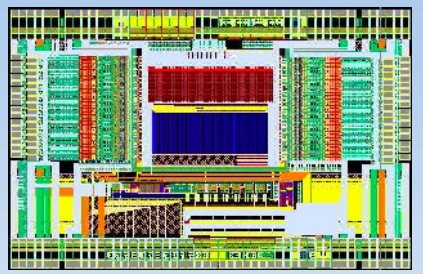
LCWS,11
Grenade
29/09/2011

CALICE collaboration
Physical prototypes

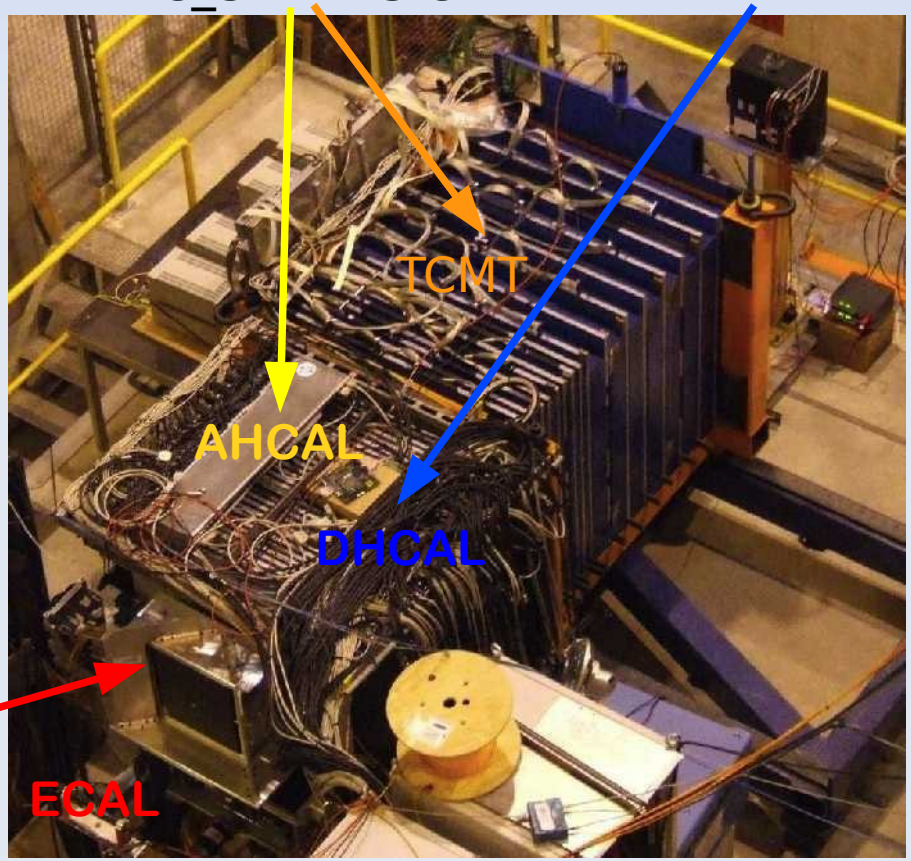
- Prototypes
  - Si-W ECAL, ScW ECAL (Scint+MPPC)
  - AHCAL (Scint + SiPM/Fe)
  - DHCAL (RPC + DCAL III / Fe)
  - TCMT (Scint+SiPM or RPC+DCAL / Fe)
- CALICE DAQ1
  - Readout of FLC* analog pipeline
  - External ADCs & Sequencing
- DHCAL DAQ
  - Readout of DCAL digital pipeline.
  - Dead time free triggered readout



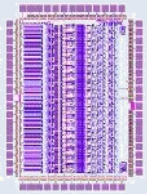
FLC_SiPM ASIC



DCAL III ASIC



FLC_PHY3 (2003)

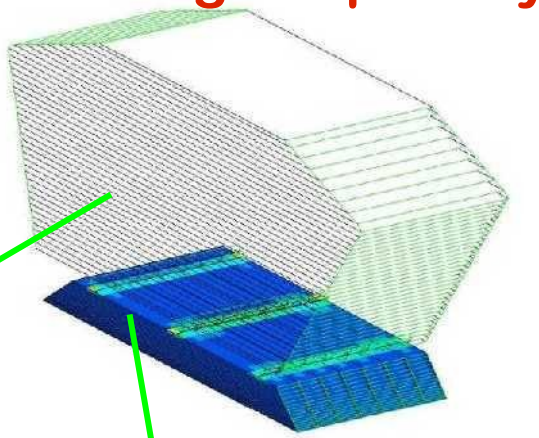


ROC familly 2nd Generation ASICs

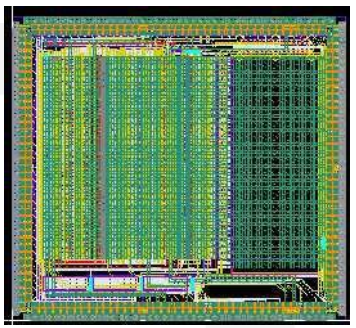
FE electronics adapted for the ILC:

- Add **auto-trigger**, analog storage, digitization and token-ring readout !!!
- Include power pulsing : <1 % duty cycle
- Address integration issues asap
- Optimize commonalities within CALICE (readout, DAQ…)

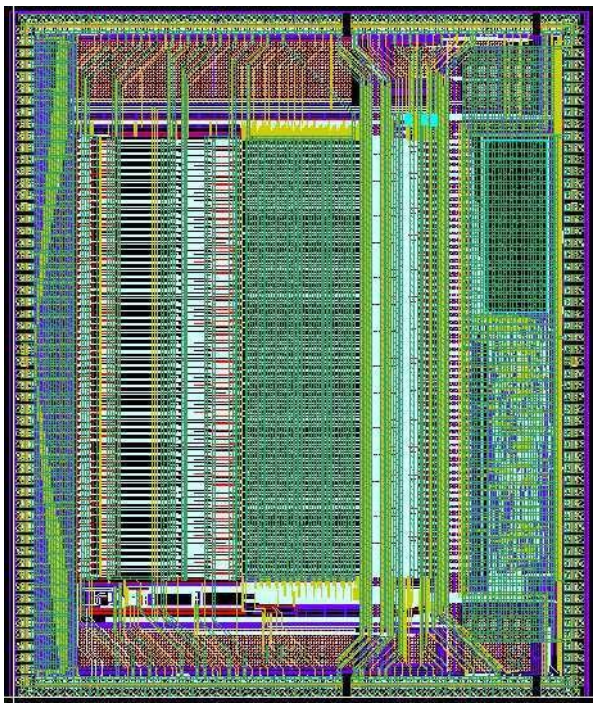
Technological prototypes



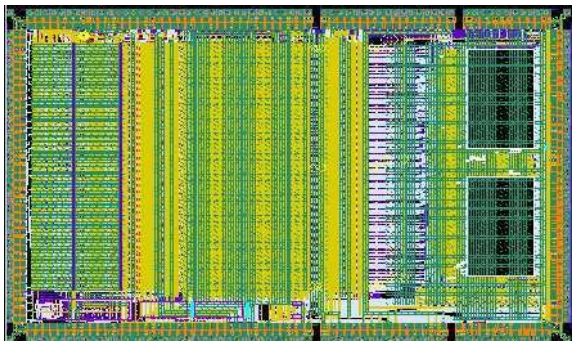
HARDROC2
SDHCAL RPC
64 ch 16 mm²



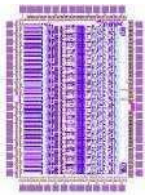
SKIROC2
ECAL Si
64 ch. 70 mm²



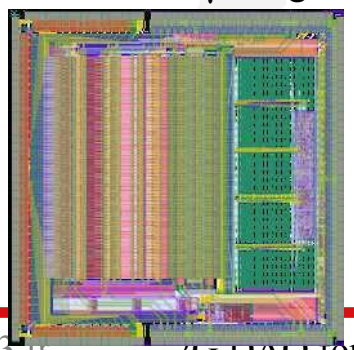
SPIROC2
AHCAL SiPM
36 ch 30 mm²



FLC_PHY3 (2003)



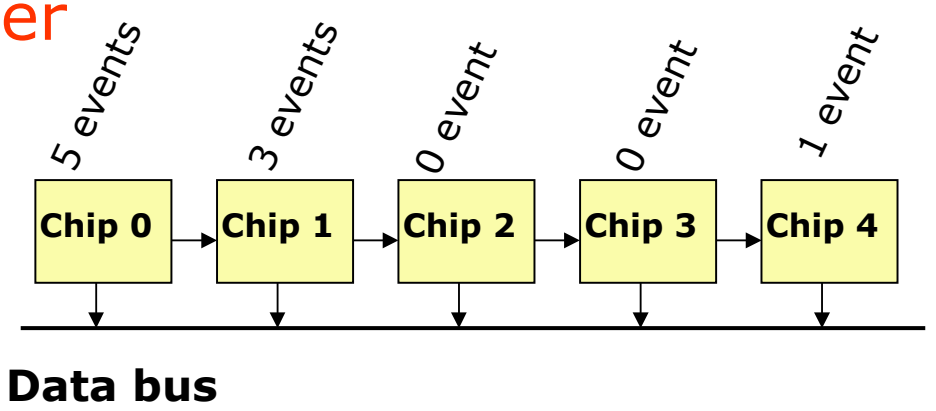
MICROROC
SDHCAL µMegas

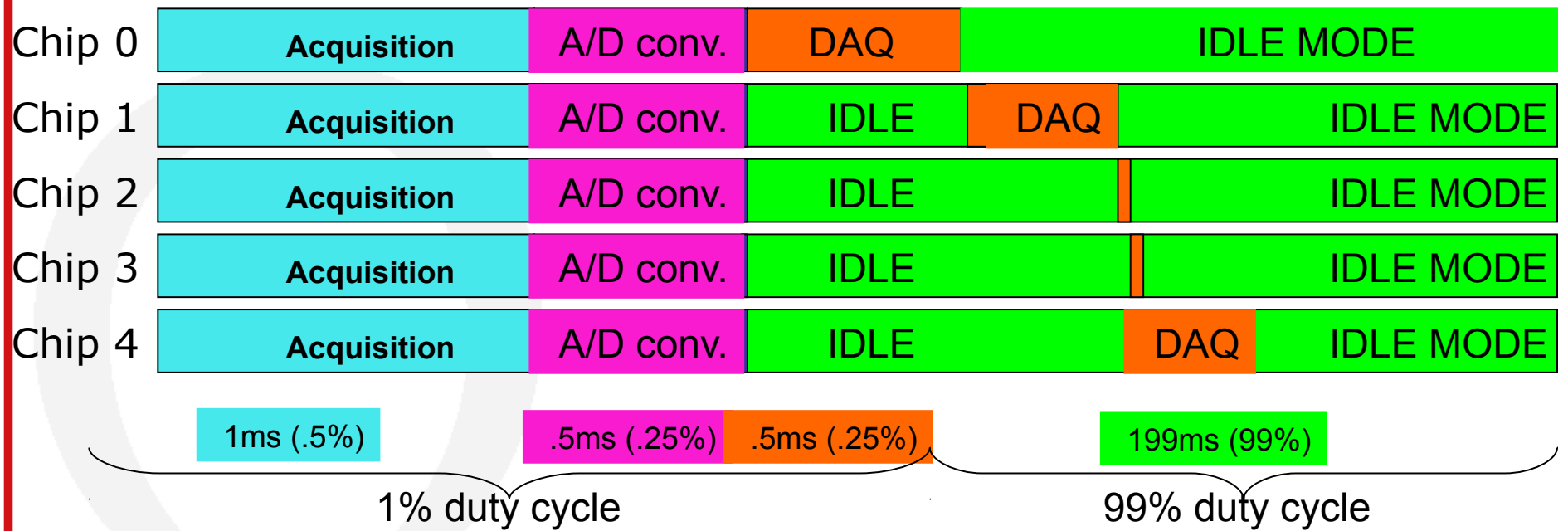


Adapted from Ch. de la Taille

Read out: token ring

- Readout architecture common to all calorimeters
- Minimize data lines & power





Slide from Ch. de la Taille

SDHCAL m^3
(IPNL, LAPP, LLR)

MICROROC $1m^2$ assembly
(LAPP)

SPIROC2 with AHCAL new electronics
(DESY)

SPIROC2 with ECAL new electronics
(LLR)

DAQ Task goal

Original ideas and R&D from CALICE-UK (UCL, Cambridge U., Manchester U., RHUL)

- "Generic" DAQ based AMAP on commercial boards
  - **Extensible** for Large Detectors + redundancy
  - **Flexible** → FPGA based : various acquisition modes (triggered, ILC-like)
- Provide the **digital** readout of CALICE embedded front end (*ROC chips) [1st gen was analogue]
  - All calorimeters seen through CALICE **standard** Detector **InterFace** board (**DIF**)
    - **Sends** configuration; fast commands; clocks; Triggers
    - **Receives** Data; Busy
  - 1 or 2 **Concentrator** cards level
  - **Distribution & collection** of the fast signal & sequencing
  - Advanced Off-Detector Receiver (FPGA based event builder)
  - **All signals on 1 cables**; add-hoc **secure communication** protocol
    - "low speed" 8b/10b coding

- 3 CALICE prototypes en route:
  - SDHCAL : ~400.000 ch; Digital (2b/ch → 2.5 with BC information & fmt)
  - ECAL : ~ 22.000 ch; Energy (12b → 32.2)
  - AHCAL : ~ 52.000 ch: Energy & time (2×12 b → 32.3)

Test beam Acquisition modes

Single Event + Ext. Trig

- External trigger (from hodoscope or calibration system) = HOLD
  - Stop Acq, Hold analog data + sampling, Start Acq
- Noise & Beam condition safe (only 1 evt per trigger)

Single Event + auto-Trig NOW USED IN DHCAL TB

- **External trigger** (hodoscope) → DIF
  - Stop Acq, ReadOut (last evt ~ triggered one), Start Acq
- **Data sync** (for Event building)
  - On synchronized BC ID → **need for a SYNC @ MClk (100– 400 ns)**
  - On trigger timestamp
  - **BUT: for the AHCAL/Spiroc:** the TDC signal needs a SYNC of the clocks **±1ns**
- **Rems:** RAMfull from 1 ASIC → Reset of all detector

ILC like

- StartAcq on Start-of-Spill signal (-δt)
- StopAcq & Readout on End-Of-Spill or RAMfull or a Given # Beam Trigger

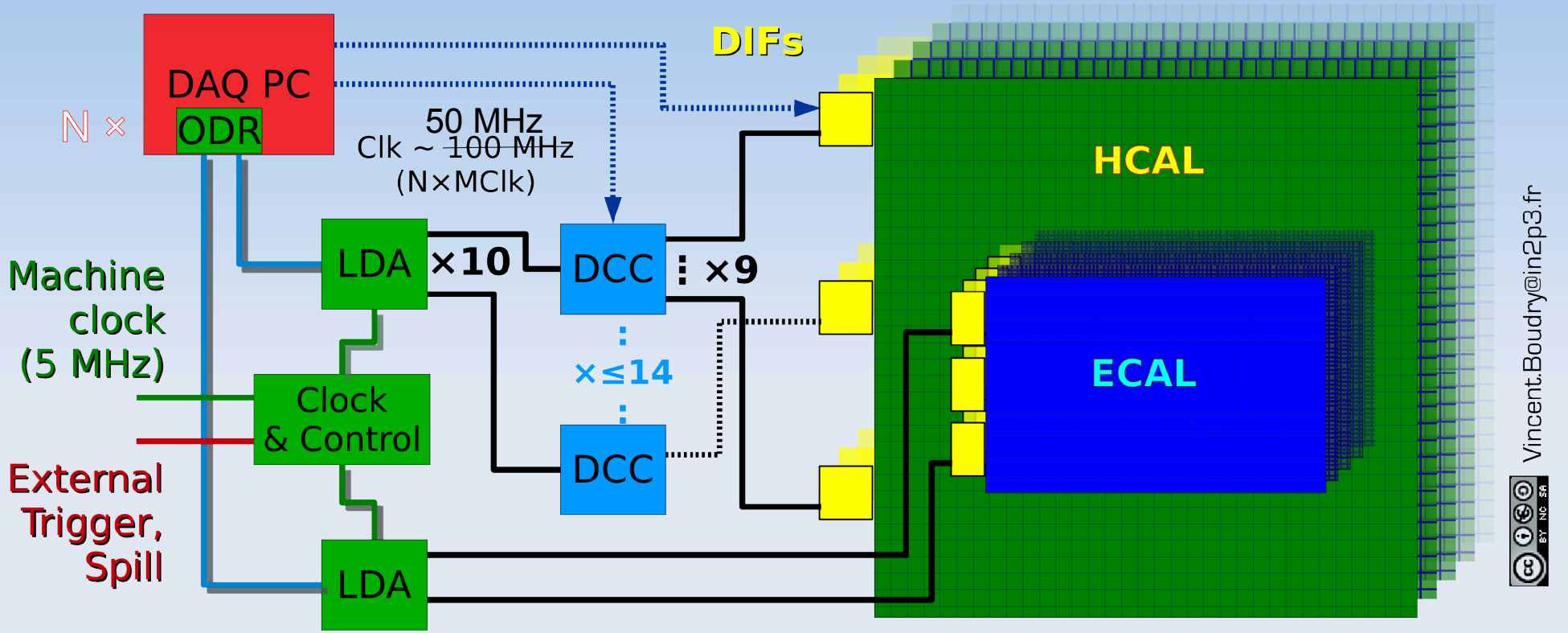
Three TB Running modes:

- **Physics**
  - as fast as possible *IN SPILL*,
  - poissonian stat → As low as possible PILE-UP (or not!)
  - Data with “low occupancy” (particle type & E dependant)

- **Demonstrator**
  - as close as possible from final ILC conditions
    - power pulsing, auto-trig
    - beam conditions close to ILC ? (Duty cycle, occupancy)

- **Calibration / noise**
  - *a priori*: off spill, fixed rate
  - all cells (“maximum occupancy”)

CALICE DAQ2 scheme



LDA-DIF on HDMI (Config, Control, Data, Clock, Trig, Busy, Sync)

Clock, Trig, Busy & Sync on HDMI (compatible LDA-DIF)

Optique (alt. Cable) GigE

Debug USB

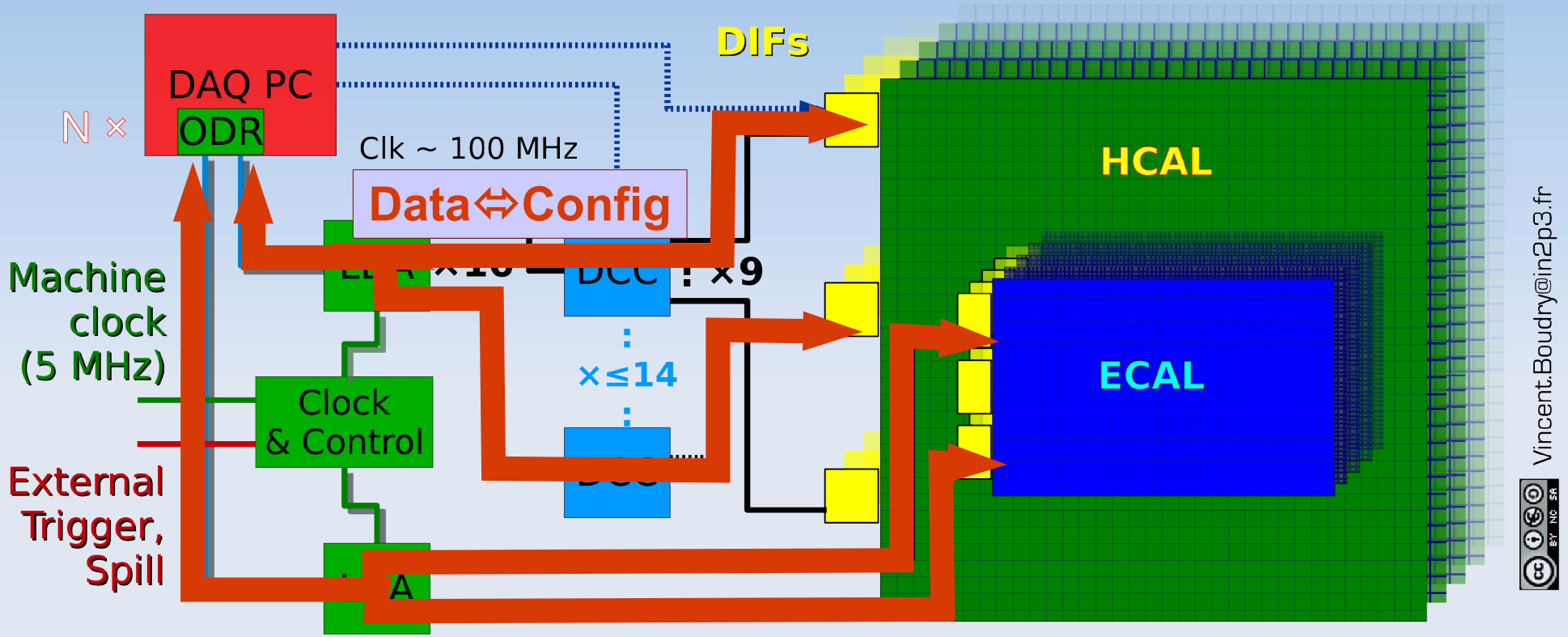
External Trigger

ODR = Off Detector Receiver
LDA = Link Data Agregator

DCC = Data Concentrator Card
DIF = Detetcor InterFace

CCC = Clock & Control Card

CALICE DAQ2 scheme



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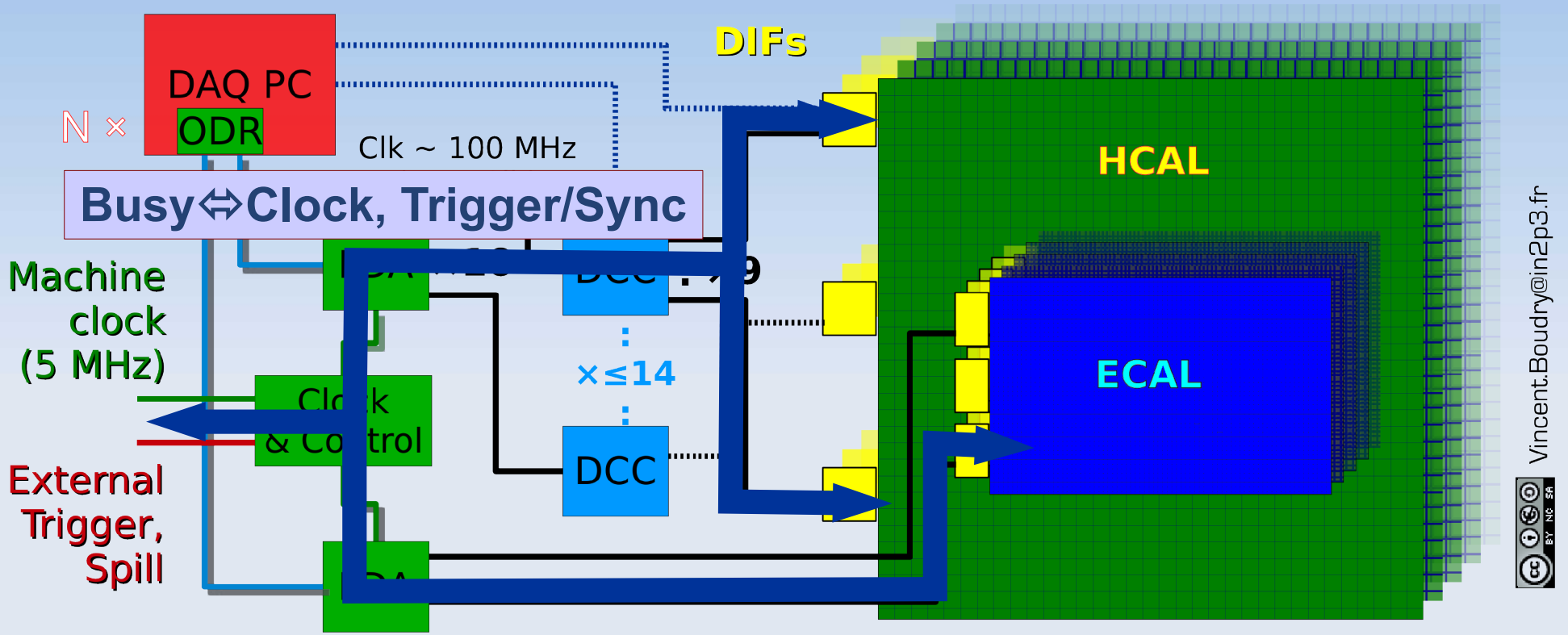

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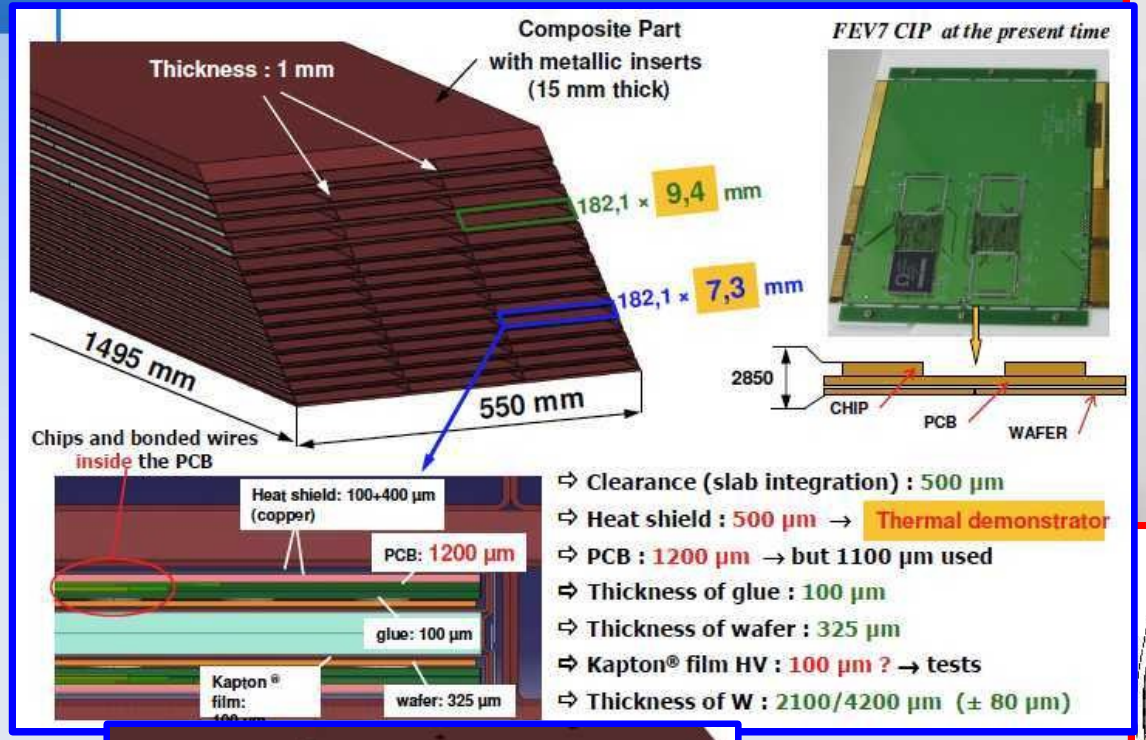
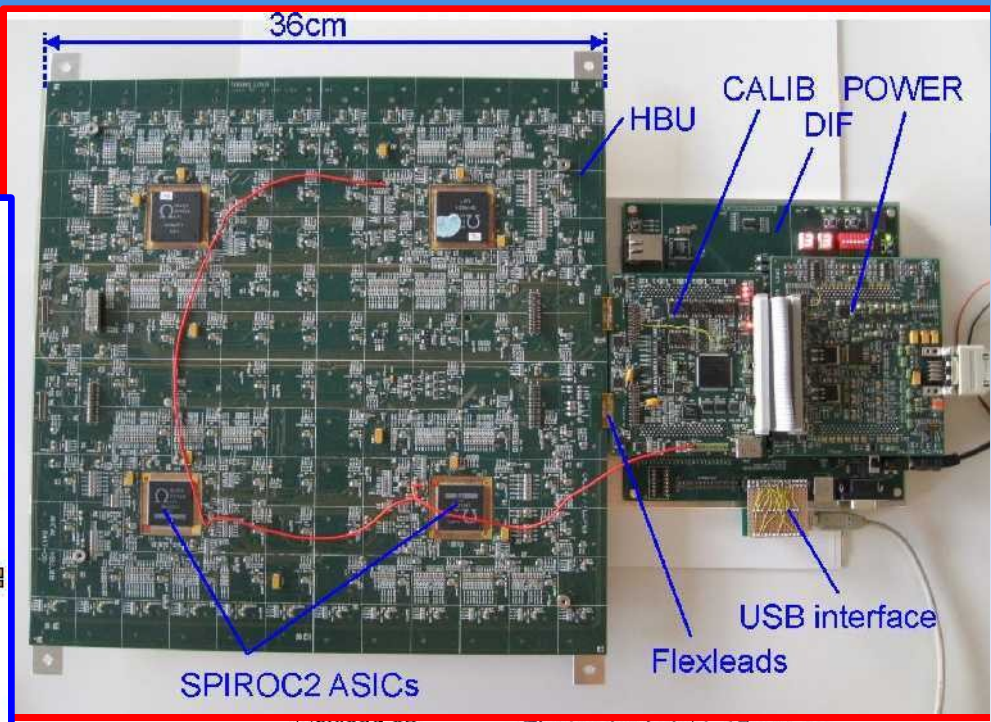
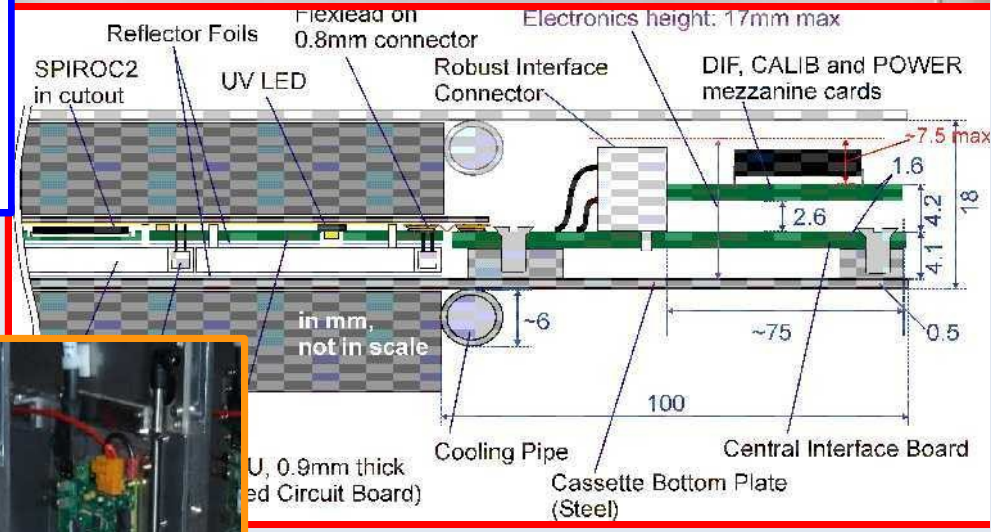
Detector interfaces



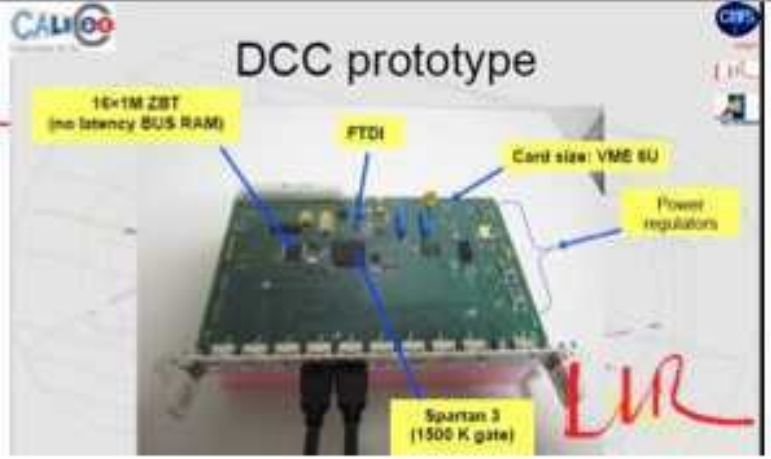




ECAL (CAM)

AHCAL (DESY)

DHCAL (LAPP)



LDA

- The LDA (from Enterpoint) consists of :
  - Mulldonoch2 baseboard;
  - add-on HDMI board to connect to 10 DIFs;
  - an add-on ethernet board to connect to an ODR.
- Firmware development :
  - DIF <=> LDA link running;
  - new code soon to be posted to svn;
  - same format as ODR in svn repository.

DCC and LDA are essentially similar to an ethernet switch but using a low level protocol

They both fan-out/in fast isochronous signals on a dedicated path and commands on the 8b/10b serial link

LDA has a fast link : Gb ethernet to the upper level = ODR, and can connect to 10 DIFs or DCC with the 8b/10b serial link
DCC can connect to 1 LDA and 9 DIFs using the 8b/10b serial link, data from DIF are buffered and sent to the LDA

CCC

- Overall status unchanged for a while.
- Fans out clocks, fast commands and control signals.
- Fans in busy.
- Full complement of 10 boards with power supplies tested.
- One in LLR and one in LAPP.
- CCC link to LDA still needs to be done :
  - Board designed and firmware developed for testing;
  - Soon to produce enough boards for all LDAs.

ODR

- Receive data on 4x fibre (RX),
- Write to disk FAST (>150MB)
- Send data up fibre (TX)
- Controlled from Linux driver
- DOOCs Interface

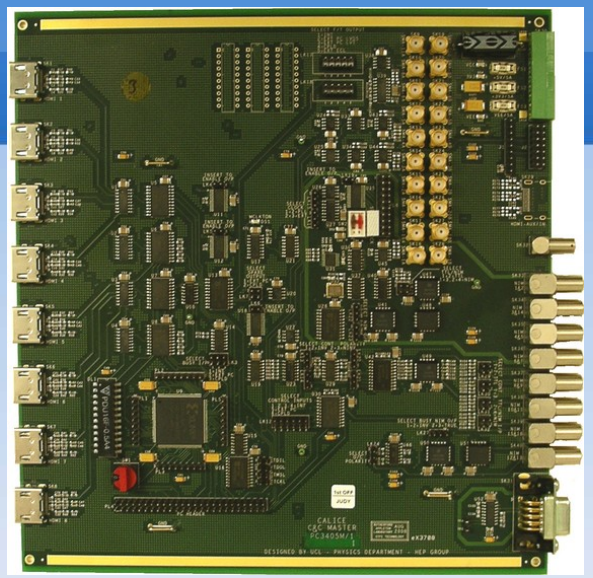
Documentation / repository

- All components *should* have extensive documentation on twiki : it is being updated and as components are basically done, can soon be finalised.
- Twiki main :

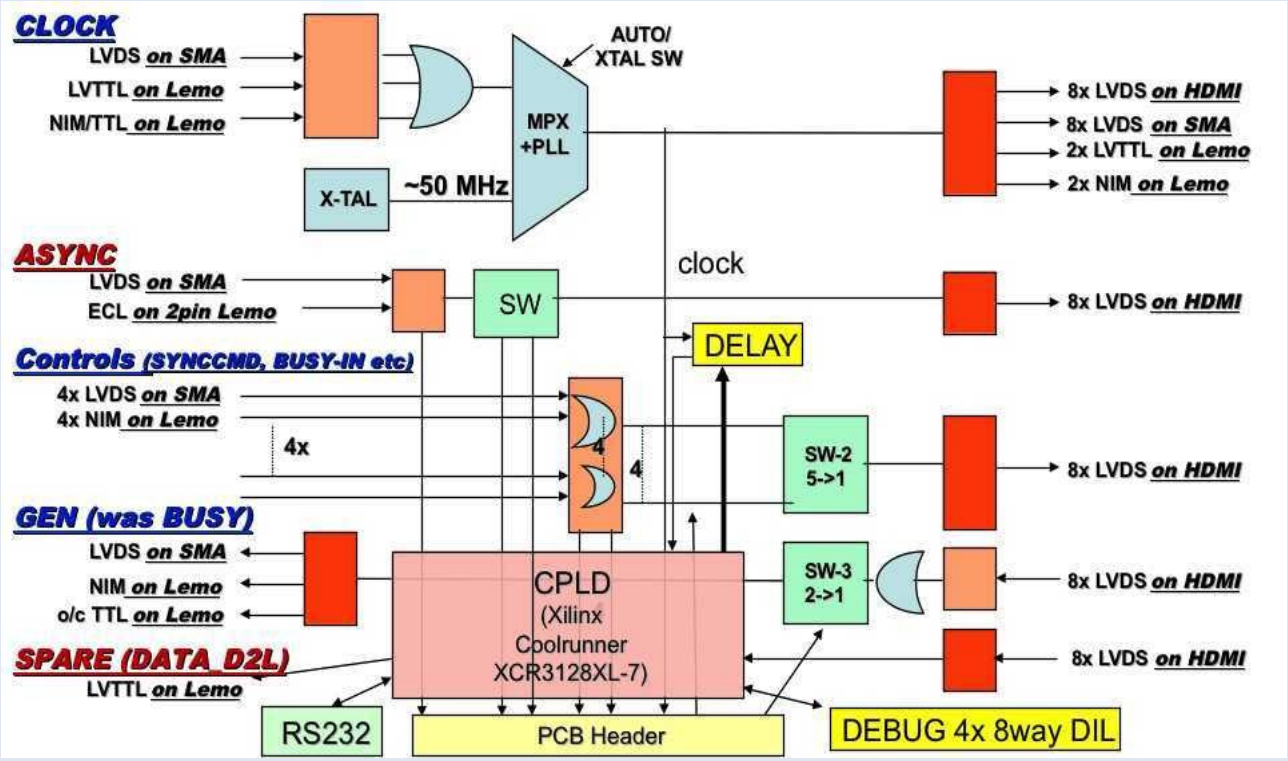
  https://twiki.cern.ch/twiki/bin/view/CALICE/CALICEDAQ
- Also list of hardware availability /status started.

  https://twiki.cern.ch/twiki/bin/view/CALICE/HardwareList

Clock and Control Card



- Developed at UCL (M. Warren, M. Postranecky)
- Distributes on 8 channels (HDMI, SMAs, NIM, …) via dedicated circuitry for **low jitter**
  - Int | ext clock
  - Fast Signal (Trigger | Sync)
- Sums-up BUSY
- Performs Trigger logics
  - CPLD
- Performs sequencing
  - Reset of detector on ramfull
  - Readout order on Trigger
- At limit
  - new HW required

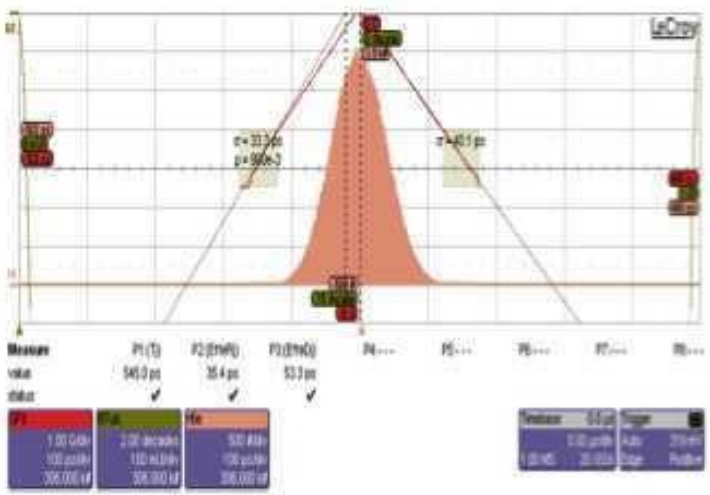


Clock & Trigger jitter

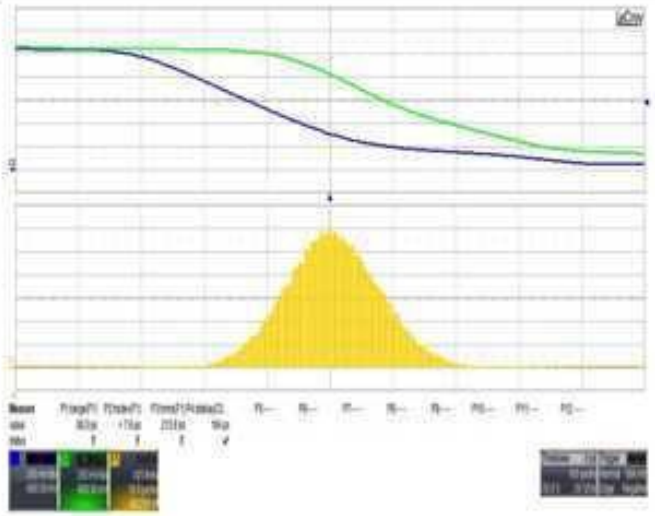
- Trigger & busy handling (G. Vouters)
  - Trig (NIM) → CCC → LDA → DCC → DIF
    BUSY ← CCC ← LDA ← DCC ↵
- Trigger Jitter between DIFs (FG)

Jitter measurement

Setup : CCC – LDA – DCC -DIF



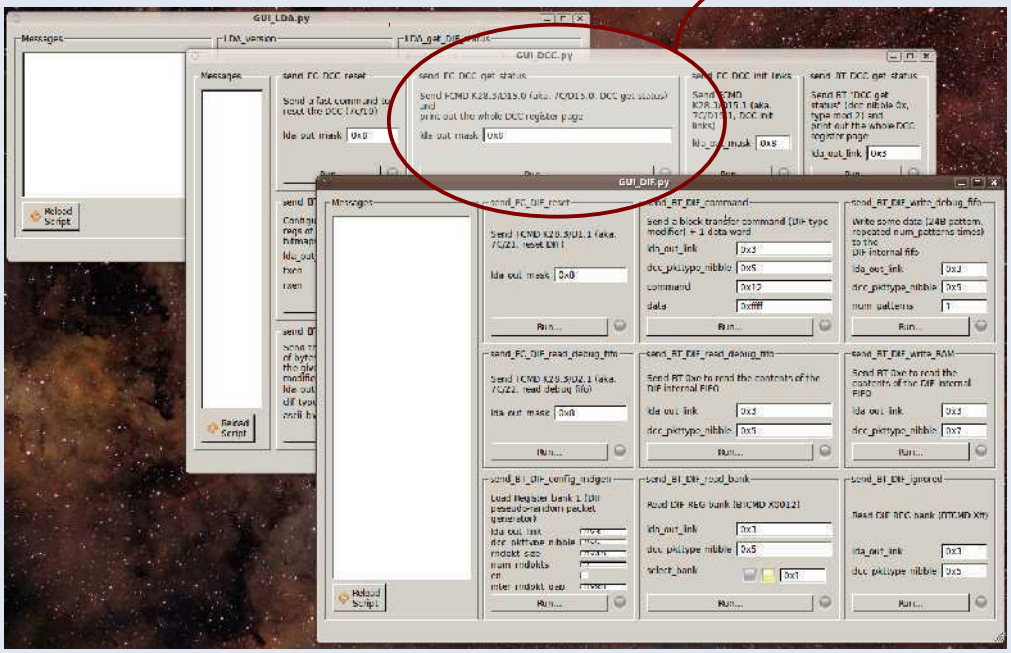
Clock (50 MHz) jitter at the input of DHCAL DIF
TJ ~ 545 ps



Delay between trigger on 2 DIFs, the delay is around 200 ps, must be confirmed with other test and more DIF connected to a DCC

Python Test toolkit

- Interactive hardware test software (GUI)
  - Each HW test easily scriptable: simple user-friendly python API: each function defined ↔ 1 graphical pane with “Run” button
  - Available to anyone working with USB/RS/Ethernet devices
- C libraries implementing the complete **DIF Task force** protocole → API



```
File  Edit  Options  Buffers  Tools  Python  Help

def send_FC_DCC_get_status(INT0x_lda_out_mask = 0x8):
    """Send FCMD K28.3/D15.0 (aka. 7C/D15.0, DCC get status) and
    print out the whole DCC register page"""
    comma  = commons.encode_8b10b_kd(28, 3)
    data   = commons.encode_8b10b_kd(15, 0)
    ans    = LDA.do_lda_send_fastcmd(INT0x_lda_out_mask, comma, data)
    calicediag.GUI.set_statusbar_message("Get_Status FCMD sent")

    return _unpack_DCC_get_status_page(ans[16:]) is not False

--:---  DCC.py      47% (189,0)   SVN-1428  (Python)----------
calicediag.register_action(DCC.send_FC_DCC_reset)
calicediag.register_action(DCC.send_FC_DCC_get_status)
calicediag.register_action(DCC.send_FC_DCC_init_links)

calicediag.register_action(DCC.send_BT_DCC_get_status)
calicediag.register_action(DCC.send_BT_DCC_config_tx_rx)
calicediag.register_action(DCC.send_BT_DCC_start_RTT)
calicediag.register_action(DCC.send_BT_DCC_stop_RTT)
calicediag.register_action(DCC.send_BT_DCC_relock_DCM)
calicediag.register_action(DCC.send_BT_DCC_register_blob)

--:---  GUI_DCC.py  Bot (7,0)     SVN-1428  (Python)----------
```

https://svn.in2p3.fr/calice/online-sw/trunk/pyserdiag/

Reliability tests

Stress tests using pseudo-random generator

- 9×DIF → 1×DCC → 1×LDA → PC
  - 9 DIFs (ECAL & SDHCAL) generate pseudo random data
- Results
  - Direction DIF → LDA ✔
  - Maximum DCC → LDA link occupancy (40Mbps) ✔
  - Many TB of data transferred no error (on table)

End-to-end test: FIFO write/read

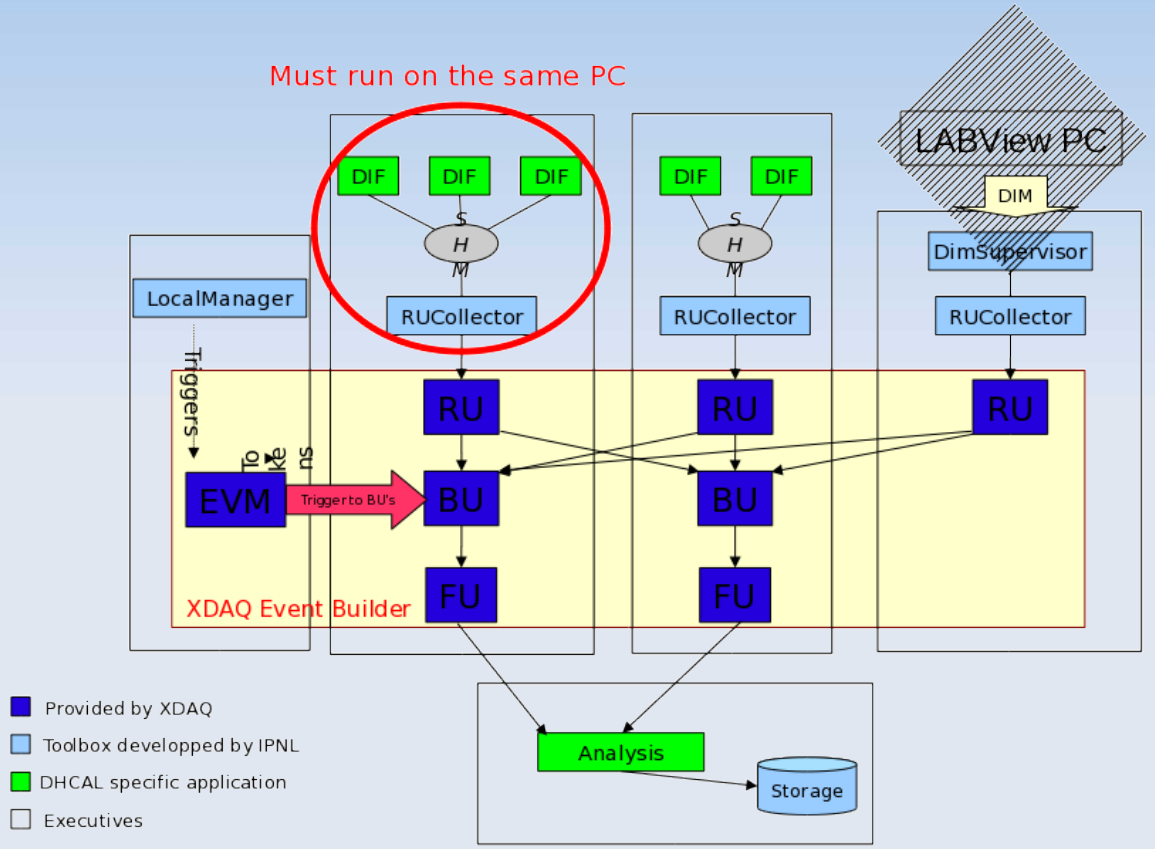
- PC ↔ 1×LDA ↔ 1×DCC ↔ 1×DIF
  - Tests both fast-commands and block transfer “read” requests
- PC ↔ LDA Ethernet OK

ROC config loading & checking ✔

Software: XDAQ framework

- dev[ts] started @IPNL for electronics test using XDAQ in 2008
- Ran for ≥ 1 year in TB, Cosmics & Electronics test
  - USB readout
  - Interface to old LabView program
- Recent development
  - Integration of DAQ2 readout chain
  - interface to a configuration DB
  - Writing of LCIO data in RAW format
  - versatile online analysis framework (root histos)

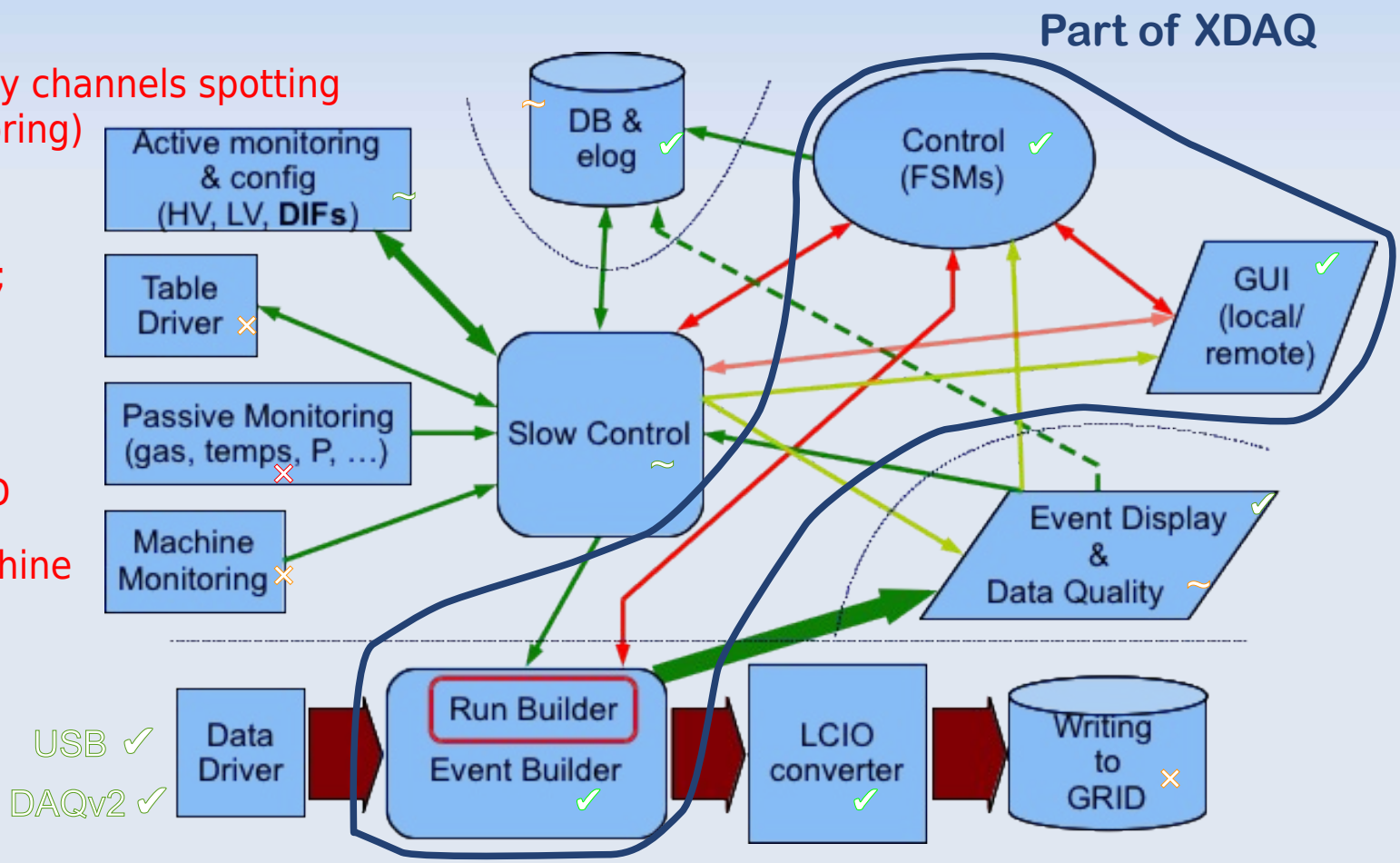
    → Marlin Based
- For current TB: deployment on 4 PC tested;
  Performances to be improved



IPN Lyon

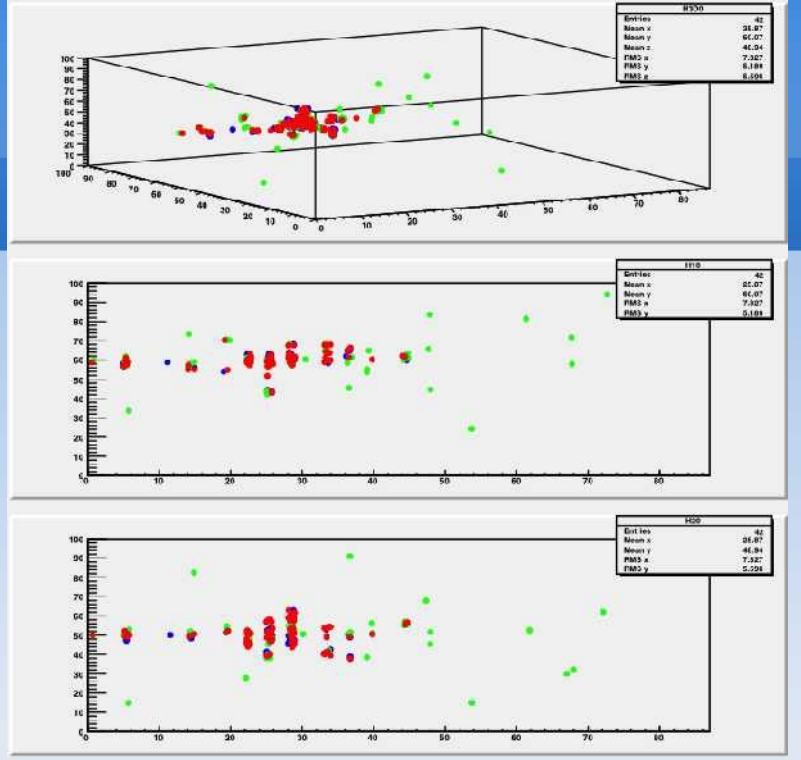
SW status

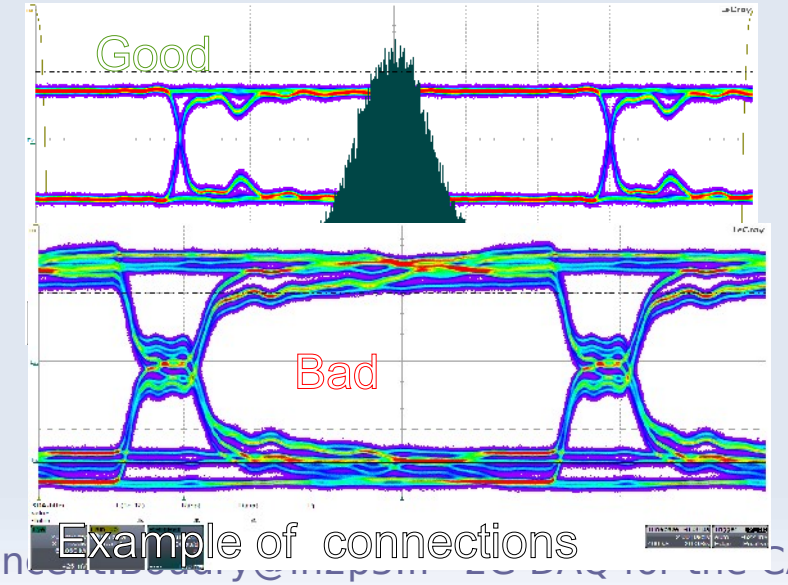
- XDAQ + C library to DAQ2
- All critical elements are ready
  - Configuration DB (being worked on)
  - DAQ2 interface
  - Semi-automatic noisy channels spotting & correcting (monitoring)
  - Clean Slow control
  - interface to CondDB;
  - event display
- Missing ancillaries
  - interface to the GRID
  - interface to the machine (⊃ in AIDA WP8.6.2)



First large scale test

- Last 2 weeks at PS
  - SDHCAL with 31 chambers (~2/3 of full det).
    - 90 DIFs, 2 LDAs, 13 DCC, 1 CCC, 4 PCs
  - ~4400 ASIC / 285k channels individually configured
- Solved grounding problems, reset procedure, mis-functionnal elements, FW glitches, Data corruption
- Readout ~100k triggers in test beam mode (10 GB of data)
  - ≥1 events per trigger
  - trigger on scintillators





Example of connections

lda	dcc	cumulative data size	nb of shmwr	Failed	Corrupted
1	1	330200	357	0	0
1	2	256638	357	0	0
1	3	1891131	355	0	1
1	4	720476	357	0	0
1	5	662954	357	0	0
1	6	944784	357	0	0
1	7	691332	357	0	0
1	8	719920	355	0	1
1	9	1289548	355	0	1
2	1	0	0	0	0
2	2	0	0	0	0
2	3	0	0	0	0
2	4	1165448	357	0	0
2	5	802156	355	0	1
2	6	838746	357	0	0
2	7	1927652	357	0	0
2	8	2155632	357	0	0
2	9	1690838	355	0	1
3	1	1287528	355	0	1

Performances

- Rather low demands in term of bandwidth
  (but >> @ ILC for same vol.)
  - SDHCAL : ~ 20MB/s in Spill
  - ECAL: ~100MB/s
  - AHCAL: ~ 300 MB/s
- **Data limited by ASICs readout**
  - Modes:
    - test beam single event
    - Test beam burst (≈ ILC-like mode)
- Some code (System C) exists for simulation of full chain, being tested
- Successful full scale test done last week at PS with the SDHCAL
  - 5 Hz of data taking
  - Noisy detector (heat)

DAQv2 data flux

N DIF/LDA	N DIF/DCC	LDA-DIF Dclk [MHz]	LDA-DIF FLUX [MB/s]	LDA Dclk [MHz]	LDA FLUX [MB/s]	ODR FLUX [MB/s]	Disk Flux [MB/s]
10	9	50	6.25	1000	125	1000	170

Detector	DHCAL	Evt Size	Mem Size	ASIC Dclk [MHz]	ASIC FLUX [MB/s]
		20 B	128	2.5	0.31

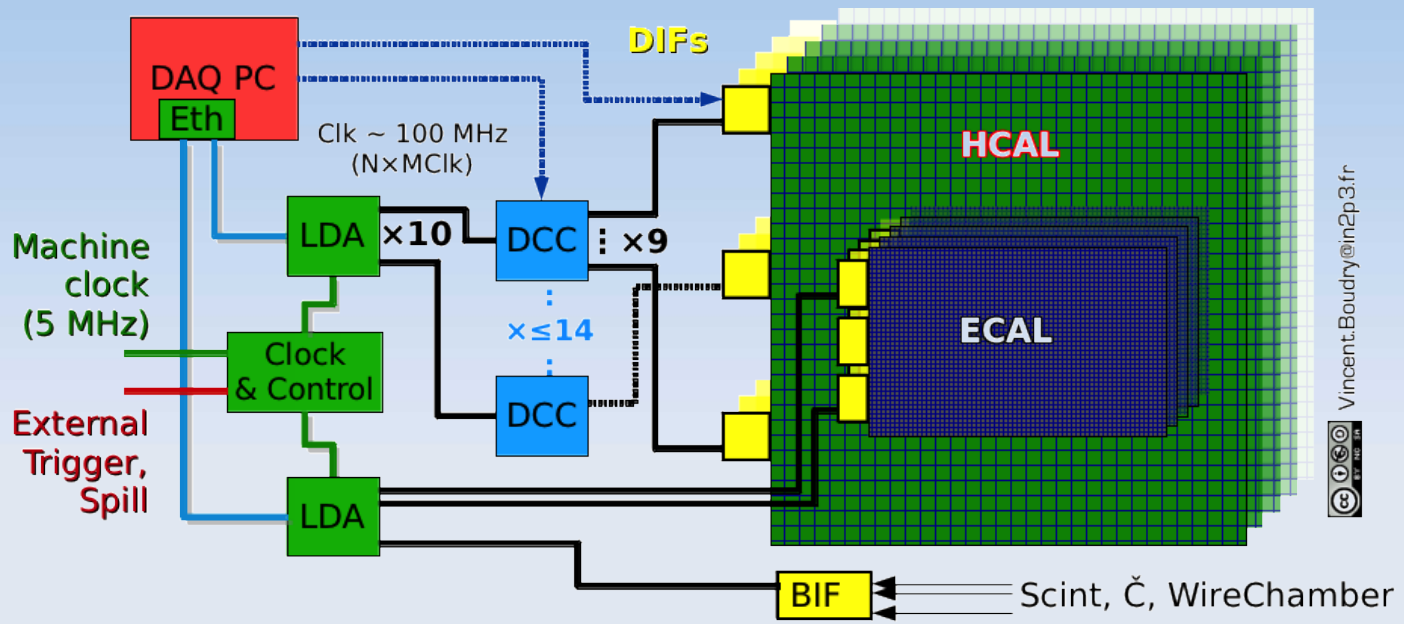
from LC-DET-2004-029

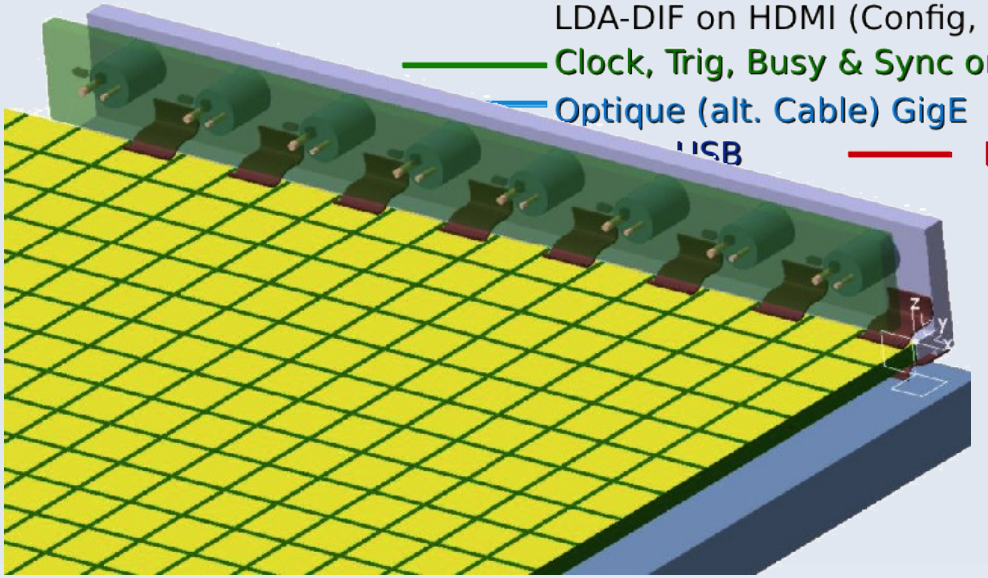
Mode	Calib/Noise Single	Calib/noise Burst	TB Single	TB Burst	Demo
N ASIC/DIF	48	48	4.8	4.8	4.8
σ (NASIC)	0	0	2.6	2.6	2.6
Touched DIF/pla	3	3	1	1	1
ASIC	20 B	2 560 B	20 B	2 560 B	2 560 B
R/O time 1	*64 µ s*	*8 192 µ s*	*64 µ s*	*8 192 µ s*	*8 192 µ s*
R/O time ALL	***3 072 µ s***	***393 216 µ s***	***307 µ s***	***39 322 µ s***	***39 322 µ s***
DIF	960 B	122 880 B	96 B	12 288 B	12 288 B
R/O time	*154 µ s*	*19 661 µ s*	*15 µ s*	*1 966 µ s*	*1 966 µ s*
LDA w/o DCC	9 600 B	1228 800 B	320 B	40 960 B	40 960 B
R/O time	*77 µ s*	*9,830 µ s*	*3 µ s*	*328 µ s*	*328 µ s*
DCC	8,640 B	1,105,920 B	288 B	36,864 B	36,864 B
R/O time	*1 382 µ s*	*176 947 µ s*	*46 µ s*	*5 898 µ s*	*5 898 µ s*
LDA w/ DCC	86,400 B	11,059,200 B	2,880 B	368,640 B	368,640 B
R/O time	*691 µ s*	*88 474 µ s*	*23 µ s*	*2 949 µ s*	*2 949 µ s*
ODR	172,800 B	22,118,400 B	5,760 B	737,280 B	737,280 B
1000MB/s	*173 µ s*	*22 118 µ s*	*6 µ s*	*737 µ s*	*737 µ s*
Disk	172,800 B	22,118,400 B	5,760 B	737,280 B	737,280 B
170MB/s	*1 016 µ s*	*130 108 µ s*	*34 µ s*	*4 337 µ s*	*4 337 µ s*
Max R/O time	***3 072 µ s***	***393 216 µ s***	***307 µ s***	***39 322 µ s***	***39 322 µ s***
Min Freq	0.33 kHz	0.00 kHz	3.26 kHz	0.03 kHz	0.03 kHz
Min. evts Freq		0.33 kHz		3.26 kHz	3.26 kHz
			19MB/s		

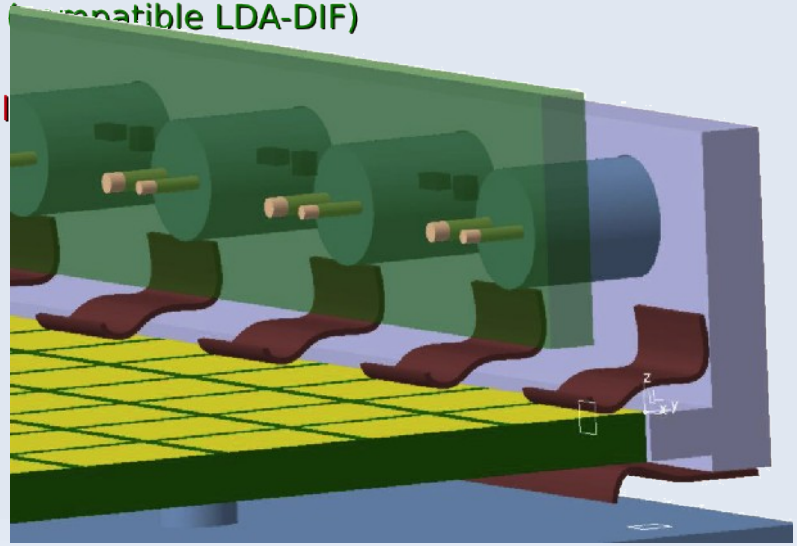
Occupancy for 100 GeV π in TB evts	
Mean	4.8
sigma	2.6
+3σ /√MemSize	5.49

Parameters codes
Hardware (~fixed)
DAQ (achievable)
Physics (occupancies)

Beam InterFace card







Beam InterFace card

Basis:

- CALICE chips use auto-trigger
  - Readout can be triggered by single event using external trigger (e.g. beam hodoscope)

    → “Single event” mode

    History of Chip is usable (e.g. in case of selective ext. trigger)
  - Readout triggered by environmental internal or extern trigger
    - Chip full
    - ILC-like mode (end-of-spill)
- Require some device to readout the beam line parameters
  - Scintillators; Cherenkov PM (coding of CEDAR bits)
  - Time of event (⊃ rec for wire chambers) within a 5 MHZ clock period

Implementation

- 2 solutions
  - Add-hoc card for interfaces with a CALICE ROC (SPIROC ?) + 1 DIF
  - Small adaption (buffers) card on a DIF + “simulation” of a digital ROC in the FPGA
    - Part of the coding can be “tricky”
- Both offer full compatibility with CALICE DIF for the DAQv2.
- To be implemented for 2nd version of CALICE beam test
- One of the task of AIDA (WP8.6.2)
  - For “standalone” CALICE tests
  - Functionnalities ⊃ in JRA1 TLU

Use of sub-ns TDC for CERN wire chambers until then ?

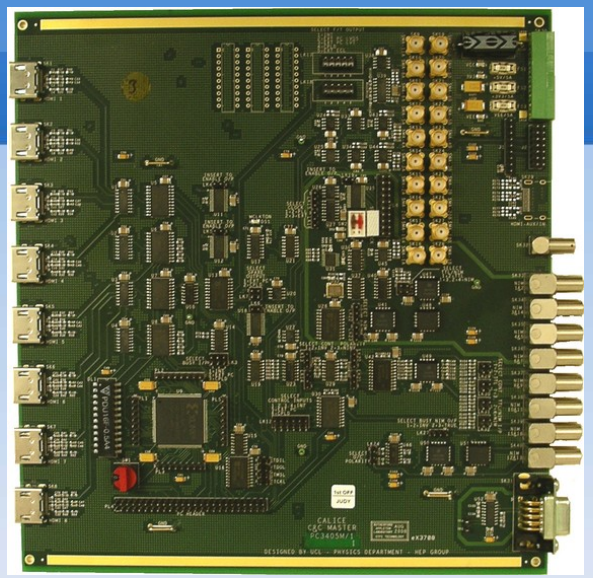
Summary & outlook

- Last months dedicated on bench studies & FW improvement
- CALICE DAQ2 has reach the **deployment phase → ready for large TB**
  - TB of SDHCAL with 400,000 channel next week with RPC (HardROC) & µMegas (MicroROC)
  - ECAL & AHCAL new electronics test bench
- HW ~ stabilized
  - Improvement of existing cards (LDA, CCC) foreseen
  - Beam InterFace card too be designed
- FW & SW in early functionnal version
  - Clean-up and part-rewriting needed
  - Improvement of diagnosis tools needed
  - Integration with environment (beam) to be done
- AIDA (co-running of CALICE & EUDAQ → common DAQ)
  - Specifications to be decided in next months

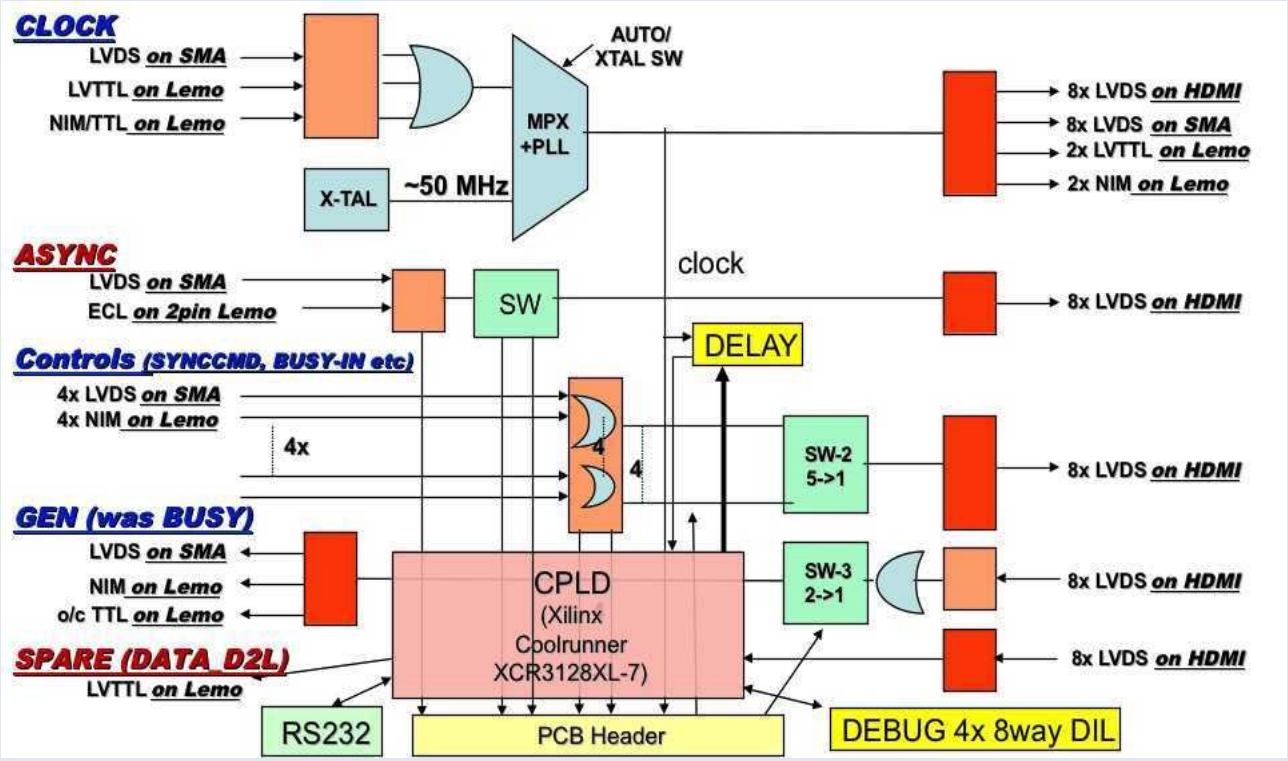
Big effort for CALICE!!
~15++ individuals from:
- UK: CAM, MAN, UCL, RHUL
- FR: LLR, LAPP, IPNL
- DE: DESY

Back-up

Clock and Control Card



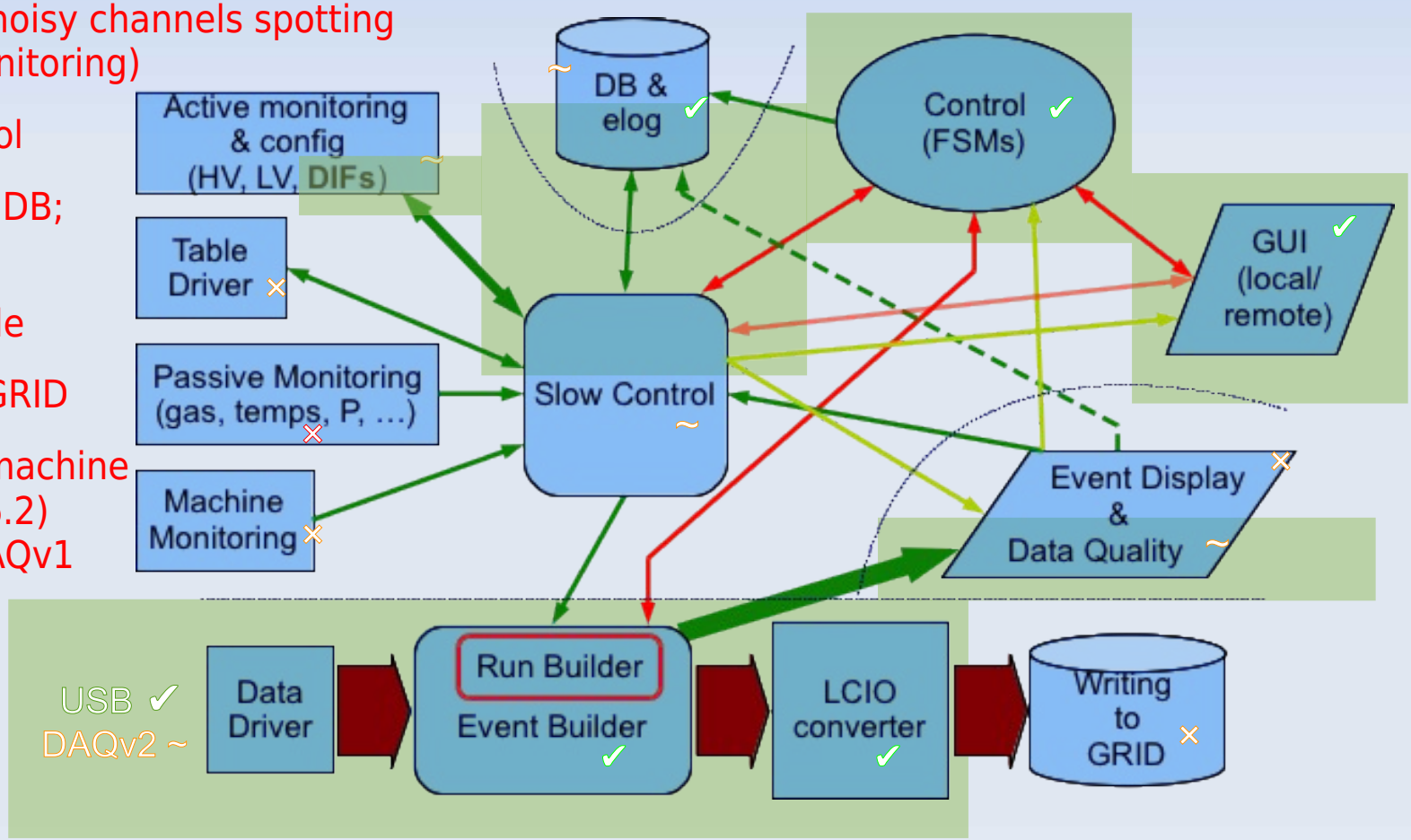
- Developed at UCL (M. Warren, M. Postranecky)
- Distributes on 8 channels (HDMI, SMAs, NIM, …) via dedicated circuitry for **low jitter**
  - Int | ext clock
  - Fast Signal (Trigger | Sync)
- Sums-up BUSY
- Performs Trigger logics
  - CPLD
- Was used as DIF-Master (dev^{t} of LAPP)
  - Aka also sending hard-coded commands to DIF directly
  - Standalone tests with USB readout



SW status

- Missing critical elements
  - Configuration DB (being worked on)
  - DAQ2 interface ↔ XDAQ being worked on
- Missing ancillaries
  - Semi-automatic noisy channels spotting & correcting (monitoring)
  - Clean Slow control
  - interface to CondDB;
  - event display : DRUID on LCIO file
  - interface to the GRID
  - interface to the machine (⊃ in AIDA WP8.6.2) Code exists in DAQv1

Implemented



Back up

Note

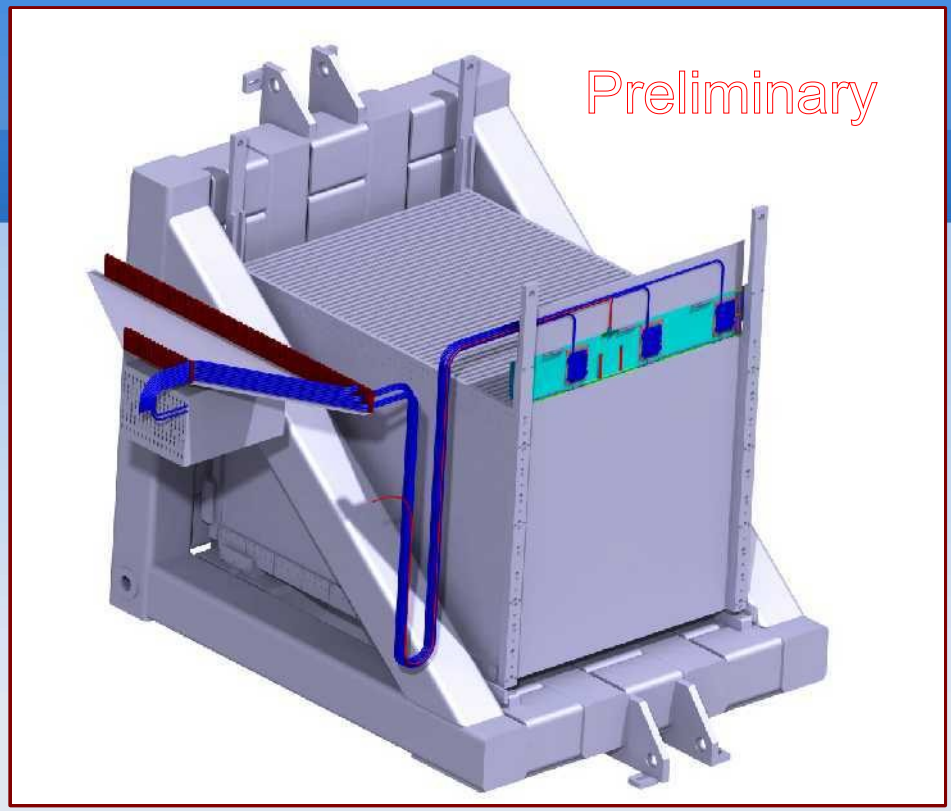
HW availability

Card	#Avail	#Tested	#OK	Remark
PC	6	6	6	OS needs upgrade
ODR	10	4	4	(commercial board: no expected default)
LDA	25	22	17	
HDMI Mezzanines	30	24	**13**	4 have faulty connectors and are being repaired. Not all cards have 10 conn. working
GEth mezzanines	25+5	25	20	2 can easily be recovered
CCC Adapter	25	17	16	Limits # of installations
CCC	10	10	**10**	term adaptation maybe be needed
DCC	2+20	22	21	1 faulty channel on 1 card; 1 burned to be repaired
ECAL DIF	29	29	29	equipement for 11 additional ones avail.
SDHCAL DIF	190	190	183	7 being refurbished; mods needed for HR2 (ok for HR2b)
AHCAL DIF	4*			*Being produced

All basic HW avail.

Complete list of HW pieces & location available on https://twiki.cern.ch/twiki/bin/view/CALICE/HardwareList

Cables



Check F. Davin presentation

- CERN requires halogen free cables
  - “IS23 does apply to above-ground installations and experiments.”
- On shelf: only for HiFi freaks (or Pigeons):
  - beautiful 100€ apiece 5m-long shielded HDMI cable
- 1 reasonable offer:
  - On demand PolyEthylene coating
  - ~ 25€/cable (5m long, ∅ 8.5mm) for 200+ cables.
  - pbm: 12 weeks delais
  - ~ enough funds on ANR to buy for the m³ SDHCAL (150 needed)
    - Urgent : 12 weeks delay due to boat shipping from China
    - Other demands being surveyed:
      - µMegas (~30 ?)
      - AHCAL (50) and ECAL (30)
      - + 10% spares (enough ?) → 260–275