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Experience with 3D integration technologies in the framework of the ATLAS pixel detector upgrade for the HL-LHC

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Experience with 3D integration technologies in the framework of the ATLAS pixel detector upgrade for the HL-LHC

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ABSTRACT

3D technologies are investigated for the upgrade of the ATLAS pixel detector at the HL-LHC. R&D focuses on both, IC design in 3D, as well as on post-processing 3D technologies such as Through Silicon Via (TSV). The first one uses a so-called via first technology, featuring the insertion of small aspect ratio TSV at the pixel level. As discussed in the paper, this technology can still present technical challenges for the industrial partners. The second one consists of etching the TSV via last. This technology is investigated to enable 4-side abuttable module concepts, using today's pixel detector technology. Both approaches are presented in this paper and results from first available prototypes are discussed.

1. Introduction

Interest in 3D technologies has been growing within the High Energy Physics (HEP) community in the past years. 3D technologies can be used to build hybrid pixel detector modules for application in high luminosity experiments, featuring increased functionality, high density and low mass. For the upgrade of the ATLAS pixel detector at the High Luminosity Large Hadron Collider (HL-LHC), R&D is ongoing on different 3D projects. The full 3D integration process is considered to build 3D ICs for the innermost detector layers. Post-processing 3D technologies, namely Through Silicon Via (TSV), are investigated to build compact hybrid pixel modules for the outermost detector layers, using standard pixel FE technology.

The 3D IC discussed in this paper is made of a vertical stack of two electronic tiers, using a via first 3D integration technology. In a via first process, TSV are formed before or after completion of FEOL[3], and are inserted within the pixel. The typical via opening in a via first process is 1–3 μmm, with a depth around 5–15 μm, requiring aggressive wafer thinning. The achievable via pitch is in the order of 2–10 μm. Using vertical integration, the different chip functionalities (such as for instance analog, digital, power) can be split over different layers, allowing to reach smaller pixel sizes, with increased functionality compared to a traditional mixed-mode IC design. Moreover, 3D integration allows to use dedicated technologies for the different layers, and thus optimize the performance of each tier. Fig. 1 shows as an example a possible 3D version of one pixel cell of the FE-I4 [1], the new generation ATLAS pixel Front-End (FE) chip. This could be a 3D stack of two tiers, containing the analog and digital part of the chip. For the analog tier, a 130 nm CMOS process could be used, as for the FE-I4, to keep the same analog performance. For the digital tier a smaller technology node (90 or 65 nm CMOS) could be chosen. In this way more functionality and memory could be added within half the pixel size. These features would allow to cope with the high hit rate to which the innermost layers of the detector will be exposed at HL-LHC.

Post-processing TSV is a via last technology, i.e. vias are formed after BEOL,[4] on the fully processed CMOS wafer. This allows to use the technology on existing pixel FE electronics. In this application, vias are etched in the peripheral bond pads. The via pitch is defined by the pitch of the chip wire bond pads, typically 100–150 μm for HEP ICs. The required wafer thickness is in the order of 80–150 μm. Using TSV the electrical connection to the module is brought to the FE back side. As the front side pads are not used for wire bonding, the height of the periphery can be

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[3] Front End Of Line (FEOL) is the step in the IC fabrication process where transistors are formed on the silicon wafer.

[4] Back End Of Line (BEOL) follows FEOL in the IC fabrication process. In this process step, the individual devices are connected using metal interconnect layers.

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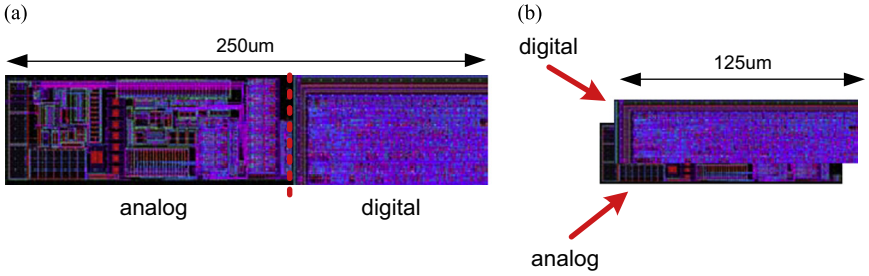

Fig. 1. Layout of one pixel cell of the FE-I4 (a), showing the analog and digital part. The pixel size is $50 \times 250\ \mu m^2$. Illustration of a possible 3D implementation of the FE-I4 (b), with split analog and digital functionality over two tiers, with a pixel size of $50 \times 125\ \mu m^2$.

reduced, leading to a reduction of the inactive area of the chip. It is demonstrated with the Medipix3 pixel chip that the inactive area shrinks from 18 to 6% of the total chip area [2]. Via last TSV can thus enable compact, low mass hybrid pixel detectors, with minimal modification to the traditional FE electronics design, and using standard CMOS technology. Four-side abuttable module concepts can then be achieved using a dedicated sensor layout (i.e longer, or ganged pixel on one sensor side). Modules featuring via last TSV can be used for the outermost pixel layers at the HL-LHC, where tileable modules are beneficial to provide full coverage over the large detector area.

Results presented in this paper cover the 3D IC effort carried out in collaboration with Tezzaron/Global Foundries, and the post-processing TSV process of the Fraunhofer Institute for Reliability and Microintegration (IZM, Berlin).

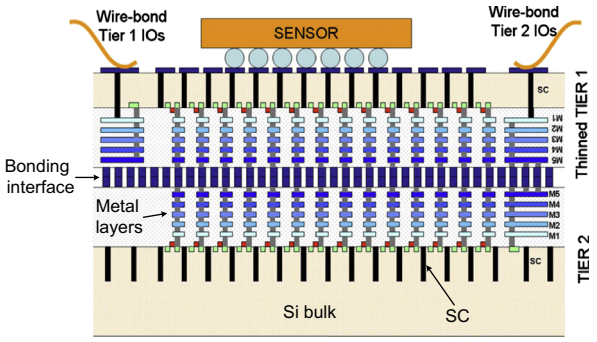

Fig. 2. Sketch of a two tier 3D assembly with the Tezzaron/Global Foundries vertical integration process. Tier 1 is thinned and vias are contacted to operate the assembly and connect to a sensor tile. In this configuration tier 2 is left unthinned. It could be thinned as well to access the TSV for connection to a third tier.

2. 3D electronics

The ATLAS pixel 3D chip prototype, the FE-TC4, is part of the first MPW (Multi Project Wafer) run for 3D ICs in HEP. The MPW run is organized by the HEP consortium for 3D circuit design,[5] using the Tezzaron/Global Foundries technology.

Global Foundries provides a commercial 130 nm CMOS technology. The performance and radiation hardness of this technology have been asserted with dedicated MPW runs by the ATLAS pixel collaboration. Different analog prototypes, either full pixel matrix or test structures, have been submitted. Results show that the performance of the Global Foundries 130 nm process is comparable to that of the 130 nm CMOS technology used for the FE-I4 [3].

The 3D processing steps are done by Tezzaron. Fig. 2 shows a sketch of a two tier 3D stack, illustrating the Tezzaron 3D technology. This is a via first technology and vias, called Super Contacts (SC), are formed after FEOL implementation of the Global Foundries technology. Via features are 12 μm depth and 2.5 μm diameter. Fully processed wafers are bonded face-to-face (F2F) with Cu thermocompression, which provides a high density electrical and mechanical connection between the two tiers. After bonding, the top tier is thinned to 12 μm to access the SC. The final step is metalization on the backside of the top, thinned tier to prepare the IO pads. As shown in Fig. 2, IO pads can access either one of the tiers or the entire stack. The 3D stack can have two different profiles, with either tier 1 or tier 2 on top.

All designs in the MPW run with Tezzaron/Global Foundries are two tier designs. To limit production costs, only one set of masks is used, containing both top and bottom designs, i.e. top and bottom wafers are identical. A special mirroring in the design is thus required for correct F2F stacking: half of the reticule contains top tier designs, while the other half contains bottom tier designs. Twenty-four full reticules are available on each wafer, each one divided in sub-reticules, hosting one or more designs.

The FE-TC4 is designed by three institutes of the ATLAS pixel collaboration, namely CPPM (Marseille, France), LBNL (Berkeley, USA), and the University of Bonn (Bonn, Germany). It is made of a stack of an analog and a digital tier. The analog tier is a translation of the FE-I4 prototype chip, the FE-I4 proto1 [4], to the Tezzaron/Global Foundries technology, with some optimization and changes in the chip layout. The analog chip has a matrix of 14×61 pixels, with a pixel size of $50 \times 166\ \mu m^2$. Each pixel consists of a preamplifier with feedback DAC, a second stage amplifier, a comparator with tunable threshold, and injection capacities for testing purposes. In addition to the pixel matrix, the analog tier contains also test transistors to assess the radiation hardness of the technology, as well as bias and configuration circuitry, which allow testing of the tier standalone. For the digital tier two designs are available, called digital complex and digital simple. The design of the digital complex tier follows the 4-pixel digital region design of the FE-I4 [5]. The digital simple tier is devoted to study noise coupling between tiers. To achieve this, every pixel in the digital simple tier contains eleven CMOS counters, so called drum cells, each one facing a sensitive node of the analog tier pixel, and generating electromagnetic noise. Both digital tiers are designed in order to be configured and tested independently, as the analog one.

Designs were submitted in April 2009, and first working 3D assemblies are available since summer 2012. The long fabrication time line is due to multiple issues encountered during the process, starting with design problems connected to design kit and 3D design rules, to fabrication issues, such as for instance, misalignment of tiers during bonding. First results on 3D chips are presented in Section 2.2, after discussing the performance of the

[5] The consortium was founded in late 2008 by 17 HEP groups from six different countries, and it is led by Fermilab.

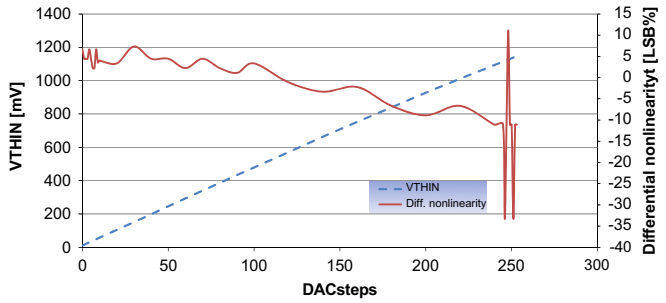

Fig. 3. Results of VTHIN DAC characterization showing the linearity of the output voltage and a maximum DNL 32% of one LSB.

Tezzaron/Global Foundries technology, asserted with tests of the analog tier standalone, in Section 2.1.

2.1. Analog tier characterization

The analog tier is characterized independently to assess the performance of the Tezzaron/Global Foundries process, i.e. the 130 nm CMOS technology from Global Foundries with TSV and bonding interface. The results are compared for reference with those obtained from the characterization of the 130 nm CMOS technology used for the FE-I4 series, a well established and characterized technology, suitable for application in HEP experiments, as well as from the FE-I4 proto1 [4], on which the analog tier design is based.

To assess proper communication to and from the chip, first tests target the shift register used for configuration and readout, DACs for biasing and configuration, and the readout chain. No failure is observed in these blocks. As an example Fig. 3 shows the output of the VTHIN DAC (8-bit comparator threshold setting for the entire matrix) as a function of the DAC step, confirming the expected linearity. The differential nonlinearity (DNL)[6] is also shown on the same plot, expressed in percents of the LSB. Maximum deviation from linearity is 32% of one LSB, i.e. 1.5 mV, showing high accuracy of the DAC.

Important figures to characterize the performance of the analog tier are the threshold and noise distributions. On the untuned chip, a threshold of approximately 1620 e^- is measured with a dispersion of 185 e^-. Tuning the chip at this threshold value reduces the dispersion to 35 e^-. The measured noise[7] is of 66 e^-. This result is obtained using bias settings of the analog FE optimized for minimum noise by parametric DAC scans. With these set of parameters a minimum operational threshold of 600 e^- with 60 e^- noise can be achieved. The threshold dispersion is however of 128 e^-. The total current consumption in this configuration is of 9.2 μA per pixel. These results are in good agreement with those on the FE-I4 proto1 characterization, underlining the good performance of the Tezzaron/Global Foundries technology.

To check the radiation hardness of the process, test transistors are integrated in the analog tier design. These are both NMOS and PMOS transistors, with linear (LIN) and enclosed (ENC) layout, and widths of 2.31 μm and 99.28 μm. The influence of the Total Ionizing Dose (TID) is studied using X-rays. Results are mostly in agreement with what has been observed on the 130 nm CMOS technology node used for the FE-I4 series [6]. The two affected transistor parameters are the leakage current and the threshold voltage, and their maximum degradation peaks for NMOS transistors at a dose of a few MRad. In particular, no leakage current is observed for PMOS transistors. NMOS transistors show, for a TID of a few MRad, an increase of leakage current. The leakage current increases of one order of magnitude (up to 10^{-7}A) for the wider transistors, and of almost two orders of magnitude (up to 10^{-8}A) for the narrow ones. Fig. 4 shows the threshold voltage shift of the test transistors for TID up to 160 MRad. These results show some differences with respect to what is observed for the FE-I4 technology, pointing to an effect different from the Radiation Induced Narrow Channel Effect (RINCE) [6] observed for the reference 130 nm CMOS process. Although the variation is of the same order of magnitude as the one observed for the reference process, in the Tezzaron/Global Foundries technology larger transistors show higher threshold voltage shift, and NMOS transistors have a positive shift.

Monitoring of the chip performance during irradiation shows that the current consumption increases to 100 mA at a TID of approximately 1 MRad, and decreases back to the pre-irradiation value (approximately 8 mA) at 10 MRad. The evolution of the noise with increasing TID is negligible (10 e^- at TID of 1MRad), while as shown in Fig. 5, a more relevant shift is observed for the untuned threshold and threshold dispersion values, around 1MRad.

2.2. FE-TC4 characterization

The first 3D wafer delivery was in November 2011. The three bonded wafers received show extensive damage on the surface. Due to misalignment of the tiers during bonding, the mechanical connection between the two tiers is very poor, leading to removal

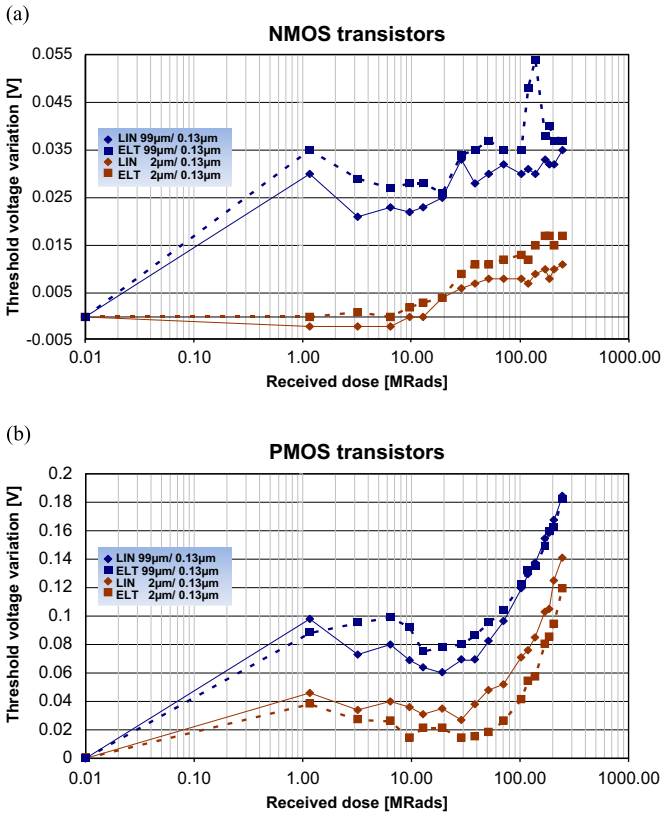

Fig. 4. Threshold voltage variation for NMOS (a) and PMOS transistors (b) with increasing TID.

[6] The differential nonlinearity (DNL) describes the deviation between two adjacent analog values of the DAC, which correspond to two adjacent digital contents of the DAC. For every DAC step the DNL could be expressed with the formula: DNL(n_j)–(n_{j-1})=(Vout$_j$–Vout$_{j-1}$) - V_ideal_LSB_step where n_j denotes the specific DAC step and Vout$_j$ the output voltage of the step.

[7] Note that no capacitive load (i.e. sensor) is connected to the analog FE for these tests.

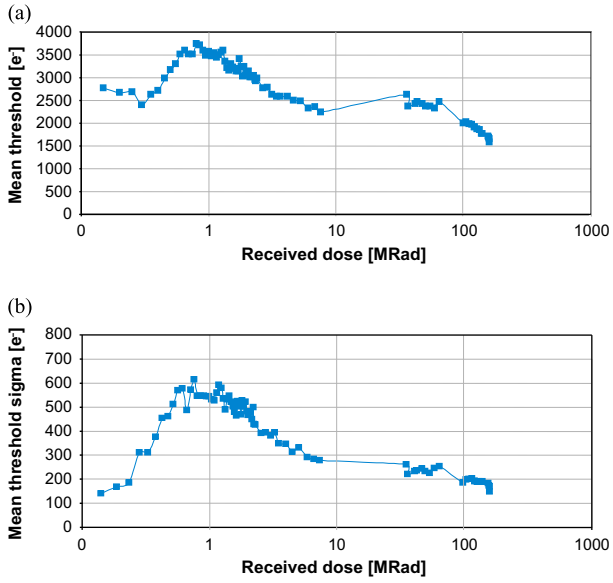

Fig. 5. Evolution of the untuned threshold (a) and threshold dispersion (b) with increasing TID. At a TID of 1MRad, the threshold increases of approximately 1000 e^- and the threshold dispersion of 500 e^-.

of the top wafer during thinning in some areas of the wafer. The electrical connection is as well bad, preventing tests of the complete 3D stacks. Results on these 3D chips thus cover only testing of the analog tier thinned down to 12 μm, and results from the 3D chips with digital simple tier. In particular, tests on the thinned analog tier result in noise figures around 90 e^-, showing a 50% noise increase with respect to the full thickness tier operation.

Interesting results can be obtained from tests of 3D chips with digital simple tier, for which a good electrical connection is not required. Noise is injected from the digital tier to the analog one, and induced fake hits can be readout using the analog tier resources. Stress tests are done on both the analog pixel as a whole, as well as individual parts of the pixel to study the most sensitive circuit blocks. Results show that the most sensitive nodes are the decoupling capacitor of the leakage current compensation scheme and the second stage amplifier, both recording fake hit during stress tests.

The digital simple tier provides as well different shielding types for different double columns (DCs) of the pixel matrix. Three types of shielding are available

- DOWN shielding: implemented in the third metal layer, covers the drum cells only;
- UP shielding: implemented in the 5th metal layer, covers the entire double column; and
- UP & DOWN shielding: a combination of the UP and DOWN shielding in one double column.

The effect of the shielding can be seen in Fig. 6, where the noise, measured with a threshold scan, is shown for the different shielding configurations. DCs with either both or just UP shielding configuration have a noise value similar to the one obtained during threshold scans without stressing the pixels. DCs with DOWN shielding configuration show a higher noise profile around 120 e^-. If no shielding is applied, a significant noise increase is observed. The results of these tests show the importance of the shielding strategy in a 3D stack, as the coupling between the tiers might be quite significant and result in pixel noise increase and fake hit injection. Although both types of shielding show quite good results, the UP configuration, which physically covers the whole DC, is the most efficient. Although pixel stressing has

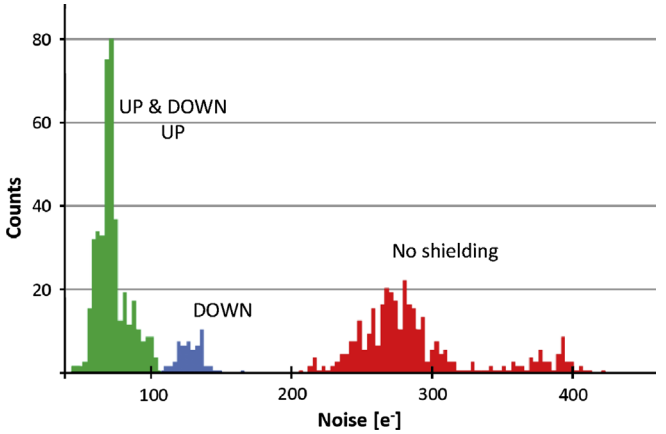

Fig. 6. Noise measured in the analog tier, while injecting noise from the digital tier. Results are depicted for different shielding configurations, showing that shielding plays a significant role in avoiding coupling between the tiers. The noise increases of several hundreds e^- when no shielding is applied.

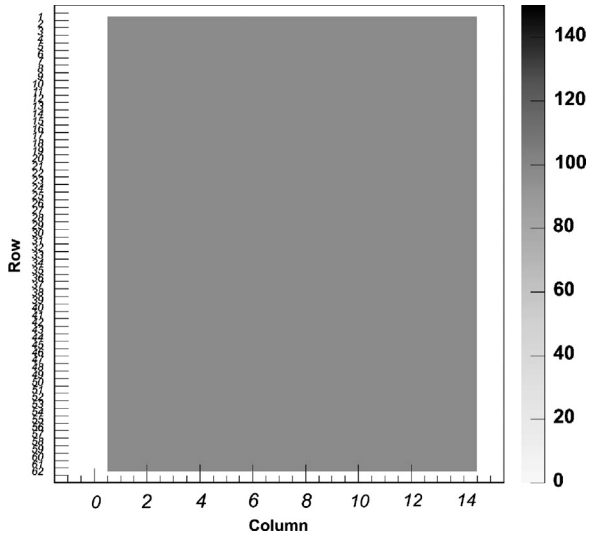

Fig. 7. Analog scan result from a 3D chip, proving that the communication between tiers is working.

significant impact on the noise of the system, it does not seem to affect the threshold value.

In summer 2012, 3D chips have been received with good bonding interface, from a second, better aligned run. The bonding for these 3D wafers is performed both at Tezzaron and Ziptronix. At the time of writing testing is at a very early stage and available results are just preliminary. The most significant test with these 3D chips is to assess the communication between tiers. This can be seen in Fig. 7: 100 hits are injected at the input of the preamplifier in the analog tier and correctly readout from the digital tier. Results on threshold and noise are so far encouraging showing results close to the performance of the analog tier standalone but more investigations are required to fully understand the measurements.

3. Post-processing TSV

R&D on post-processing TSV is carried out in collaboration by the University of Bonn and the Fraunhofer Institute for Reliability and Microintegration (IZM, Berlin). IZM offers two via last TSV processes, namely straight side wall and tapered side wall TSV. The

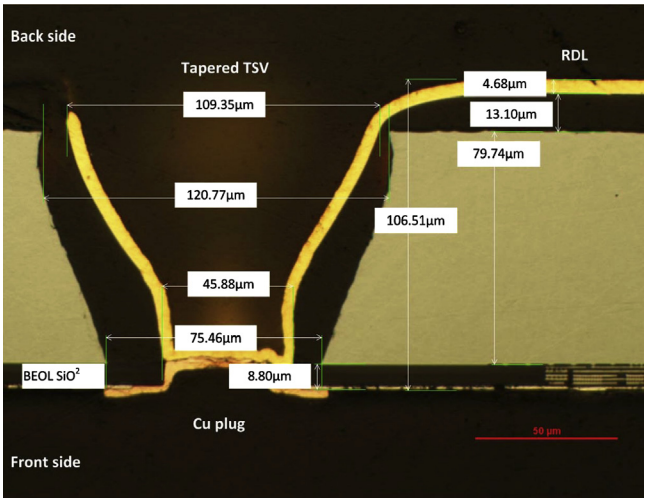

Fig. 8. Tapered profile TSV and plug on the FE-I3 wafers.

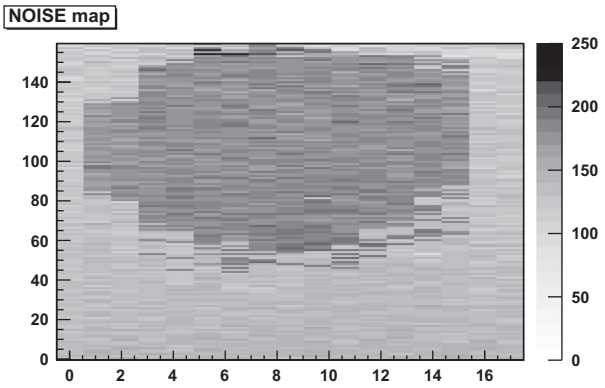

Fig. 9. Noise map of a TSV module. Connected pixels, in the center of the pixel matrix, have higher noise as the connection to the sensor increases the input capacitance seen by the FE preamplifier.

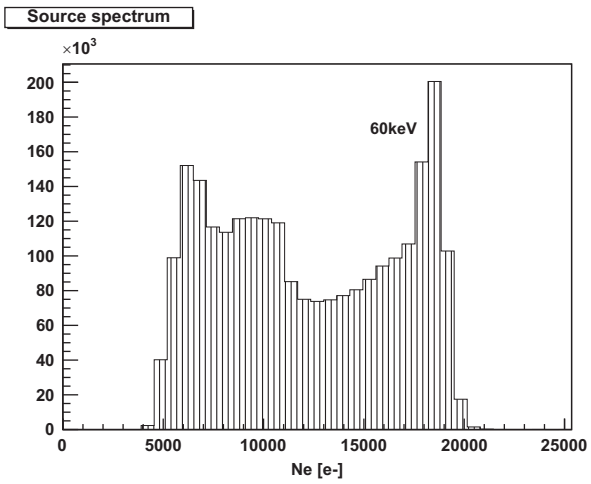

Fig. 10. Spectrum of an Am-241 source recorded with a demonstrator module with TSV (no clustering applied).

first makes use of a standard Bosch process [7], in which etching and passivation steps are alternated. Tapered side wall vias are instead etched in one step and passivation is deposited at the end of the etching process. This technique allows for a simpler deposition process of the isolation layer with respect to straight side wall TSV, using thin film polymers. Both processes are demonstrated on monitor wafers, and the tapered profile via process is selected to prototype demonstrator TSV modules with the ATLAS FE-I3 electronics [8].

Fig. 8 shows a tapered profile via on an ATLAS FE-I3 wafer. Vias are etched in the FE peripheral bond pads, where the pitch is 150 μm. The via top diameter is approximately 110 μm, for a via depth (i.e. wafer thickness) of 90 μm, resulting in a via bottom opening of 45 μm. The connection of the via to the aluminum pad on the FE front side requires a dedicated processing step as only the last metal layer is present in the bond pad in this FE design. The aluminum pad and the BEOL SiO_2 stack underneath are etched from the front side, and a so-called Cu plug is formed to connect the via bottom to the front side pad, as shown in Fig. 8.

For these first demonstrator TSV modules, a simple Re-Distribution Layer (RDL) on the FE back side is chosen which reproduces the front side bond pads. The wafer is then processed for bump bonding to a sensor tile using a standard flip chip process, i.e. no handle wafer is used during reflow as it is normally the case for thinned ATLAS chips. It is therefore expected that the thin FE bends up at the corners due to the high temperature used in the reflow process (in this case up to 260 °C), and that only an area in the center of the pixel matrix is connected to the sensor.

Fig. 9 shows the noise map of a TSV module operated using the connection on the FE backside. Two areas can be clearly distinguished, with different noise values, indicating connected pixels at the center of the module, and unconnected pixels along the perimeter of the FE, as expected. Noise figures for both connected and unconnected pixels are approximately 180 e^- and 130 e^-, respectively, and compare well with the noise figures from FE-I3 bare chips and modules operated with the standard front side connection [9]. The module can be operated with threshold values down to 2000 e^-, in agreement with what has been observed on ATLAS pixel FE-I3 modules [9].

To assess full module operation, the spectrum of a radioactive source (60 keV gamma rays) is recorded. The spectrum is shown in Fig. 10 demonstrating that the TSV processing is successful throughout, such that the operation of the module suffers no loss in performance.

A detailed description of the TSV process on the ATLAS FE-I3 electronics and the results of the TSV module characterization can be found at [10].

4. Conclusions

For the upgrade of the ATLAS pixel detector at the HL-LHC, different technologies are investigated to build modules able to cope with high hit rate and radiation levels, while having high resolution and low material. One possibility to meet these requirements is offered by 3D integration technologies. In particular, 3D IC design and post-processing TSV are investigated.

IC design in 3D (via first technology) allows to reach small pixel size with high functionality and low power consumption, which are beneficial for application in the innermost layers of the detector. 3D integration technologies are however not yet mature for mass production, and technical issues can still arise during production. In the case of the ATLAS pixel 3D prototype chip, the FE-TC4, developed with Tezzaron/Global Foundries technology, many issues have been encountered, from wafer ordering to fabrication. First prototypes are available only 3 years after submission. Results are however very positive. The Tezzaron/Global Foundries technology performance has been fully characterized, including radiation hardness, and proved to be suitable for application at the HL-LHC. Preliminary results on 3D chips show so far good functionality.

Post-processing TSV, a via last technology, offers on the other hand the possibility to improve the design of standard hybrid pixel modules for the outermost detector layers towards compact, four-side abuttable modules. A via last TSV technology has been successfully demonstrated. ATLAS pixel electronics wafers have been processed with the tapered via last TSV process from IZM Berlin. Results from first demonstrator modules show no performance degradation with respect to standard modules.

In order to establish these technologies for application at the HL-LHC further prototyping is planned, namely a second 3D submission and processing of FE-I4 wafers with via last TSV.

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