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Presentation

Development of front-end electronics for LumiCal detector in CMOS 130 nm technology

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AGH University of Science
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Development of Front-end Electronics for LumiCal Detector in CMOS 130 nm Technology

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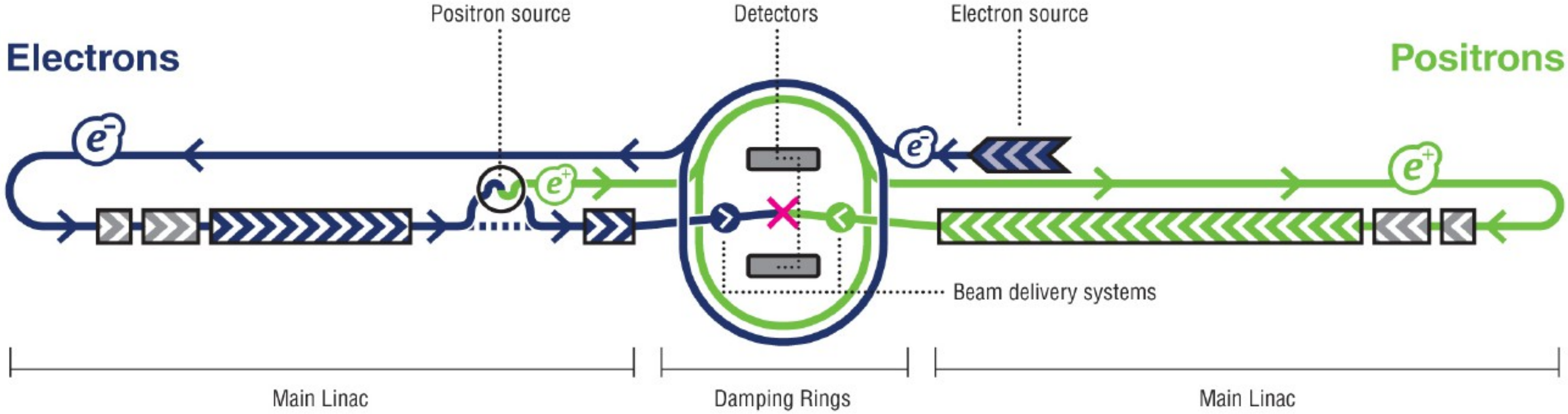
TWEPP Topical Workshop on Electronics for Particle Physics, 22-26 September 2014, Aix en Provence, France

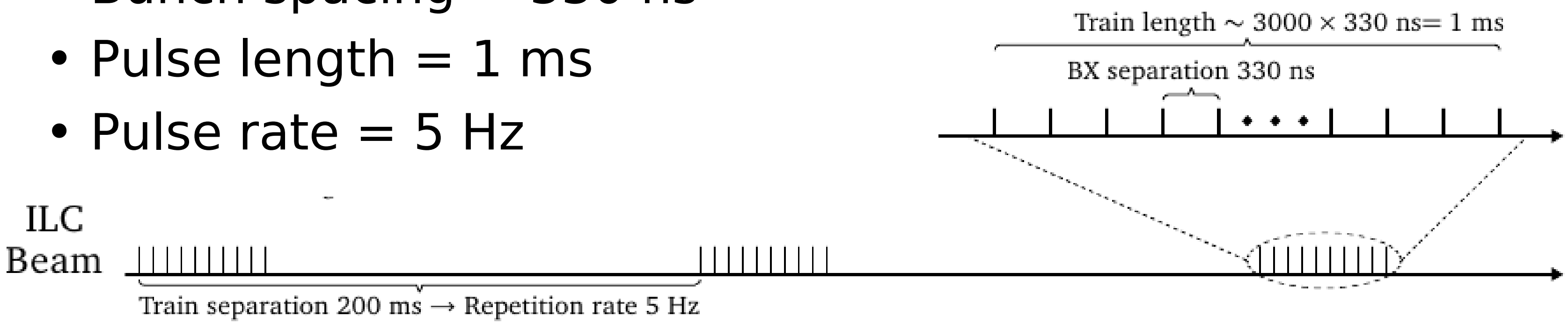
Agenda

- Motivation
- Analog Front-End
  - Architecture
  - Simulations
  - Measurements results
  - Deconvolution performance
- Summary

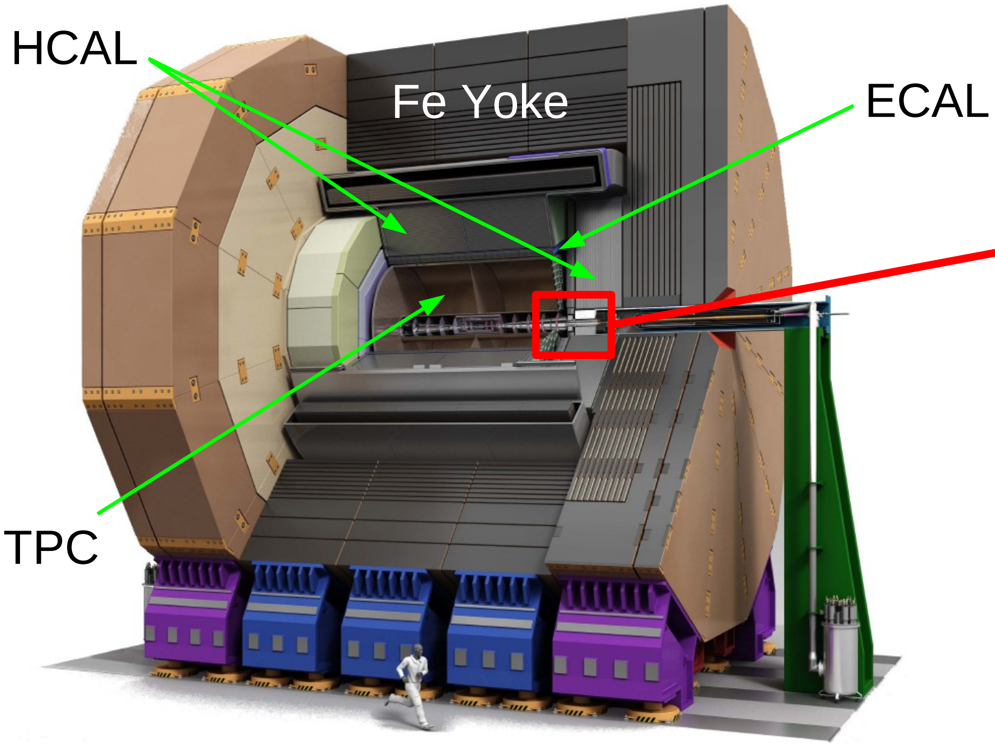
International Linear Collider (ILC) Schematic layout and beam structure

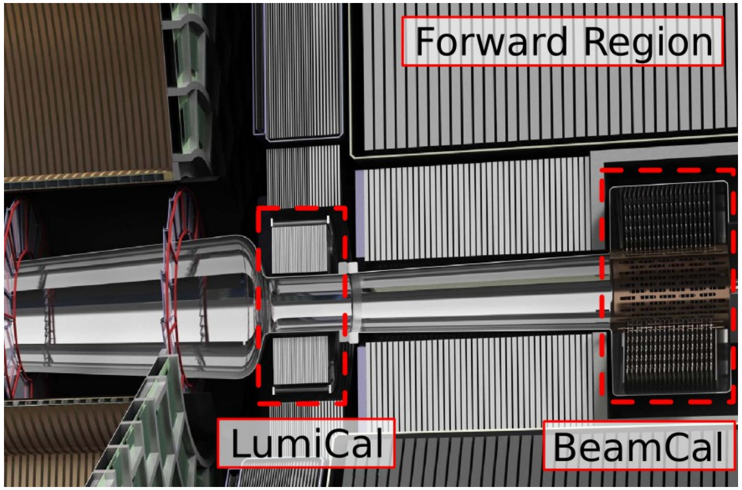


- Center-of-mass energy = 500 GeV
- Peak luminosity = 2 x 10^{34} $cm^{-2}s^{-1}$, particles per bunch = 2 x 10^{10}
- Bunch spacing = 330 ns
- Pulse length = 1 ms
- Pulse rate = 5 Hz



International Linear Collider (ILC): International Large Detector (ILD)





- Beam monitoring:
  - **LumiCal – luminosity calorimeter**
  - BeamCal – beam monitor

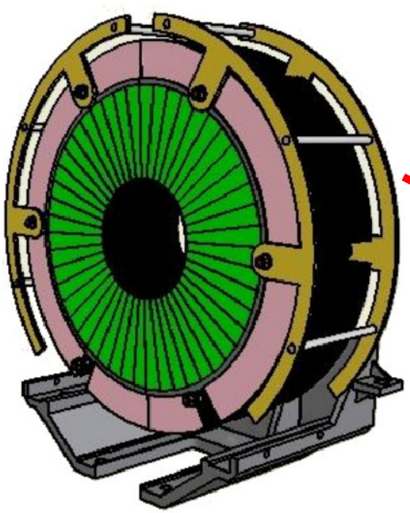
- Particle detectors:
  - Time Projection Chamber (TPC) – tracking
  - Electromagnetic/Hadronic Calorimetes (E/HCAL) – calorimetry
  - Fe Yoke – muon system

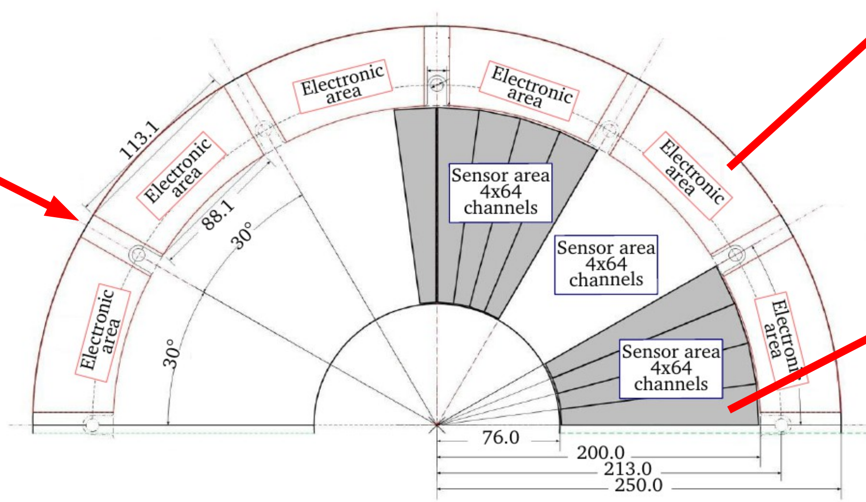
Luminosity measurements at ILC
LumiCal – dedicated luminosity calorimeter

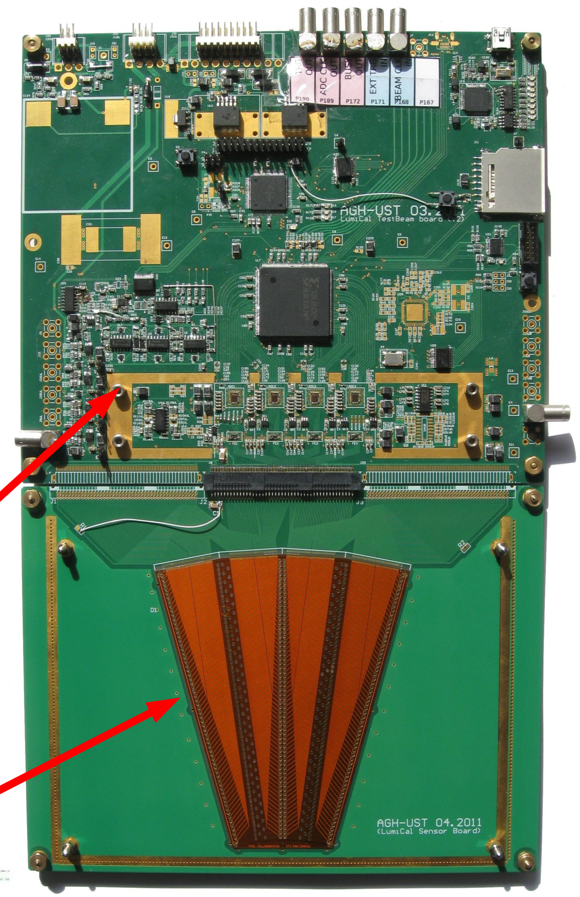
- Gauge process for luminosity measuremet - Bhabha scattering with $\sigma \sim \theta^{-3}$
- Main **LumiCal** features:
  - 30 layers of tungsted + silicon detectors
  - Each layer – 12 sensors with 4 sectors each
  - Each sector divided into 64 radial pads

  → 3072 channels in single layer

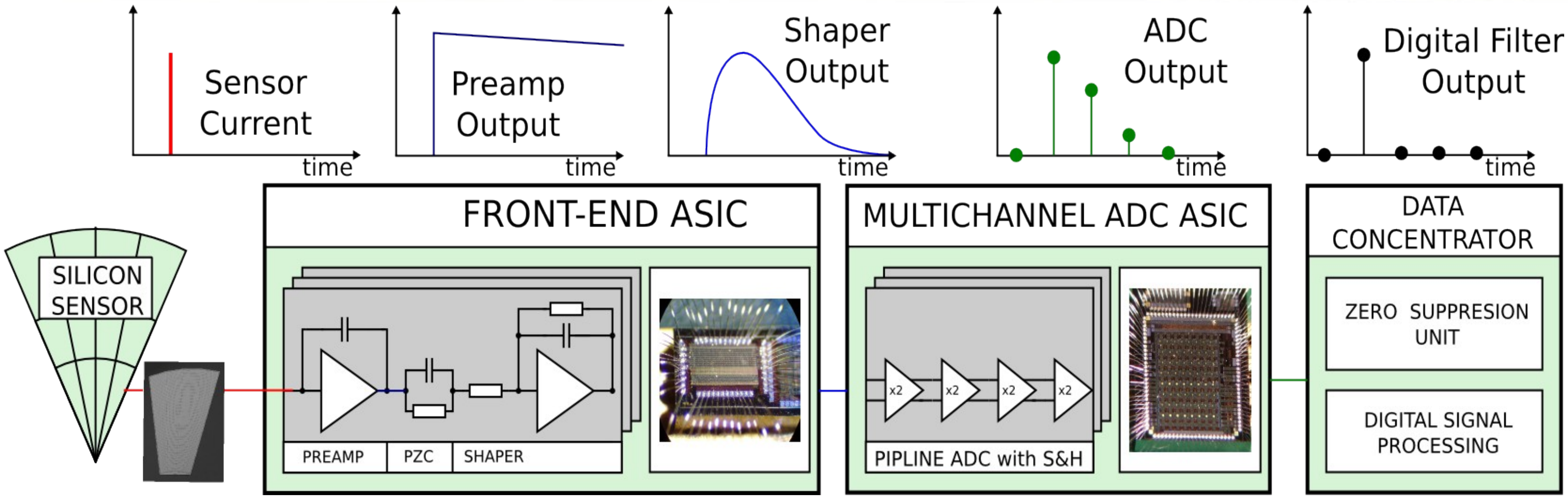
  → 92 160 channels on the entire barrel







Luminosity measurements at ILC: LumiCal readout chain



Existing LumiCal detector readout comprises:

- 8 channel front-end ASIC with preamp & CR-RC shaper Tpeak~60ns, ~9mW (**AMS 0.35um**)
- 8 channel pipeline ADC ASIC, Tsmp<=25MS/s, ~1.2mW/MHz (**AMS 0.35um**)
- FPGA based data concentrator and further readout

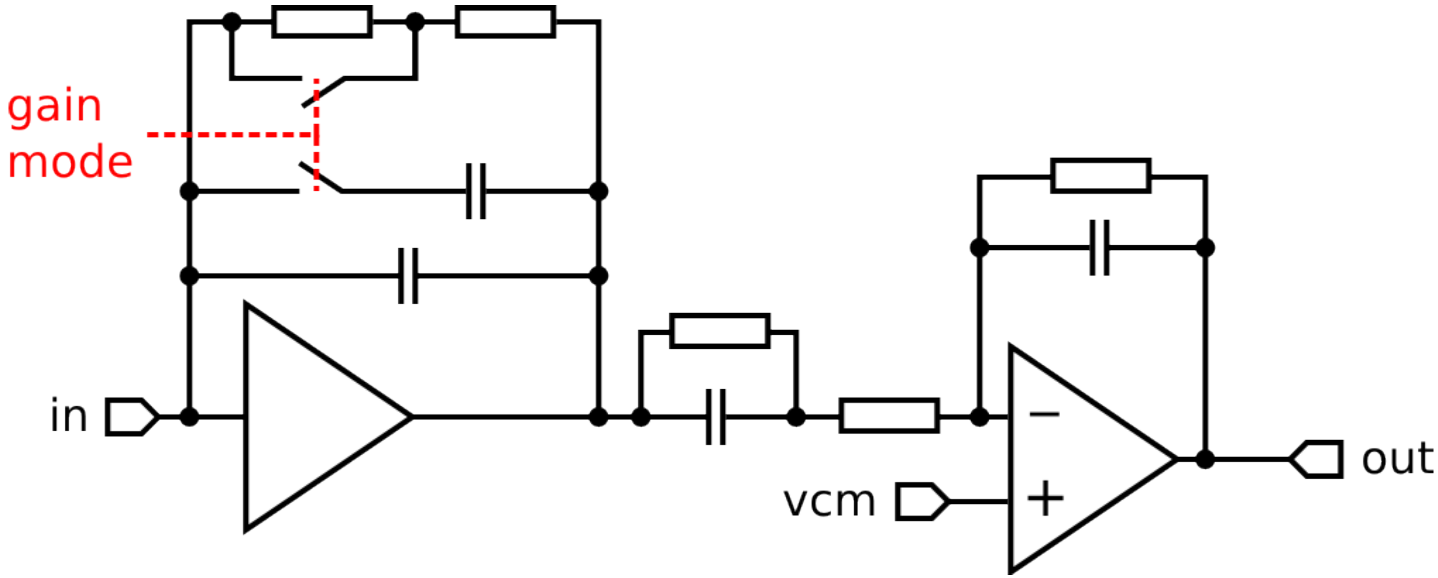
New developments for LumiCal detector readout:

- Prototype front-end ASIC in CMOS 130 nm under development... (main subject of this talk)
- Prototype SAR ADC ASIC in CMOS 130 nm – fabricated, tested and working well, already presented at TWEPP2013. New 8-channel version waiting for tests

LumiCal front-end in CMOS 130 nm Specifications

- CMOS 130 nm technology
- Analog Front-End and ADC conversion in each channel
- Detector capacitance $C_{det} \approx 5 \div 50$pF
- At present stage CR-RC shaping with peaking time $T_{peak} \approx 50$ ns, allows strightforward deconvolution implementation at asynchronous test-beam sampling
- Variable gain:
  - calibration mode - MIP sensitivity
  - physics mode - input charge up to ~6 pC
- Noise: ENC ~ 1000e^{-} @10pF
- Crosstalk < 1%
- Analog Front-End power consumption ~1.5 mW/channel
- ADC 10-bit resolution, F_{sample} > 20 MSps (asynchronous read-out), power<1 mW
- Power pulsing – average power will be decreased by ~10^{2}

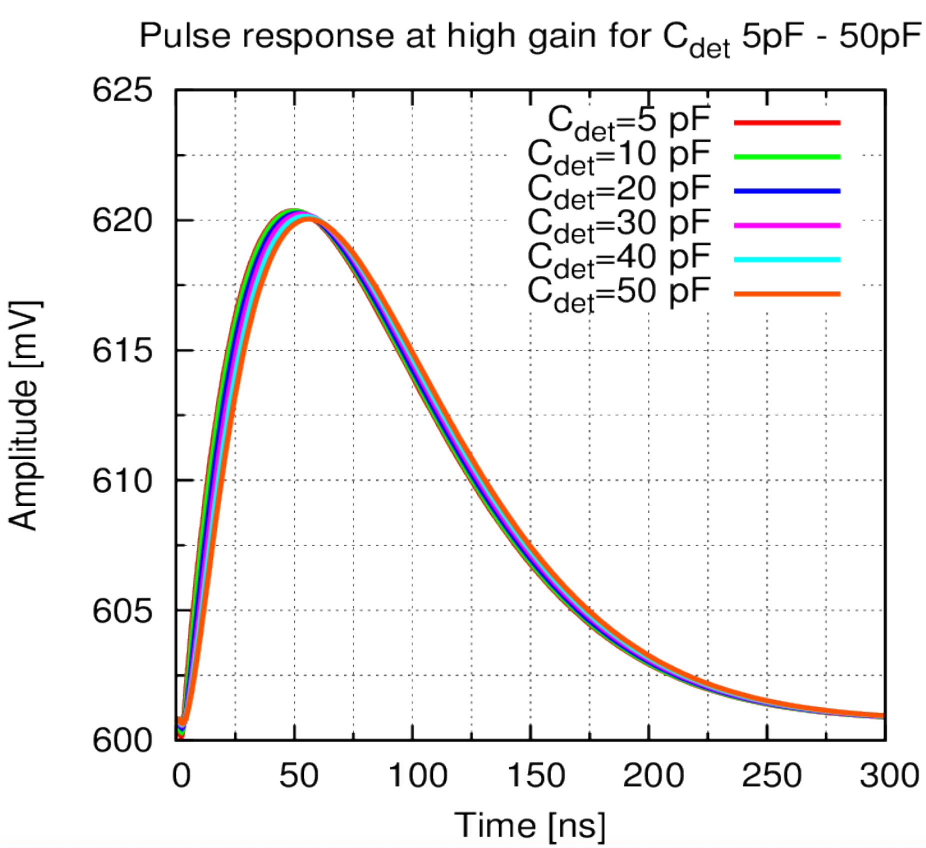
Analog Front-End Architecture

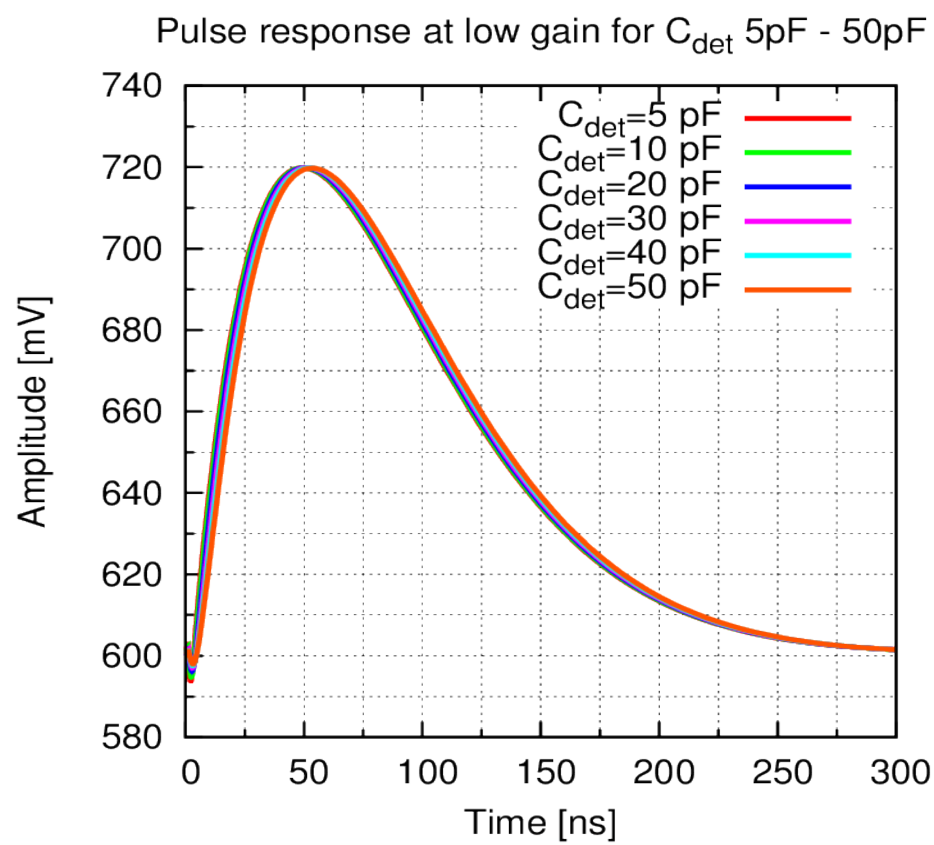


- Preamplifier + PZC + CR-RC shaping
- Two gain modes (calibration and physics) applied by switching R,C components in preamplifier feedback circuit
- Preamplifier – telescopic cascode with boosting amplifiers
- Shaper amplifier – recycled folded cascode (RFC)

Analog Front-End simulations
Pulse response

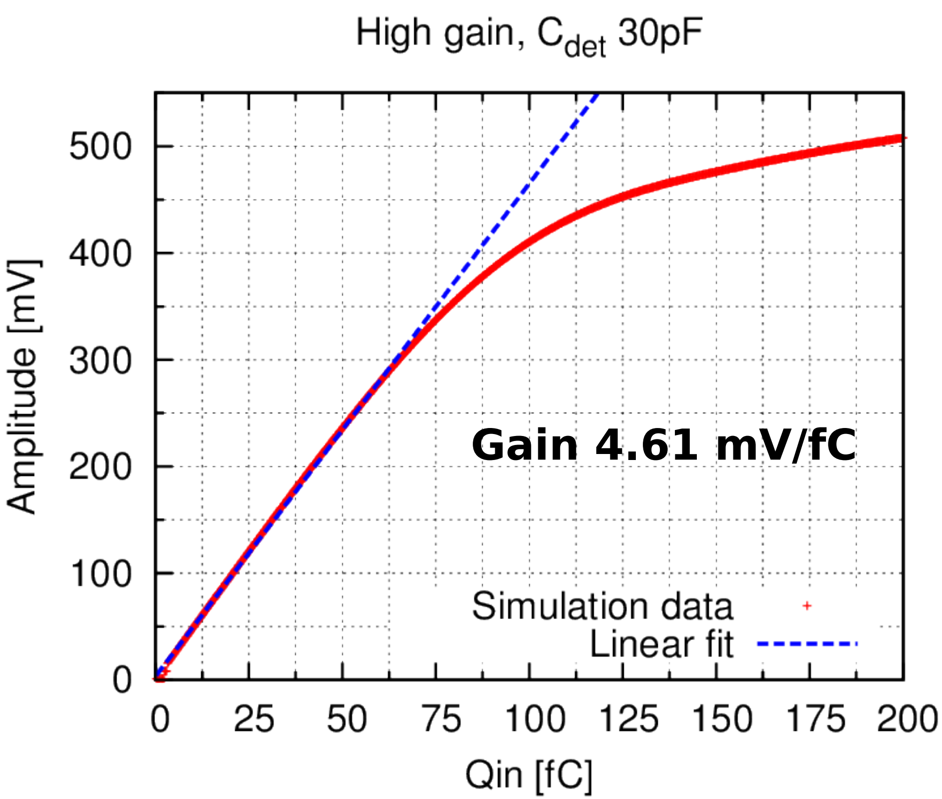
- Pulse response for both gains for various detector capacitance Cdet:
  - Pulse for Q_{in}=4 fC (1 MIP) in high gain mode on the left
  - Pulse for Q_{in}=1 pC (250 MIPs) in low gain mode on the right

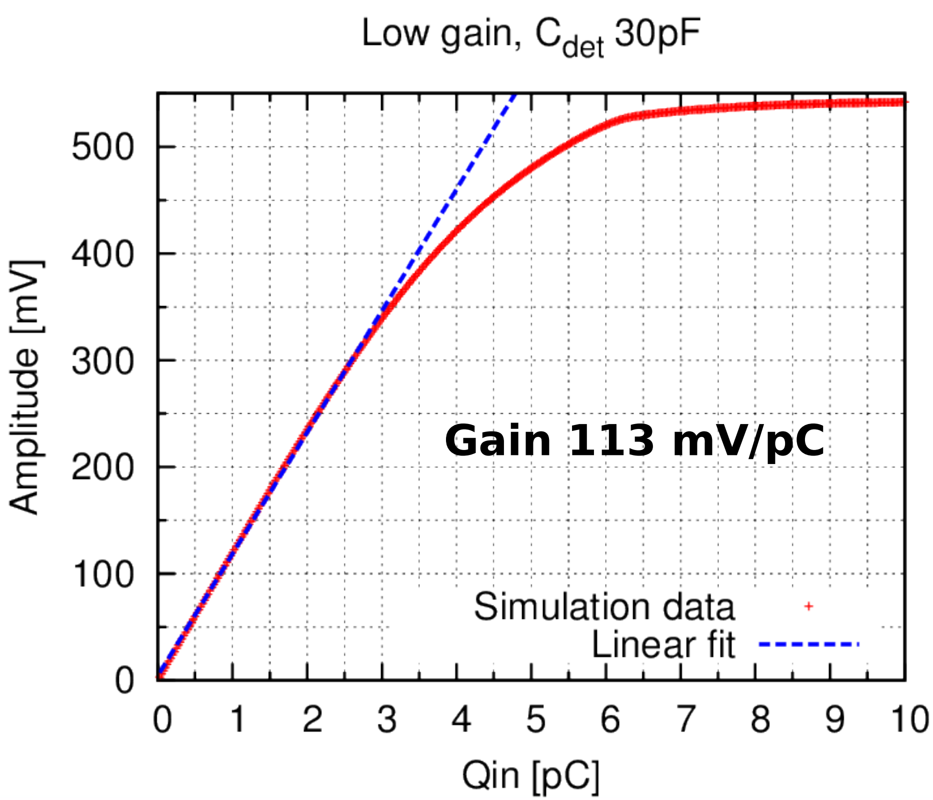




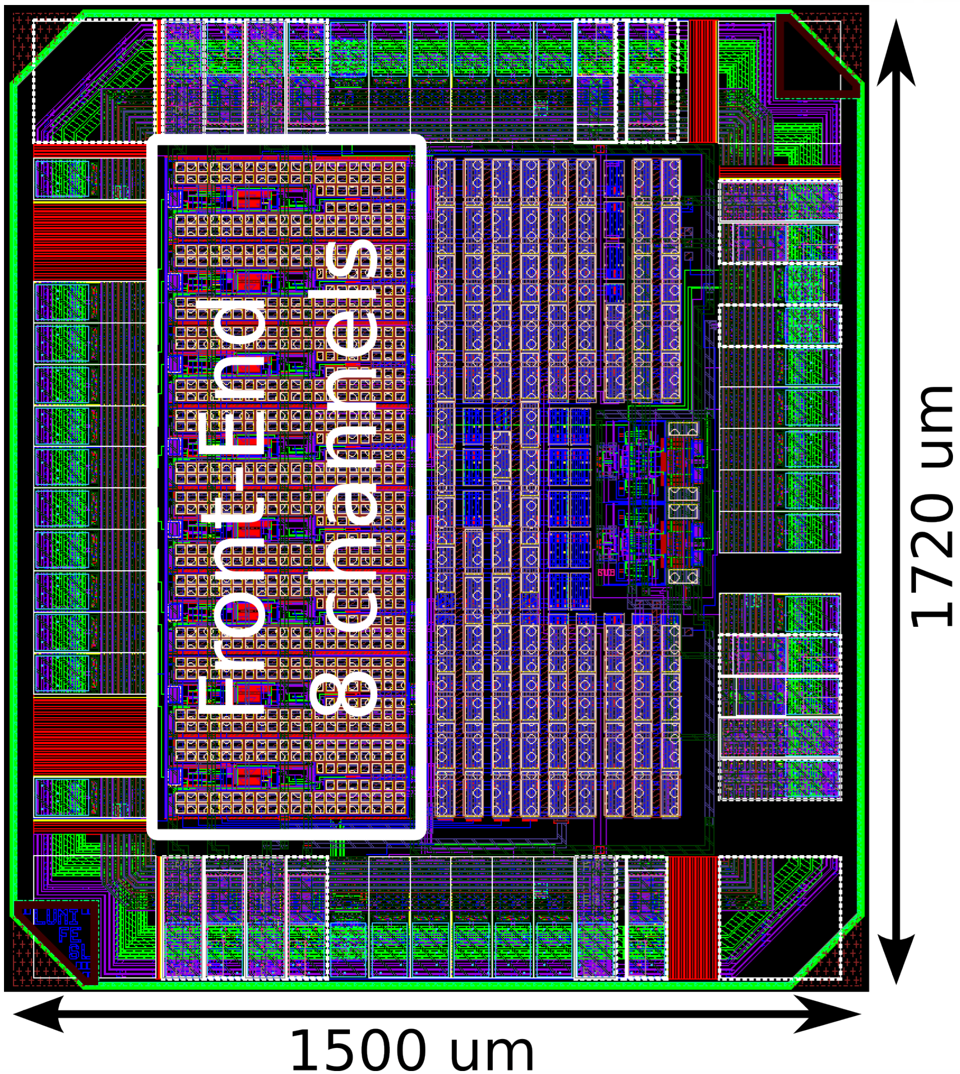
Analog Front-End simulations Linearity

- **Two gain modes in Front-End:**
  - Position calibration with muons – sensitivity for MIP (~4fC) – **high gain**
  - Luminosity measurement – high energy particle → electromagnetic shower → charge deposition up to few pC – **low gain**

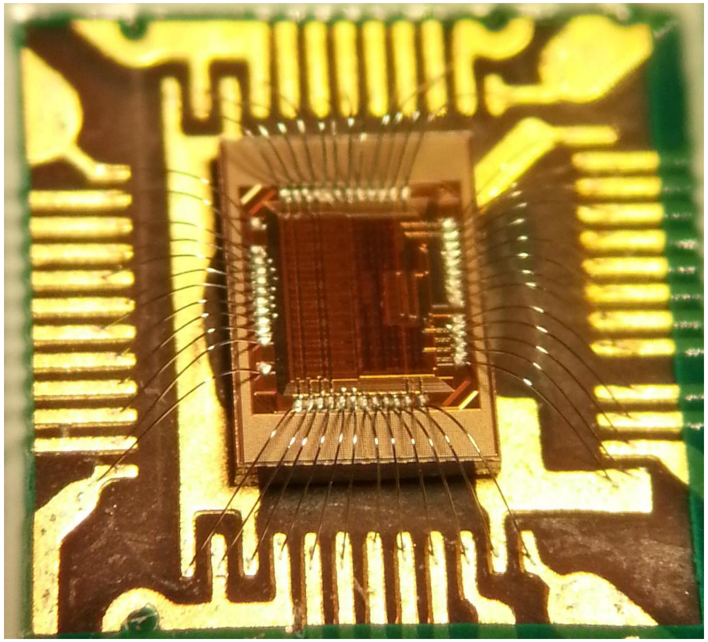




Analog Front-End Prototype ASIC

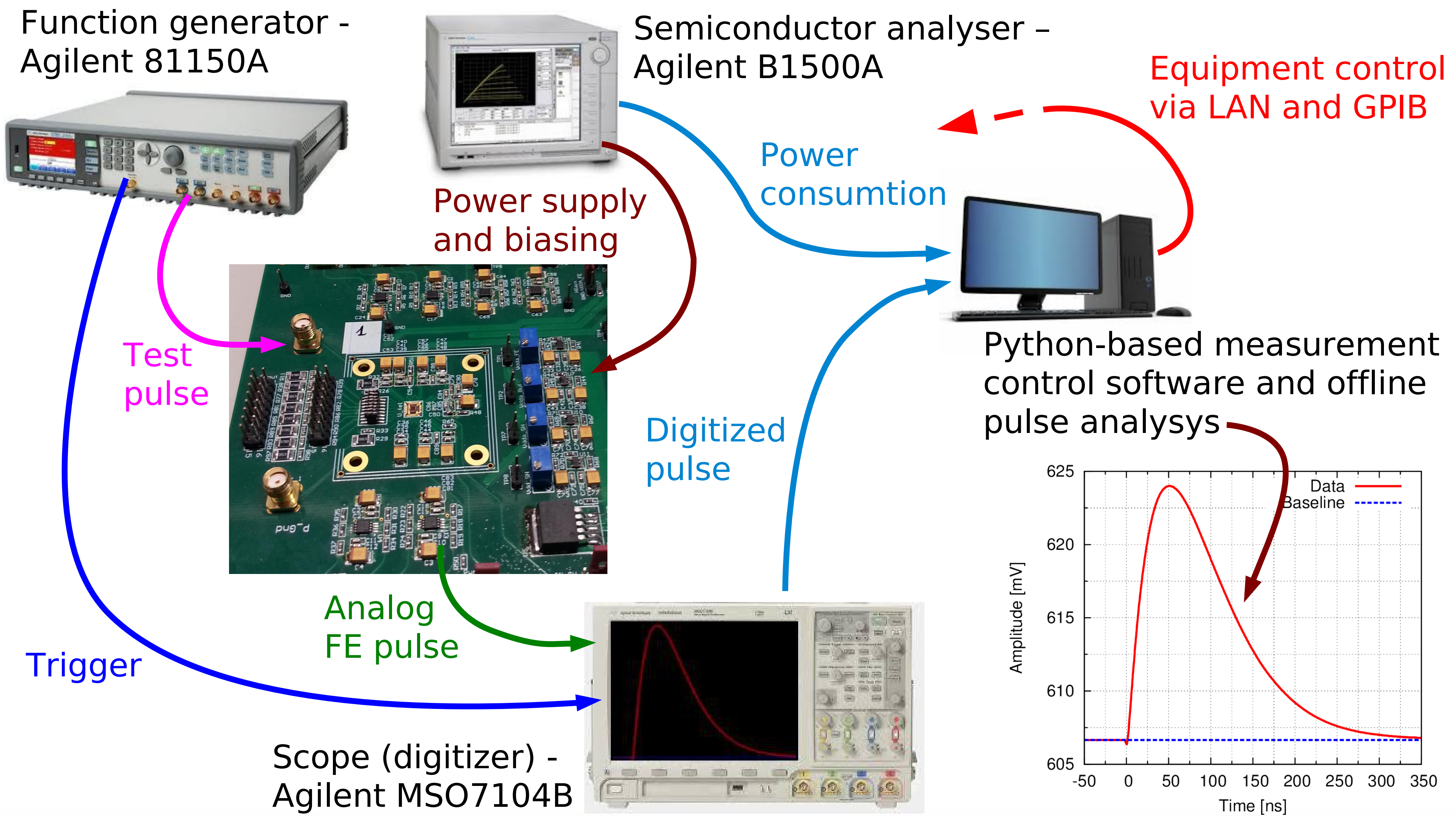


Front-end ASIC prototype contains:
- 8 channels of Preamplifier&Shaper in pitch of 140 um
- 2 channels of Single-to-Differential converter



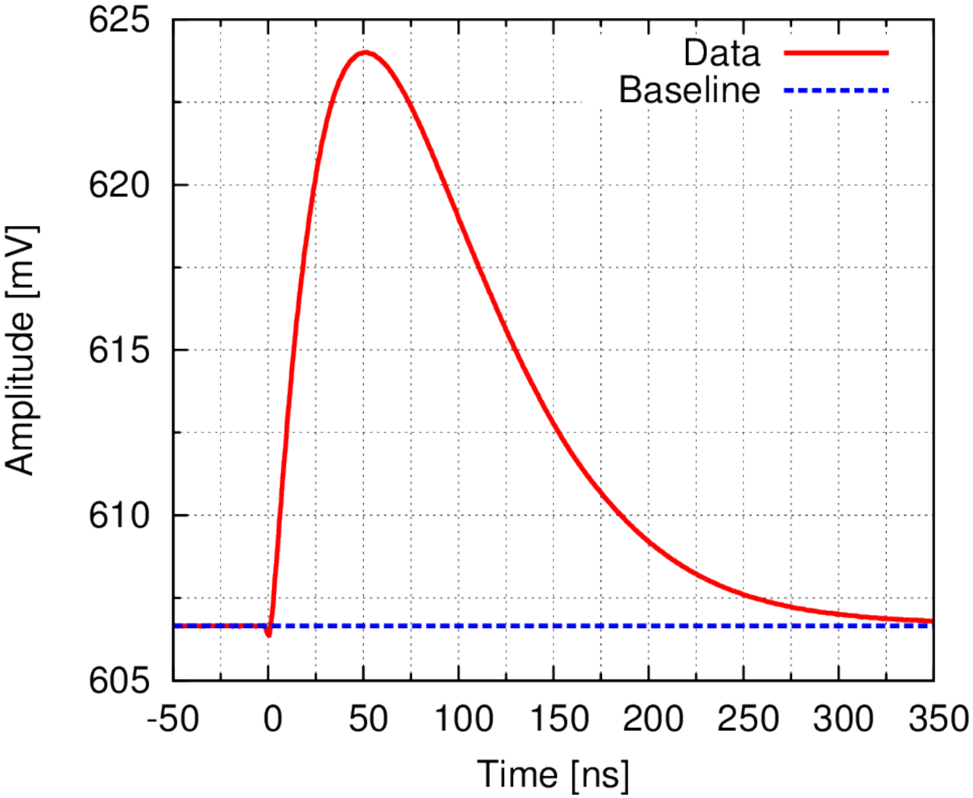
Design submitted in February 2013

Measurements setup

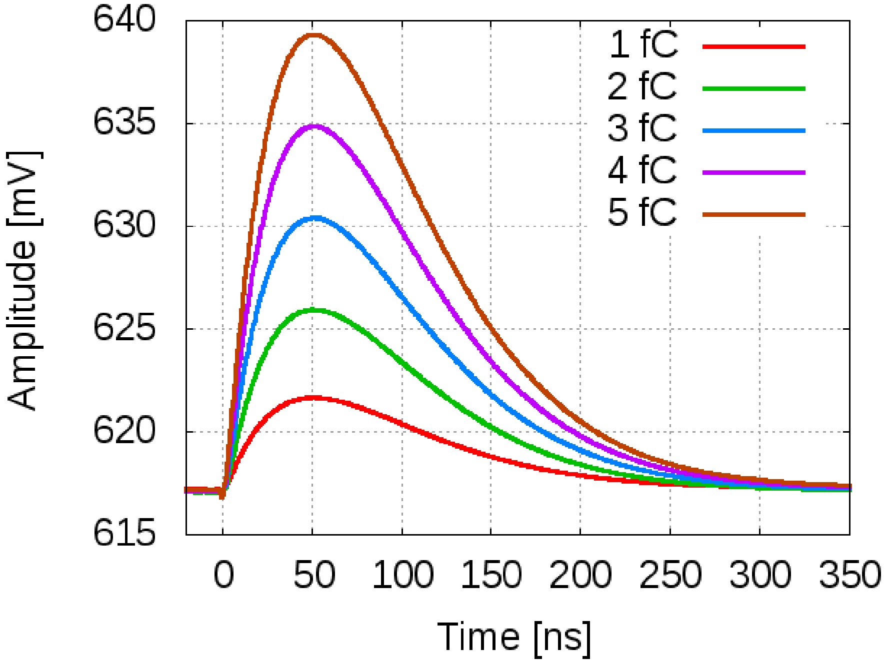


Analog Front-End measurements
Pulse response in high gain mode

Example pulse response
C_{det}=10 pF, Q_{in}=4fC



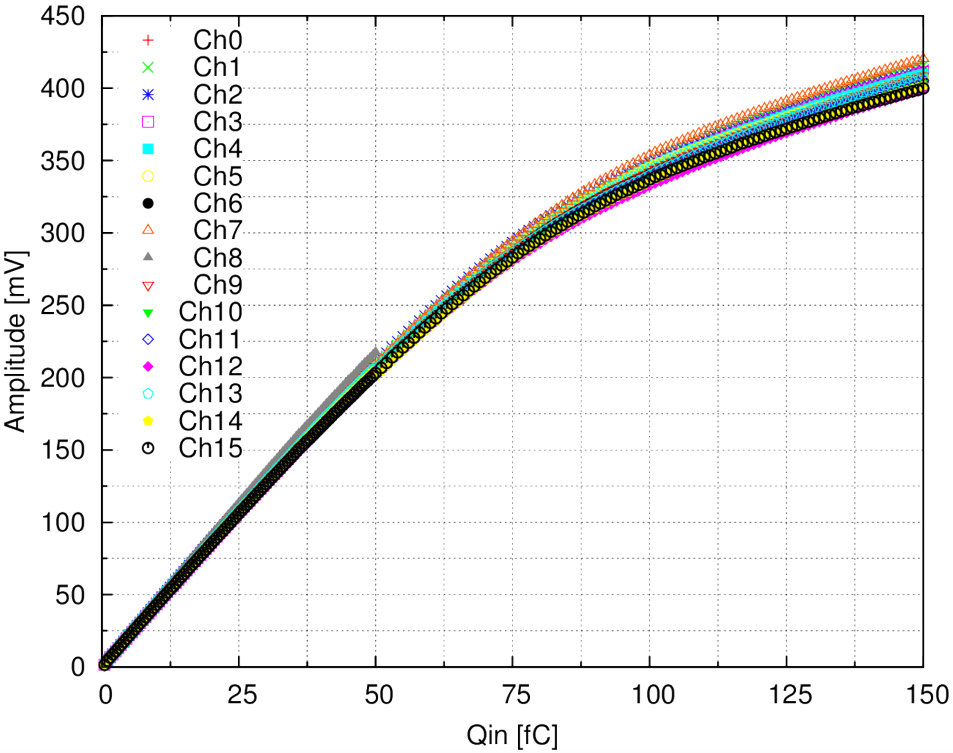
Pulses for different Q_{in}

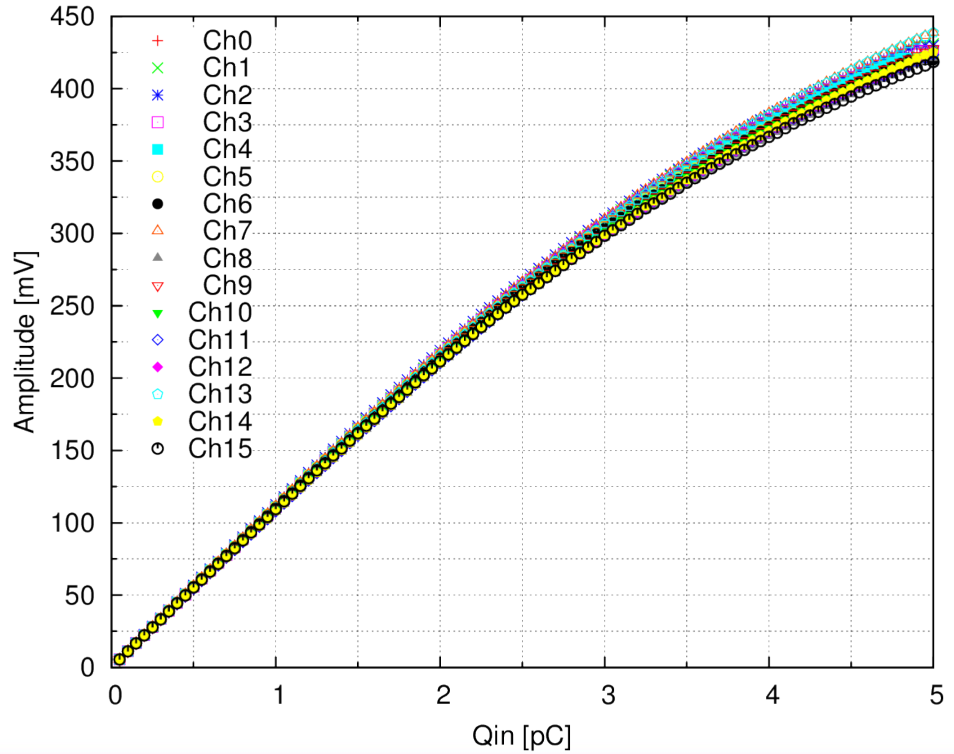


Measured shapes agree with simulations

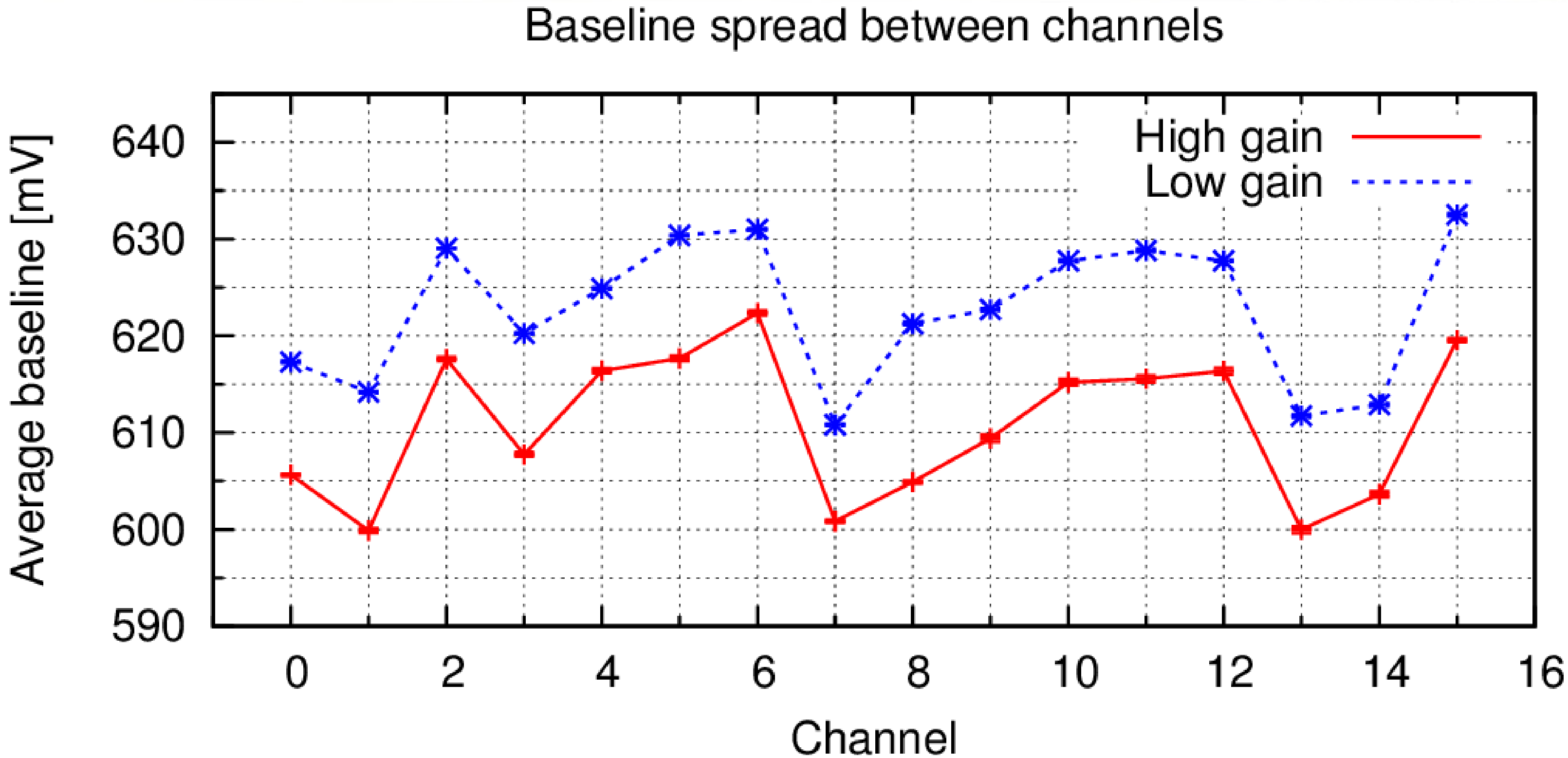
Analog Front-End measurements
Linearity

- **Measurements reasults – with agreement with simulations**
  - **High gain – 4.2 mV/fC** (4.6 mV/fC from simulations) –
    - varies between 4.03 to 4.37 mV/fC
  - **Low gain** – **105 mV/pC** (113 mV/pC from simulations)
    - varies between 101.7 to 106.4 mV/pC



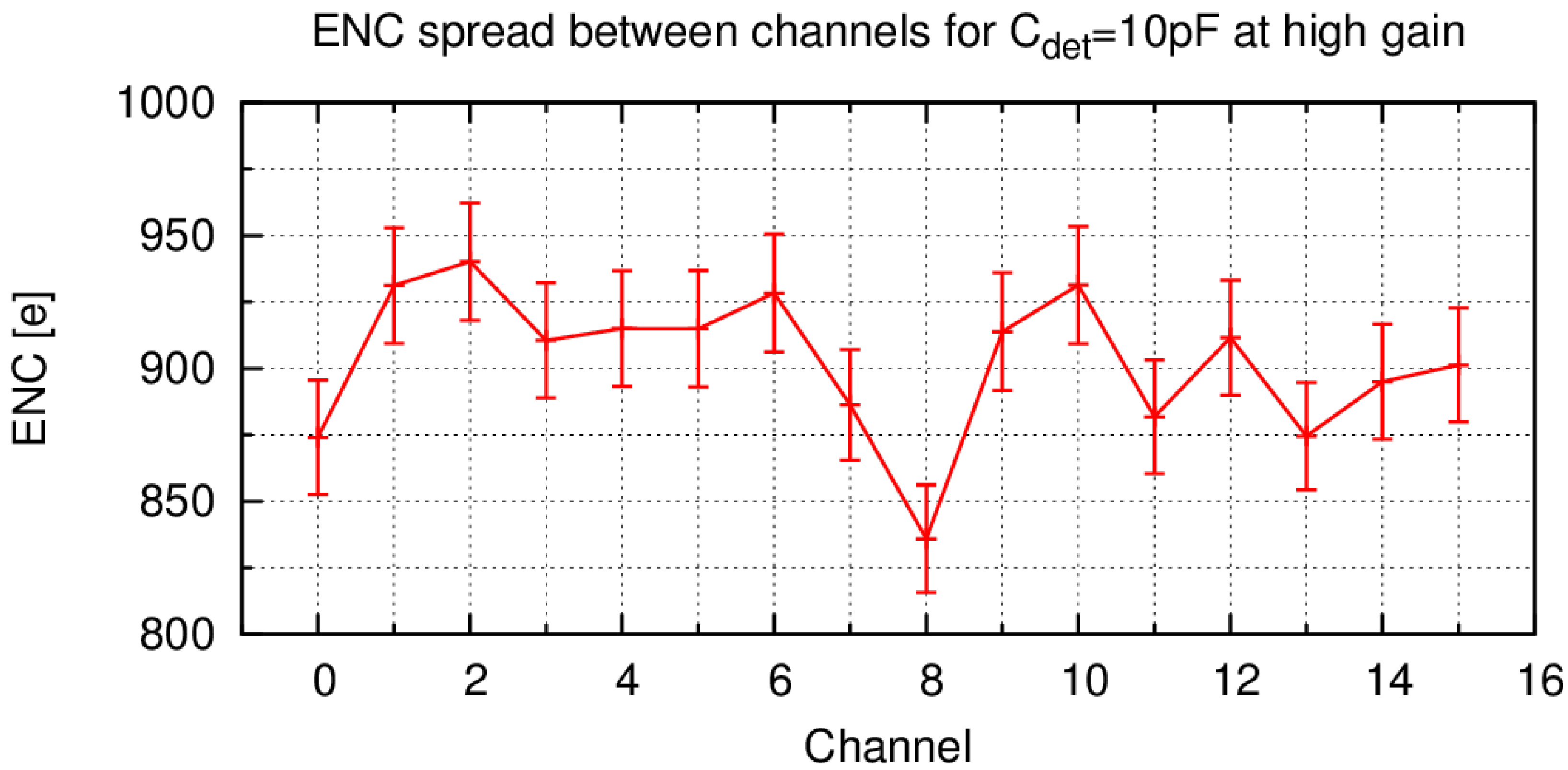


Analog Front-End measurements
Baseline spread



- 2 ASICs tested – channels 0-7 from first ASIC and 8-15 from the second
- Baseline spread is below 25 mV for both gains - in agreement with shaper amplifier offset simulations
- Baseline spread in high gain – 600 mV to 622 mV
- Baseline spread in low gain – 610 mV to 633 mV

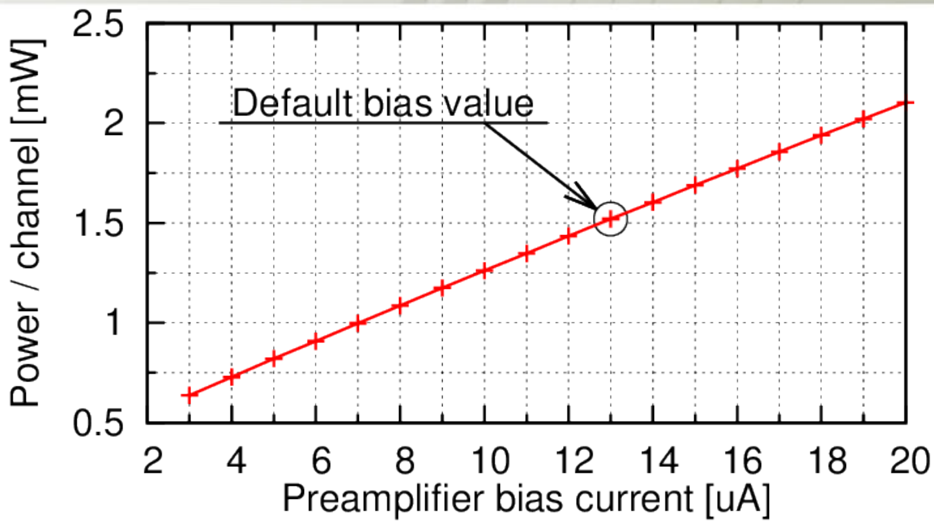
Analog Front-End measurements Noise performance

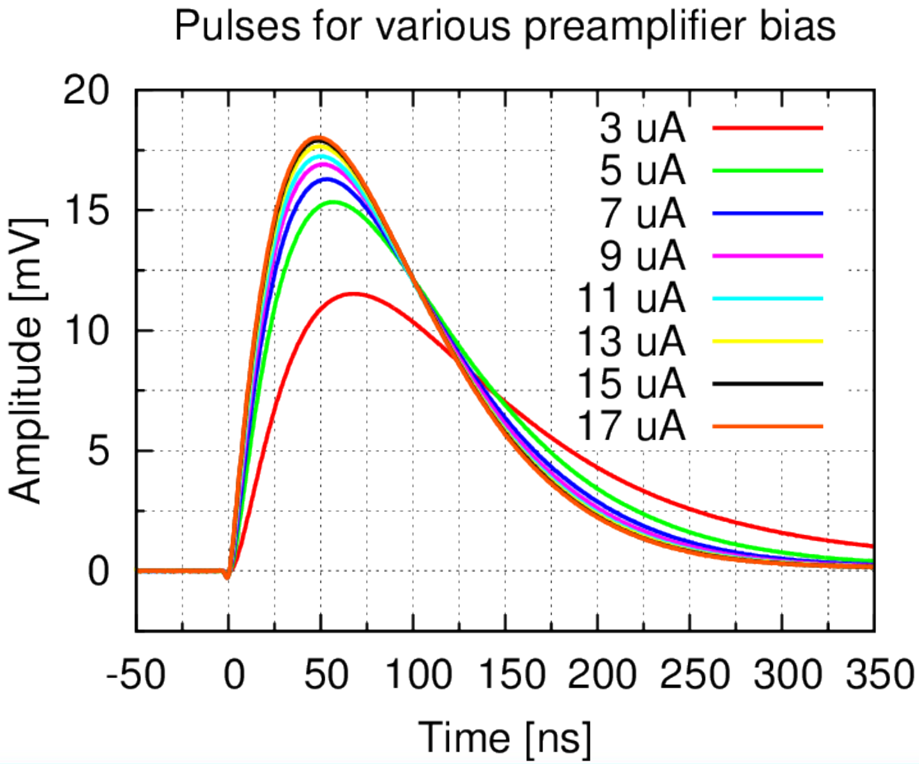


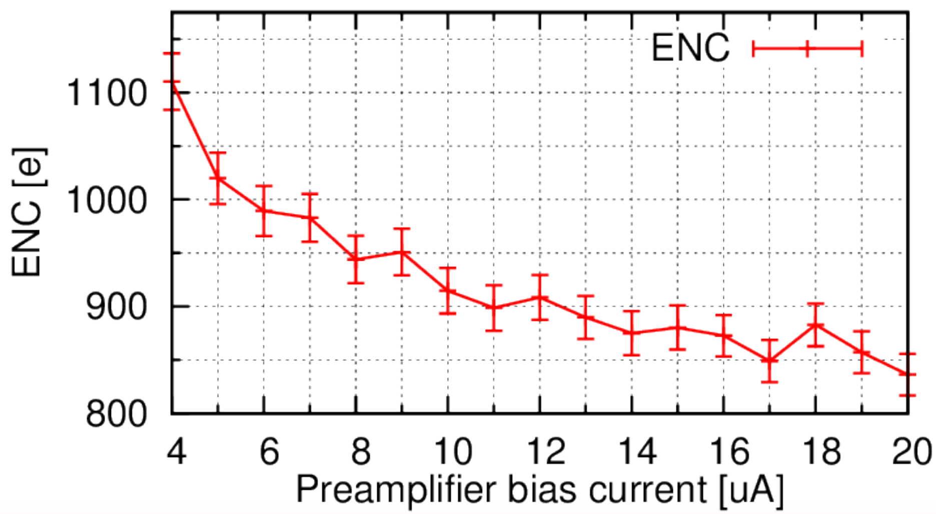
- Noise is uniform between the channels
- **ENC** (Equivalent Noise Charge) is **below 950** electrons giving **SNR** (Signal to Noise Ratio) in high gain mode **above 25** for **1 MIP** input charge

Analog Front-End measurements Power consumption vs performance: Preamplifier bias current in high gain

- Power consumption at typical biasing 1.5 mW / channel
- Power consumption may be decreased without significant decrease of performance

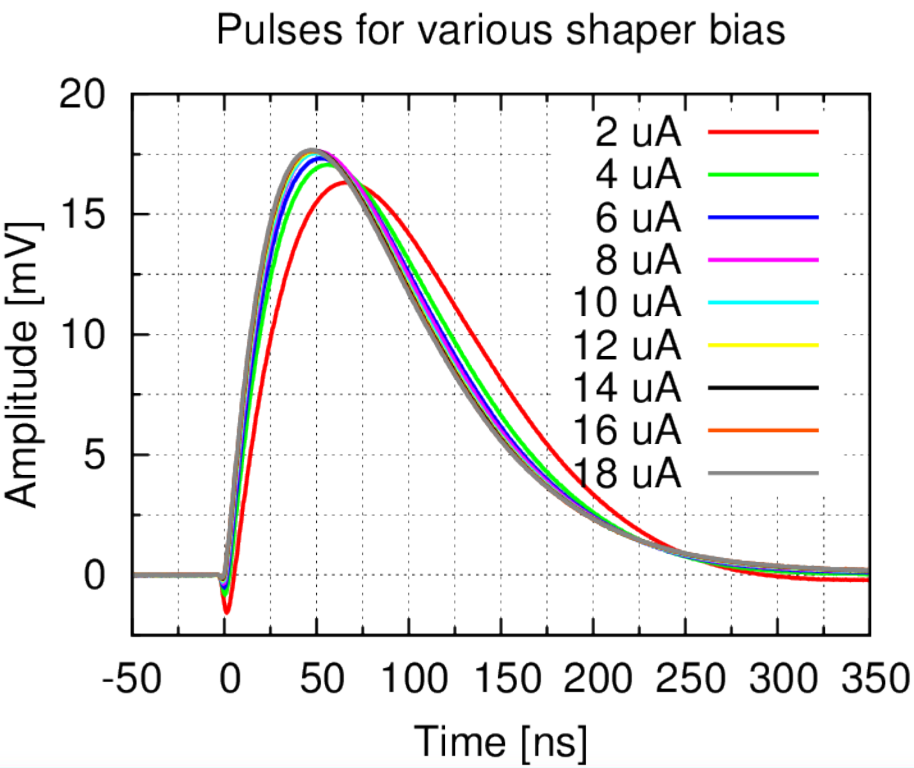


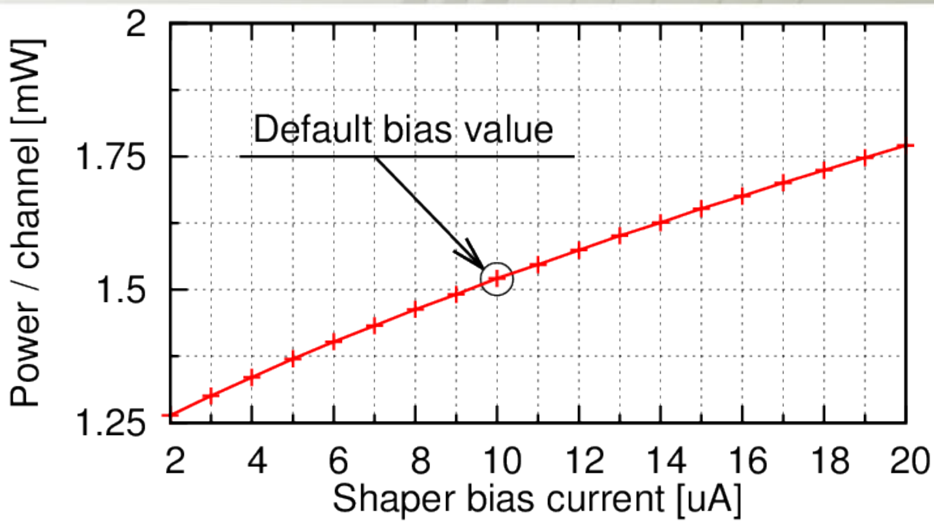


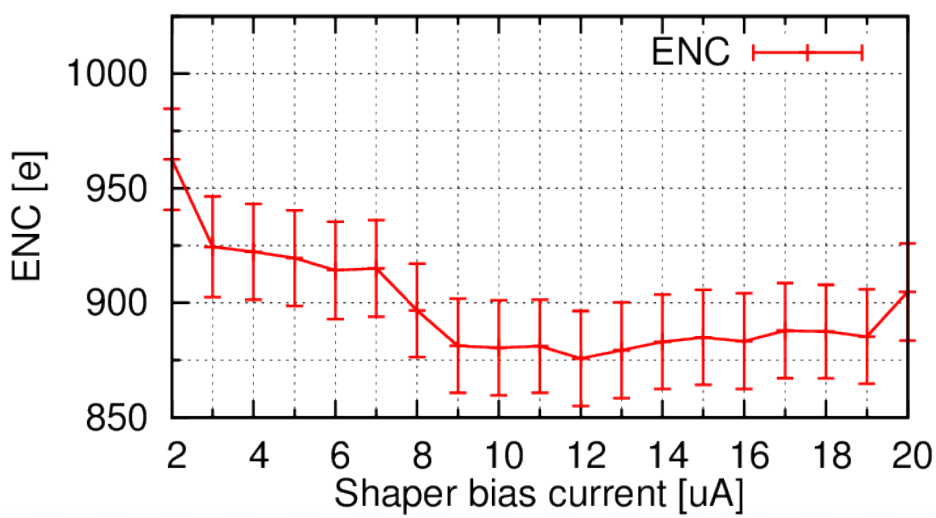


Analog Front-End measurements Power consumption vs performance: Shaper bias current in high gain

- Power consumption at typical biasing 1.5 mW / channel
- Power consumption may be decreased without significant decrease of performance







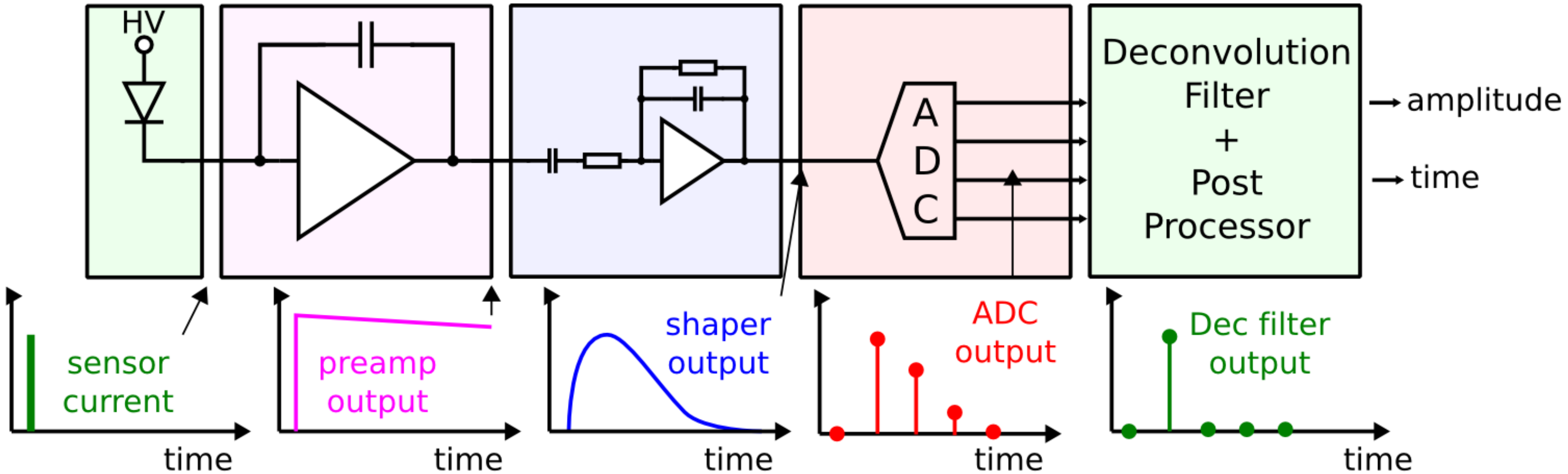
Analog Front-End measurements Summary

- Measurements results agree with simulations and specifications
  - Pulse shape and peaking time (50ns) as excepted
  - Gains in both modes differs within 10% from simulated
  - Baseline spread below 25 mV
  - Noise ENC at 10 pF below 1000 e-
  - Crosstalk measuremets:
    - High gain – 0.64%
    - Low gain – 0.80%
  - Power consumtion ~1.5 mW/channel – can be reduced by factor of ~2 by lowering bias currents
  - All parameters uniform between channels (2 ASICs measured)

- Detector capacitance measurements needs to be completed...

LumiCal readout electronics diagram – Deconvolution theory

- In the FCAL test-beams performed last years (with asynchronous trigger) deconvolution procedure was used to reconstruct the pulse amplitude and the time of its occurence



- Pulse at output of shaper v(t) is convolution of input signal (current from sensor – s(t)) and impulse response of readout chain h(t):

$$v(t)=\int_{-\infty}^{+\infty} h(t-x)\,s(x)\,dx$$

- Using data from continuously running ADC and taking advantage of known pulse shape one can perform invert procedure – **deconvolution** – to get information about event time and amplitude

Deconvolution for CR-RC shaping - Theory

$$d_i = s_i + w_1 s_{i-1} + w_2 s_{i-2}$$

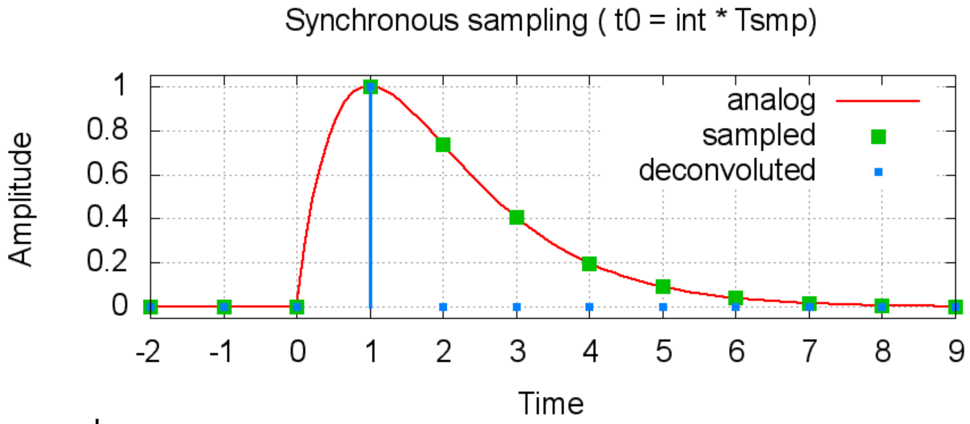
CR-RC, $T_{smp} = T_{peak} = 1$, amp =1

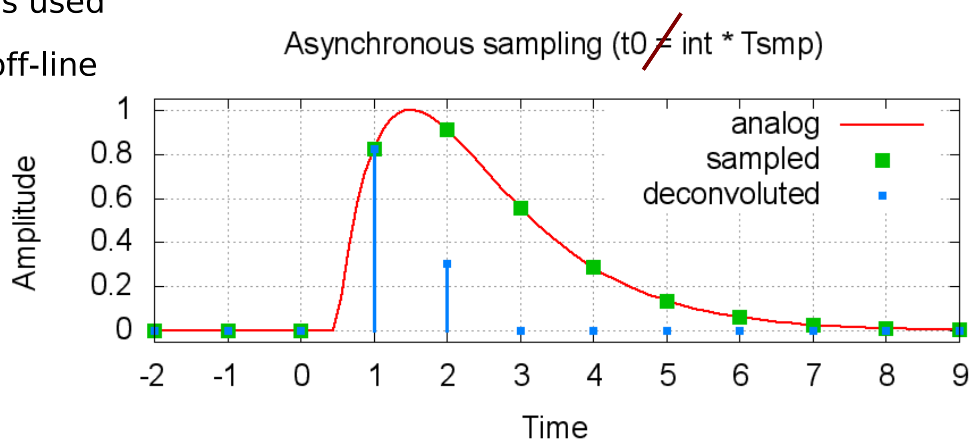
- Only two multiplications and three additions (very fast and light !)
- Deconvolution produces non-zero data only when one or two first samples are on baseline, and second/third is on pulse
- **Initial time** of pulse is found from ratio of those samples
- **Amplitude** is found from sum of those samples, multiplied by time dependent correction factor

} Look Up Tables used

Can be done off-line

- Deconvolution reduces (infinite number) of CR-RC pulse samples to 1 or 2 non zero samples !

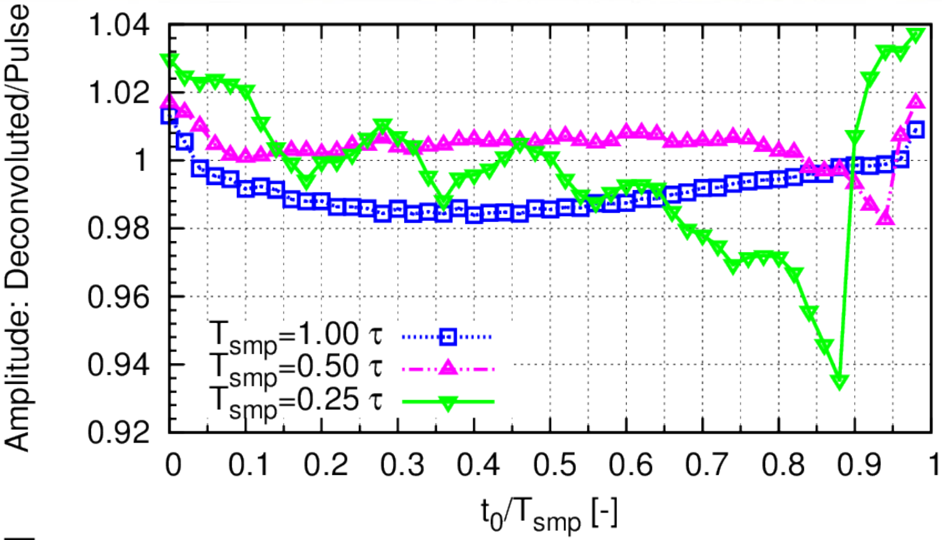


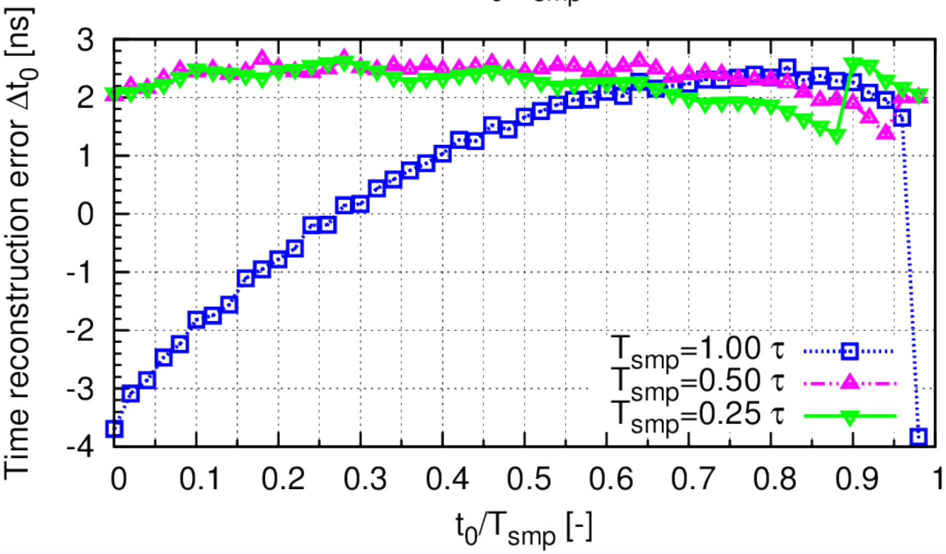


Deconvolution for new Front-End prototype Averaged pulses, ideal deconvolution weights

- Real pulse (1 MIP) deconvoluted for various phase shift t0 between the Front-End pulse and ADC sampling
- Deconvolution done for different sampling periods (12.5, 25 and 50 ns are presented)
- **Amplitude reconstruction** (top plot) – deconvoluted to real pulse amplitude ratio
  - Error is below 2% except shortest sampling period
- **Time reconstruction** (bottom plot) – difference between reconstructed and real pulse peak position
  - Constant offset of around 2 ns except longest sampling period

- **S/N after deconvolution still to be measured...**





Summary and Future Plans

- Development of new, low power, front-end electronics in CMOS 130 nm for LumiCal detector readout at linear collider is proceeding well
  - Low power 10-bit SAR ADC has been already positively verified and presented at TWEPP2013, 2nd prototype of 8 channel ADC is fabricated and waiting for tests
  - 1st prototype of 8 channel analog front-end, shown here, is working well, some quantitive tests (e.g. Cdet dependence) still need to be done...
  - Works on deconvolution implementation for new read-out system ongoing
- We hope to integrate and submitt in 2015 (in one or two ASICs) the whole front-end containing preamp+shaper+ADC in each channel, and all other functionalities (DACs, I2C, PLL, DLL, SLVS) needed in complex SoC type chip

Thank you for attention