

AIDA

Advanced European Infrastructures for Detectors at Accelerators

Presentation

Readout electronics for LumiCal detector - present status and new development

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27 May 2013



The research leading to these results has received funding from the European Commission under the FP7 Research Infrastructures project AIDA, grant agreement no. 262025.

This work is part of AIDA Work Package 9: **Advanced infrastructures for detector R&D.**

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AGH UNIVERSITY OF SCIENCE
AND TECHNOLOGY



Readout electronics for LumiCal detector

Present status and new developments

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On behalf of the FCAL Collaboration

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AGH University of Science and Technology

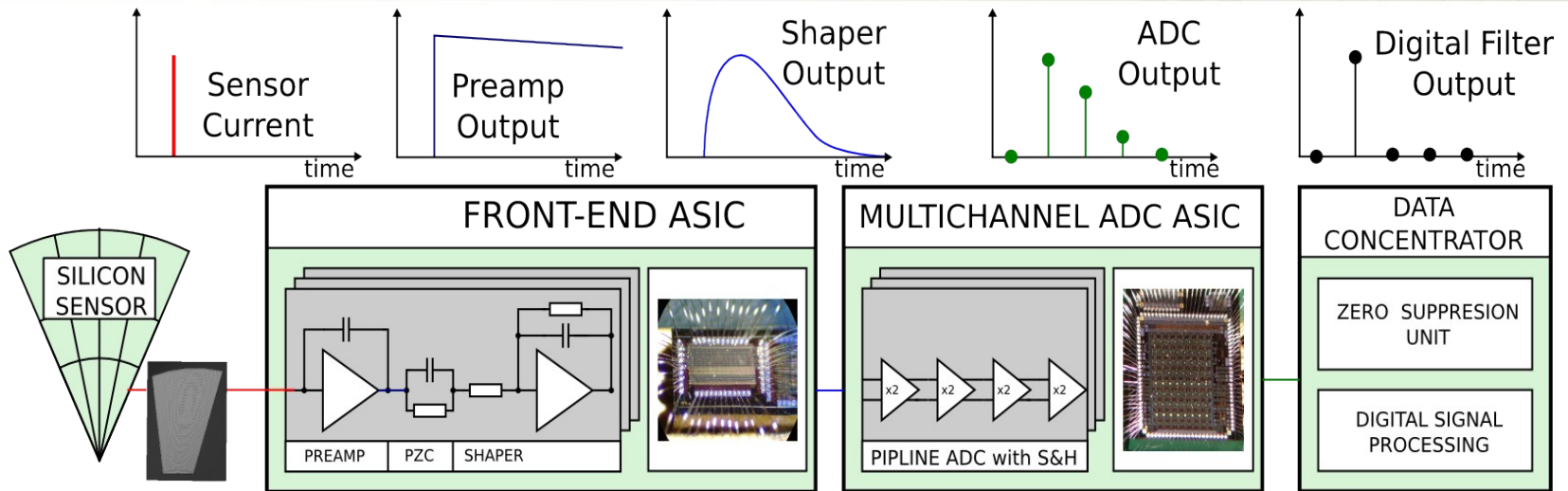
ECFA Linear Collider Workshop 2013 27 – 31 May 2013, DESY in Hamburg, Germany

- **Present LumiCal Readout**
- **ASIC developments in IBM CMOS 130nm:**
 - Front-end electronics
 - 10b SAR ADC
 - PLL, Single Ended-to-Differential converter
- **Preliminary measurements of prototypes**

Present LumiCal Readout

LumiCal detector readout chain

Status and plans



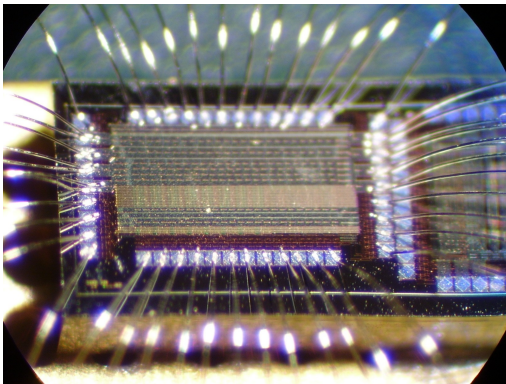
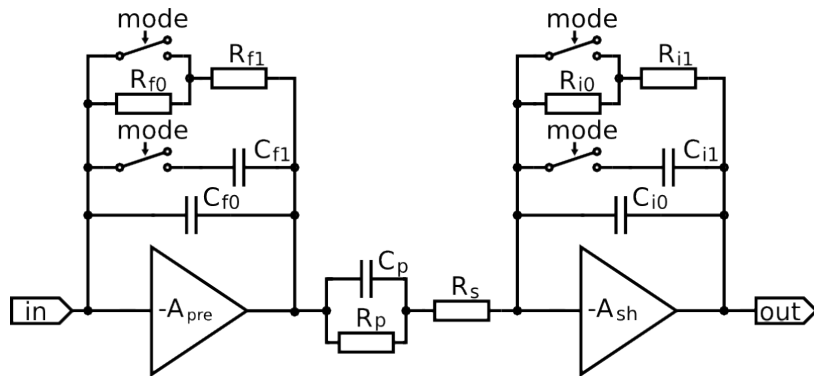
Existing LumiCal detector readout comprises:

- 8 channel front-end ASIC with preamp & CR-RC shaper $T_{peak} \sim 60\text{ns}$, $\sim 9\text{mW}$ (**AMS 0.35 μm**)
- 8 channel pipeline ADC ASIC, $T_{smp} \leq 25\text{MS/s}$, $\sim 1.2\text{mW/MHz}$ (**AMS 0.35 μm**)
- FPGA based data concentrator and further readout

New developments for LumiCal detector readout:

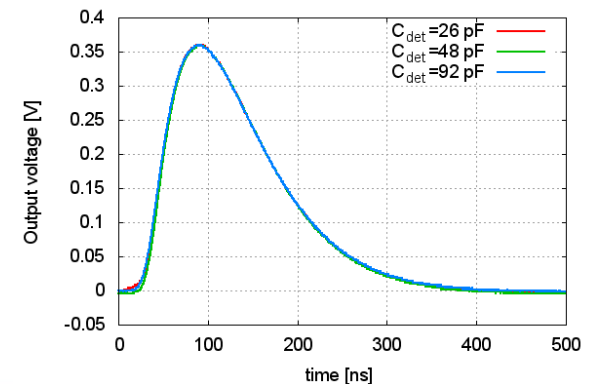
- Prototype front-end ASIC in **IBM 130 nm** under development...
- Prototype SAR ADC ASIC in **IBM 130 nm** under development...

Present LumiCal Readout Front-end Electronics for LumiCal detector in AMS 0.35 μ m



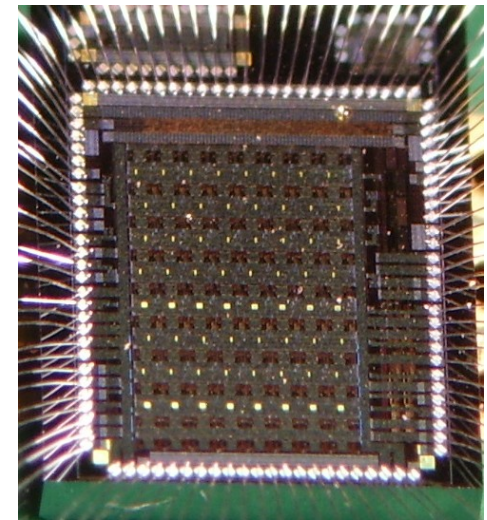
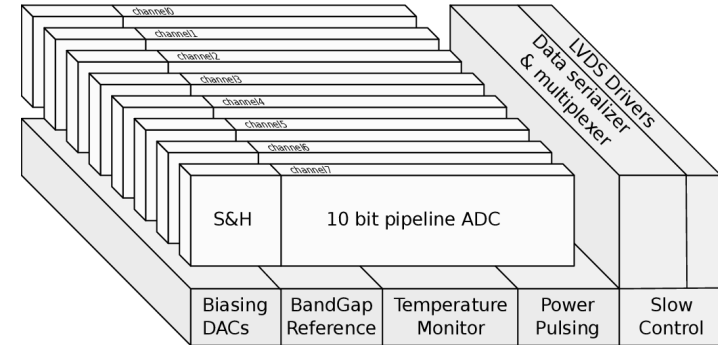
Existing prototypes:

- 8 channels in AMS0.35 μ m
- $C_{det} \approx 0 \div 100$ pF (in new specs: $C_{det} < 30$ pF)
- 1st order shaper ($T_{peak} \approx 60$ ns)
- Variable gain:
 - calibration mode - MIP sensitivity (~ 4 fC)
 - physics mode - input charge up to 10 pC
- Prototypes fabricated and tested
 - power consumption 8.9 mW/channel
 - event rate up to 3 MHz
 - Crosstalk $< 1\%$



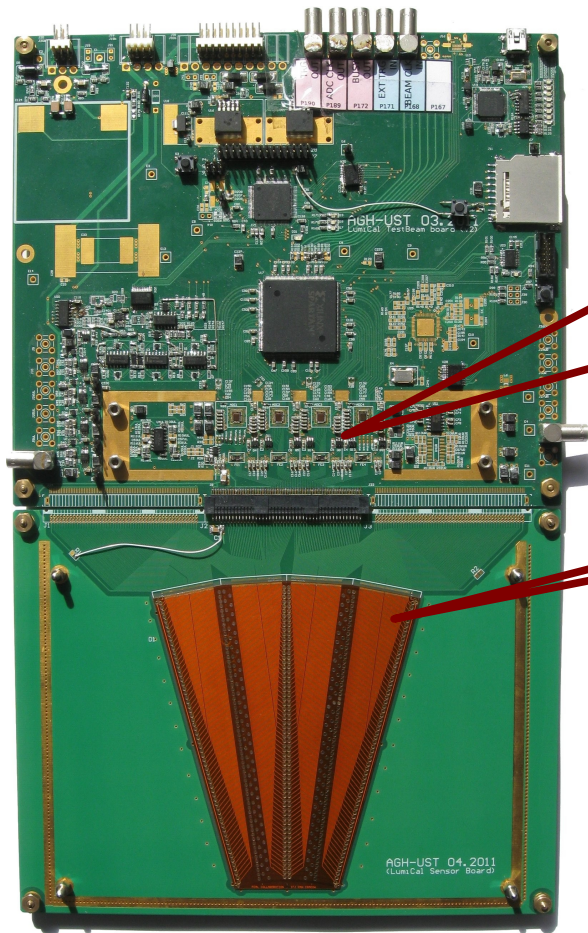
Present LumiCal Readout Multichannel digitizer in AMS 0.35um architecture

- Specs & implementation issues:
 - 8 channels of 10-bit pipeline ADC
 - Technology AMS 0.35um
 - Fully differential ADC
 - Layout with 200um ADC pitch
 - Multimode digital multiplexer/serializer:
 - Serial mode ($\sim 250\text{MHz}$): one data link per all channels (max f_{smp} ~ 3 MSps)
 - Parallel mode ($\sim 250\text{MHz}$): one data link per channel (max f_{smp} ~ 25 MSps)
 - Test mode: single channel output (max f_{smp} ~ 50 MSps)
 - High speed LVDS interface ($\sim 1\text{GHz}$)
 - Bootstrapped S/H switches
 - Power pulsing
 - Low power DACs for internal settings
 - BandGap reference source
 - Temperature sensor

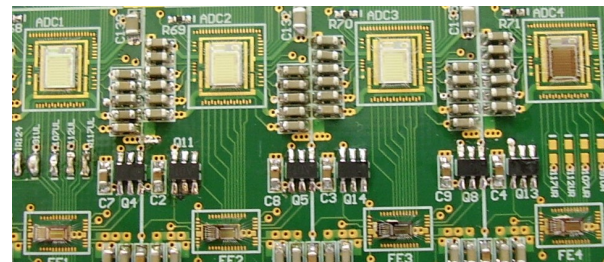


2.6mm x 3.2mm

Present LumiCal Readout LumiCal detector readout module (ASICs in AMS 0.35um)



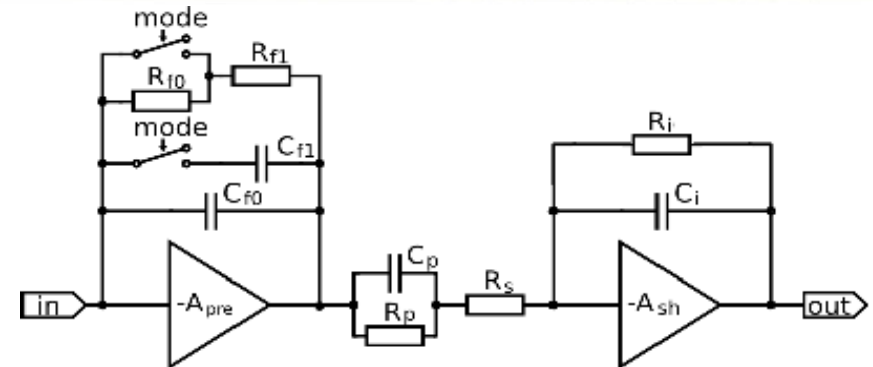
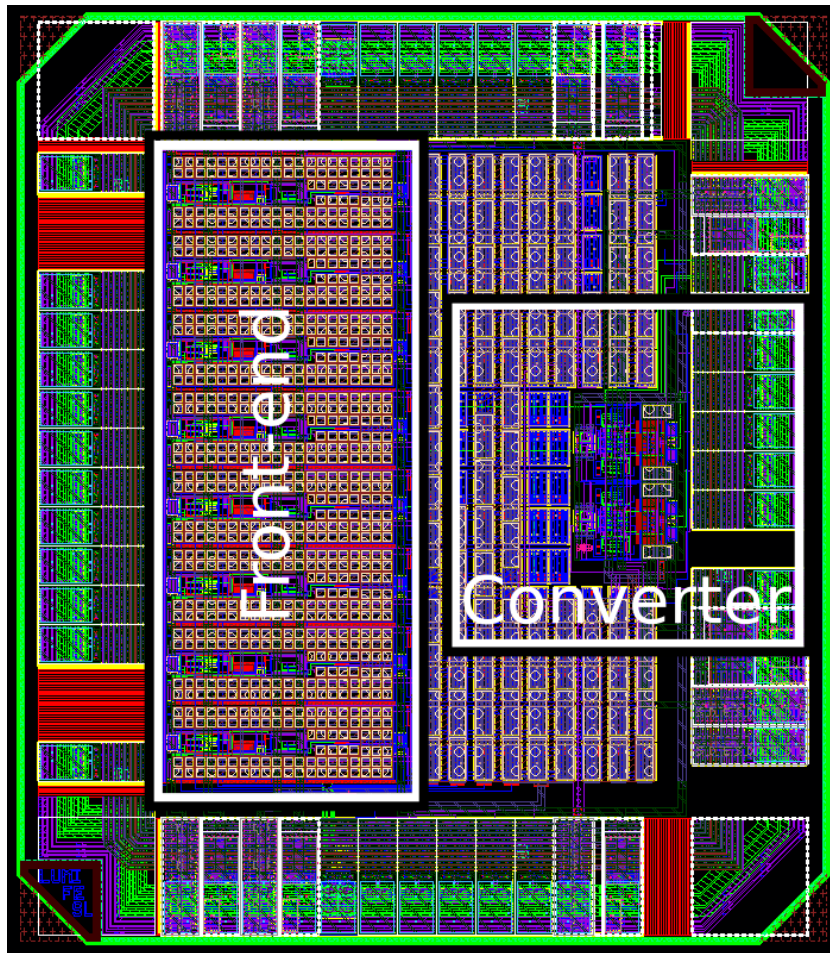
4 pairs of Front-end + ADC



Sensor (IFJ PAN)

- ❑ LumiCal detector module with 32 fully equipped channels (Front-end +ADC ASICs) plus FPGA data concentrator is regularly used during FCAL Collaboration test-beams

Developments in IBM CMOS 130nm Front-end: Preamplifier & Shaper



Design specs:

- 8 channels
- $C_{det} \approx 5 \div 50 \text{ pF}$
- 1st order shaper ($T_{peak} \approx 50 \text{ ns}$)
- Variable gain:
 - calibration mode - MIP sensitivity
 - physics mode - input charge up to $\sim 6 \text{ pC}$
- Power pulsing implemented
- Simulated power consumption $\sim 1.5 \text{ mW/channel}$

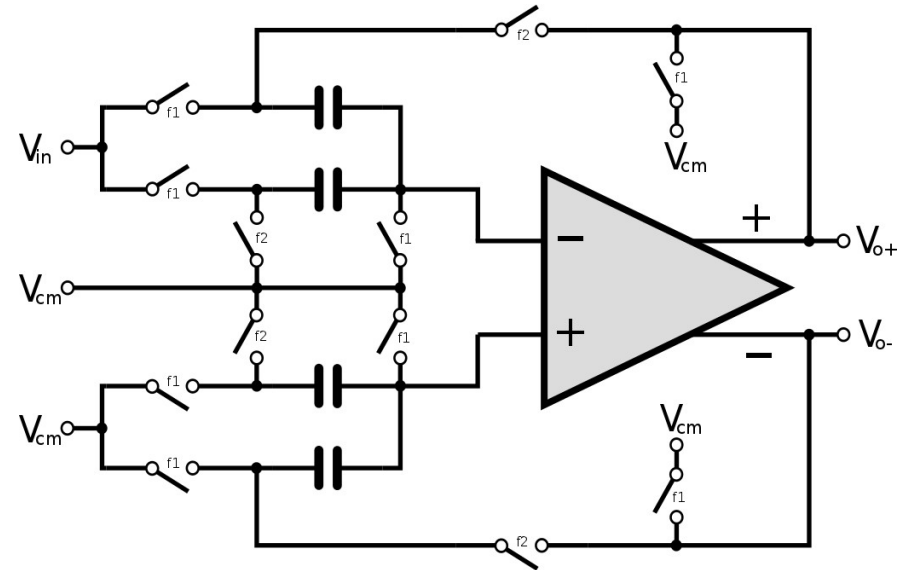
Design submitted in February 2013

Developments in IBM CMOS 130nm

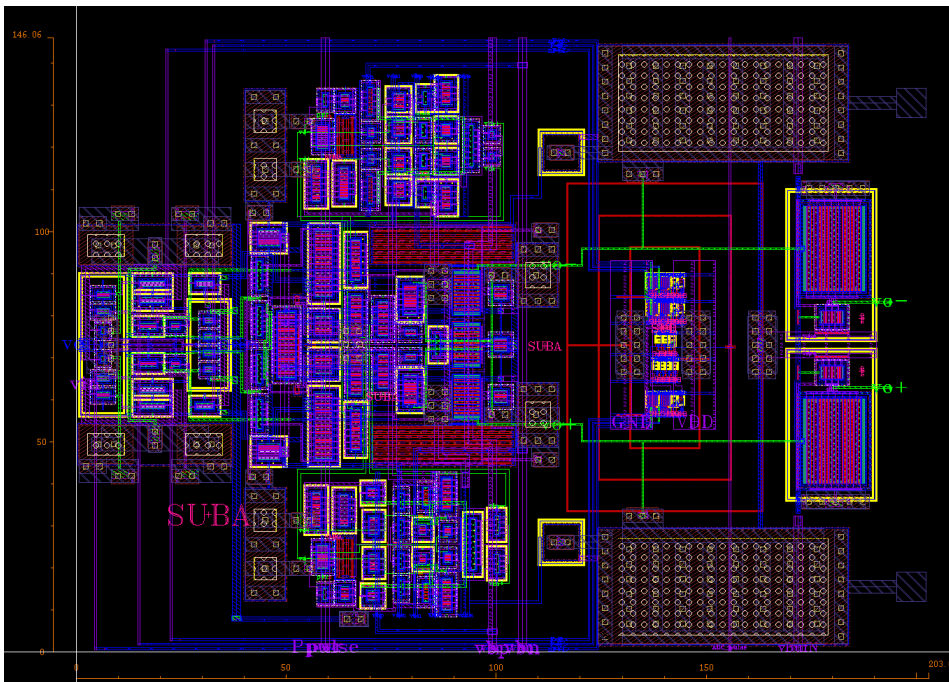
Single Ended-to-Differential converter

Single Ended to Differential converter

- Dynamic input range ~ 600 mV
- Differential output range ~ 1.2 V
- Maximum frequency ~ 50 MHz

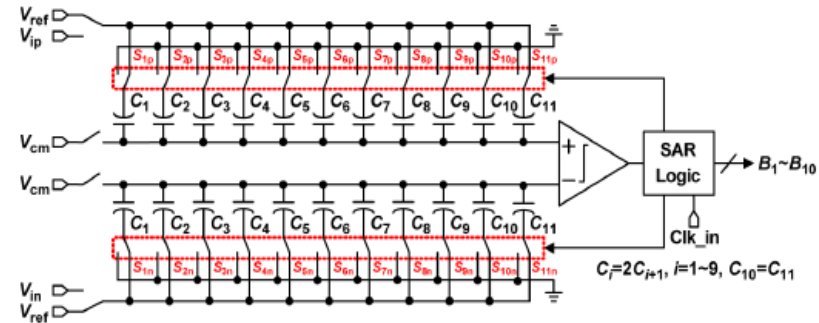


Design submitted February 2013



Developments in IBM CMOS 130nm SAR ADC: General features & design considerations

- Power and area-efficient architecture
 - the same circuitry is used N-times (for N-bit ADC) to approximate the input voltage
- Only one comparator, two DACs and SAR logic needed – fits well to modern digital CMOS
- Limited sampling rates - but with modern CMOS technology ($\sim 100\text{nm}$) up to $\sim 100\text{MSps}$ 10-bit ADCs were reported
 - next conversion cannot be started before completion of previous one
 - sampling time adds to conversion time (not like in pipeline)



- Comparator – the only analog block
- DAC network serves as sampling capacitance
- Simple digital logic
- Fully differential implementation increases the resistance to disturbances

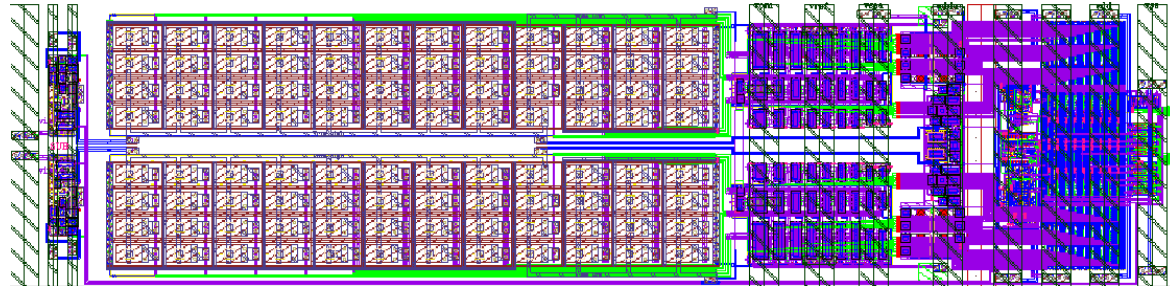
Developments in IBM CMOS 130nm

Design of 10-bit SAR ADC

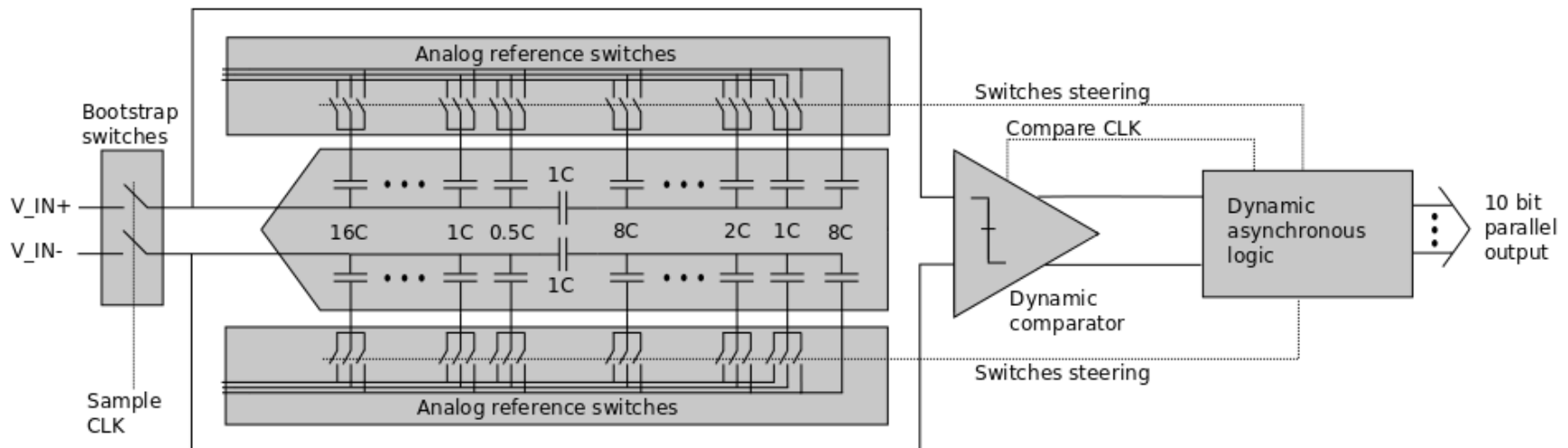
Designs of 10-bit ADC

- Architecture: SAR ADC with segmented/split DAC
- Scalable frequency (up to ~ 50 MS/s) and power consumption
- Asynchronous SAR logic – No bit-clk

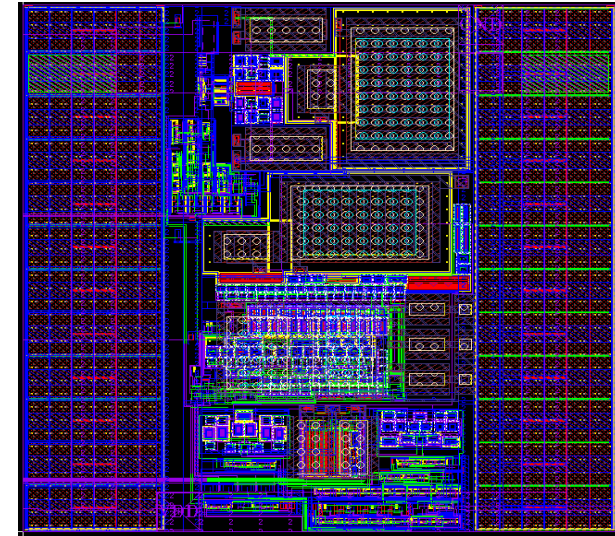
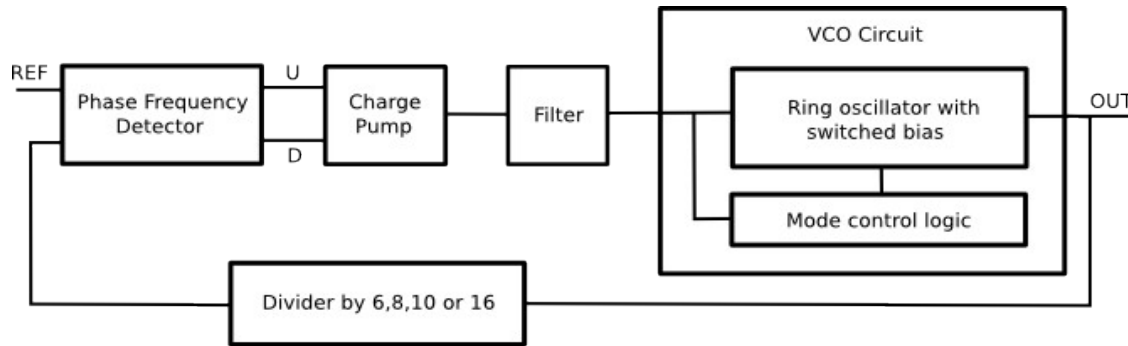
SAR channel $600\mu\text{m} \times 146\mu\text{m}$



- 1-2 mW at 40 MS/s
- $146\mu\text{m}$ pitch
- Fabricated in 2012 (2 prototypes)



Developments in IBM CMOS 130nm Design of PLL for data serialization

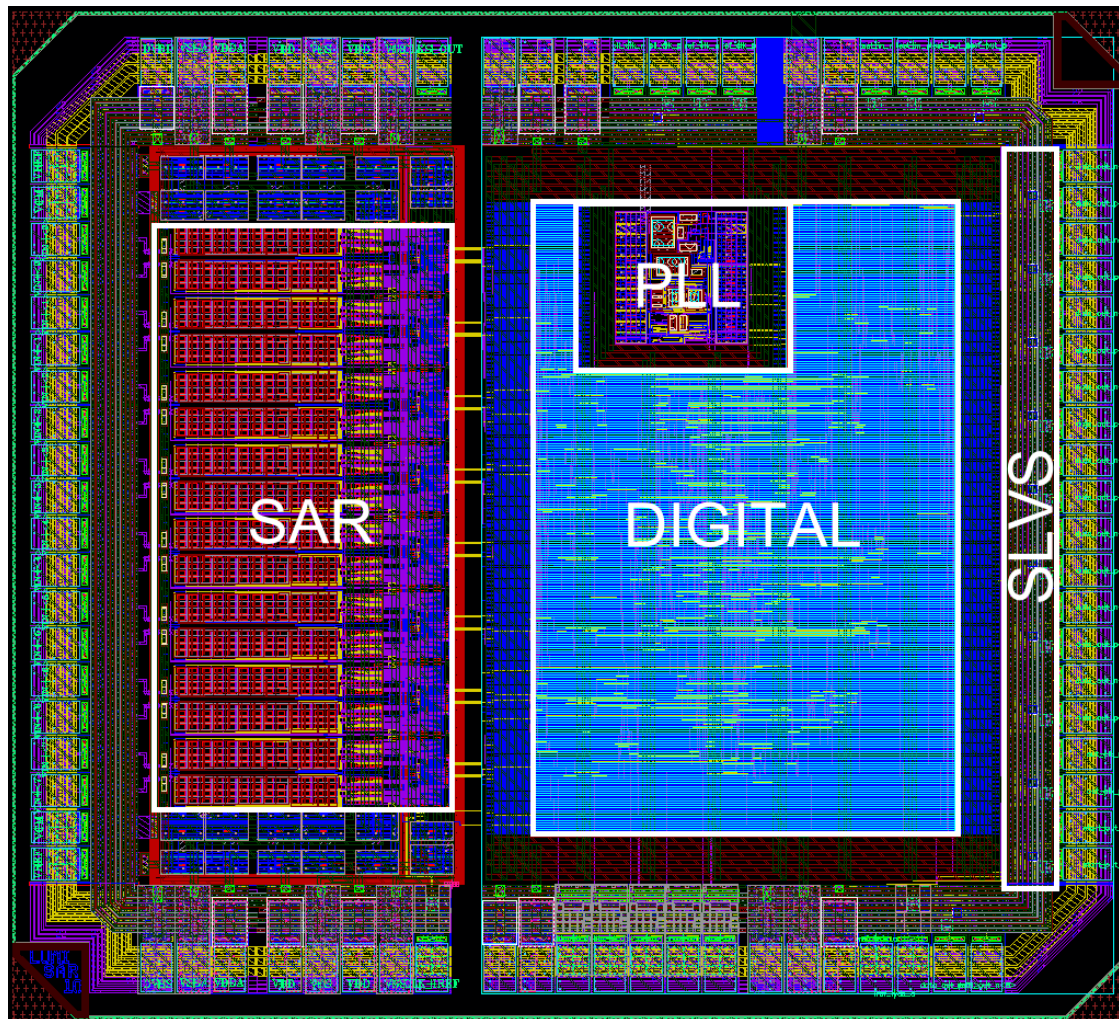


300 x 300 um

Design specs:

- Architecture: type II PLL with 2nd order filter
- Scalable frequency & power
- Automatically switched VCO freq. range
- VCO frequency range 8MHz – 3GHz,
- VCO frequency division by 6, 8, 10 or 16
- Power consumption <2mW at 3GHz
- ***Submitted and fabricated in 2012, the tests have just started...***

Developments in IBM CMOS 130nm Layout of 8 channel 10-bit SAR ADC



ASIC comprising:

- 8 channels of 10-bit SAR ADC,
- Multimode digital multiplexer / serializer
- PLL for data serialization
- High speed SLVS interface

***Design submitted
and fabricated in
2012***

2200um x 2000um

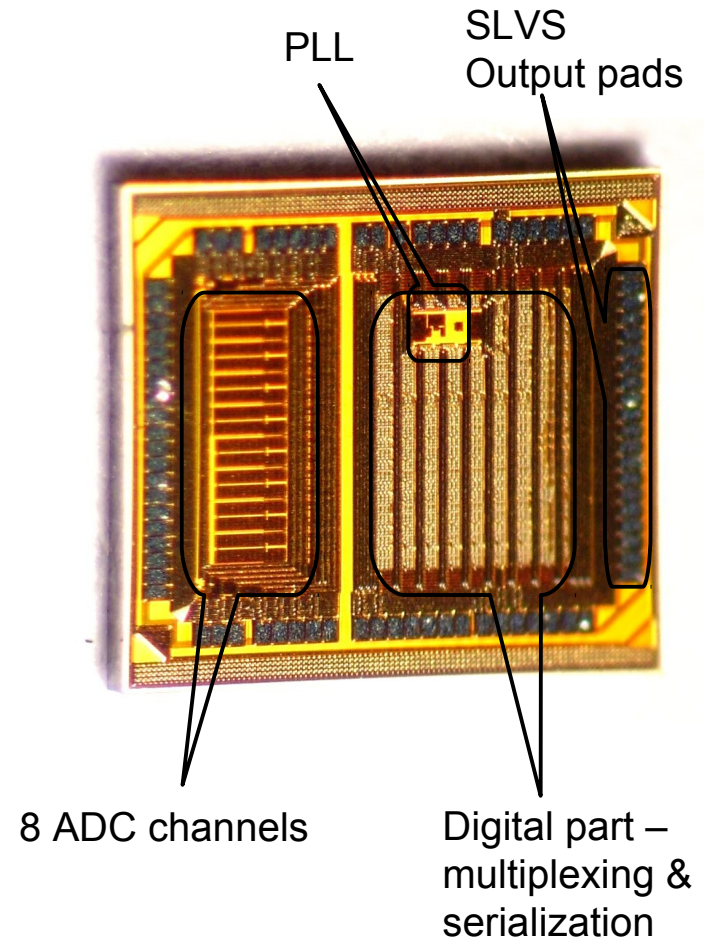
Preliminary measurements

First prototypes in IBM 130nm under tests

10-bit ADC, PLL, SLVS

Prototype ASIC contains:

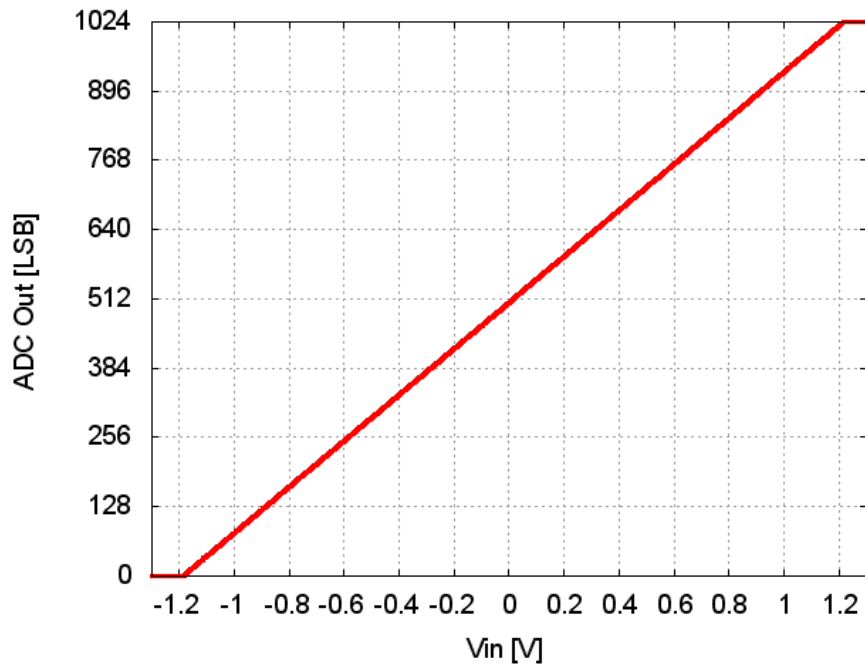
- 10-bit SAR ADC
- PLL
 - Systematic tests are just starting. PLL output clock signal was observed with scope.
- SLVS interface
 - No dedicated tests of SLVS interface were done, but looking at ADC and PLL differential outputs it was verified that SLVS driver operates at least up to 700 MHz.



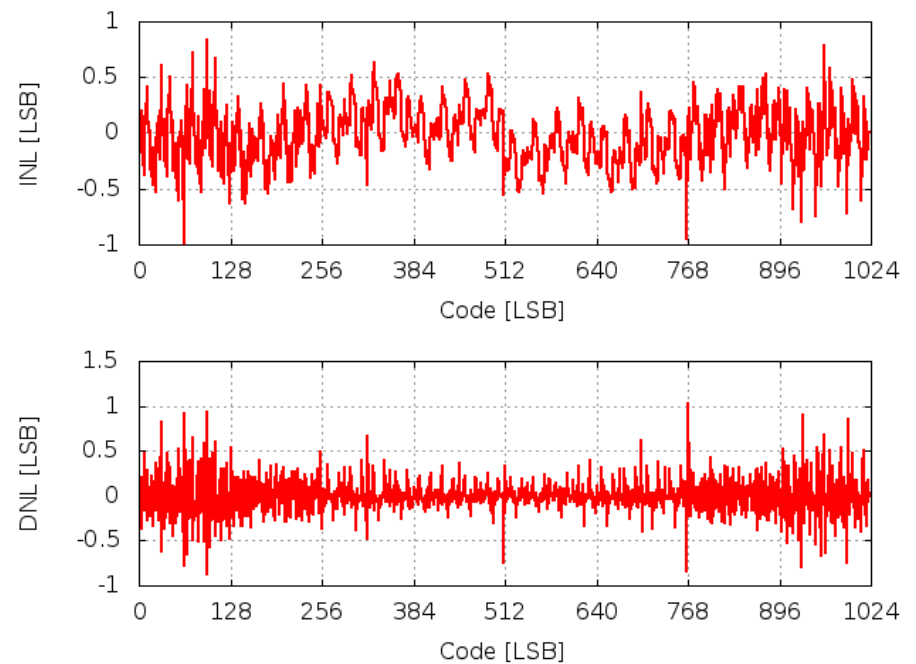
Preliminary measurements

10-bit SAR ADC - Static measurements

Transfer function



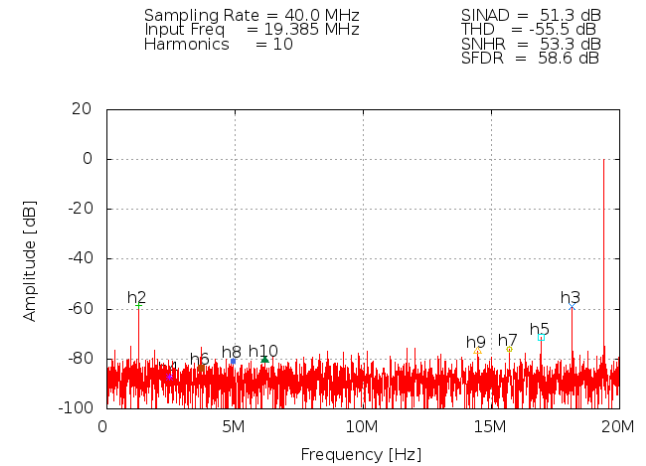
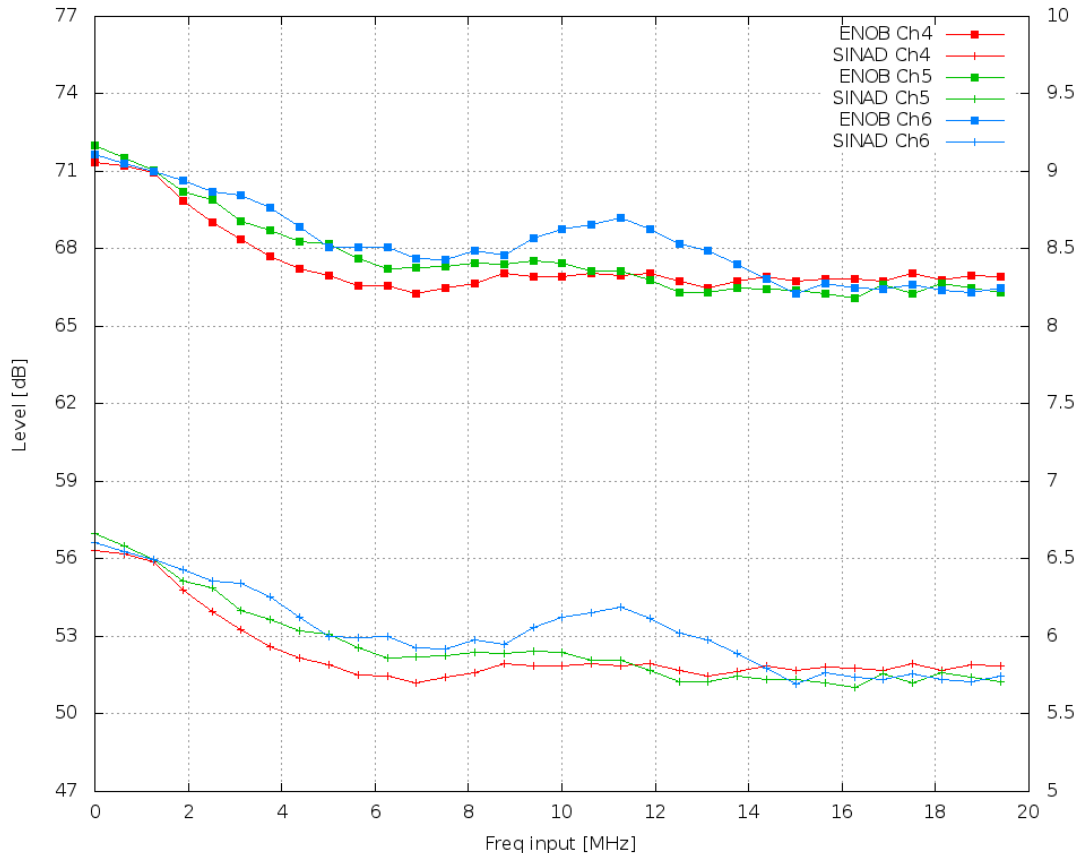
INL/DNL measurements



- ADC is alive and works in the whole input signal range
- There are some codes with worse linearity (to be investigated...)

Preliminary measurements

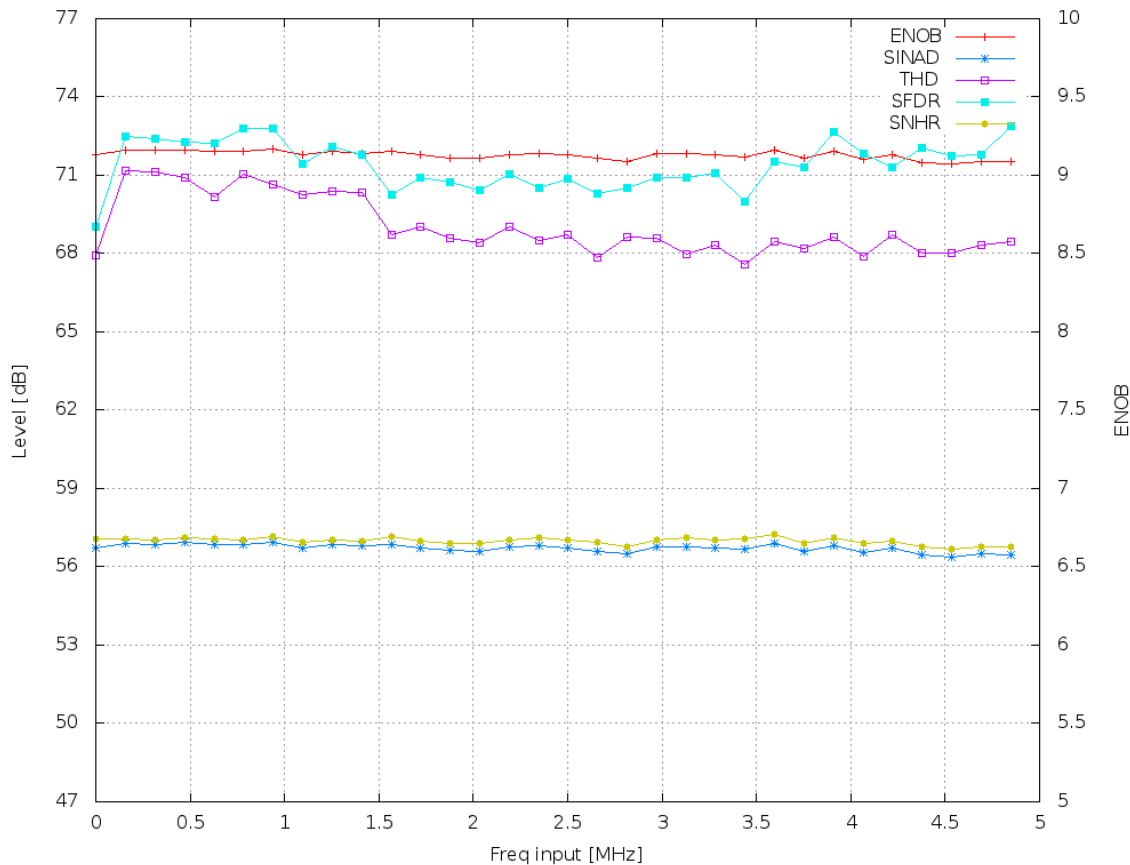
10-bit SAR ADC - Dynamic measurements – different channels



- Results for different channels (only one channel ON during measurements) are similar
- It was suspected that ENOB decrease with f_{in} is partially/mainly due to setup

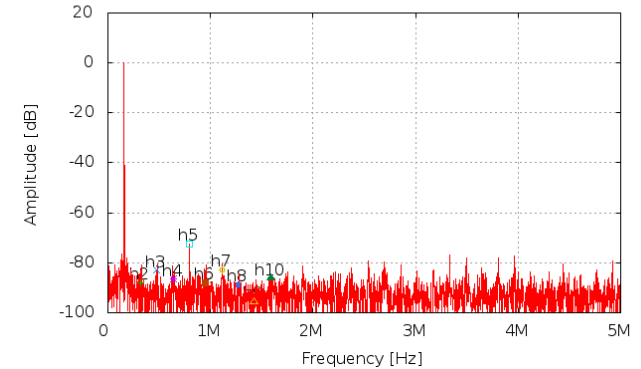
Preliminary measurements

10-bit SAR ADC - Dynamic measurements – f_{in} scan



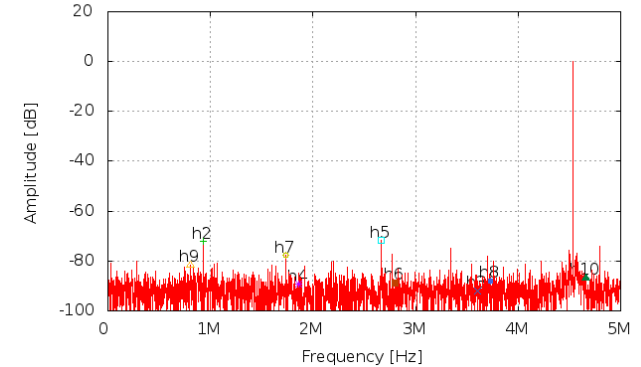
Sampling Rate = 10.0 MHz
 Input Freq = 158.691 kHz
 Harmonics = 10

SINAD = 56.9 dB
 THD = -71.2 dB
 SNHR = 57.1 dB
 SFDR = 72.5 dB



Sampling Rate = 10.0 MHz
 Input Freq = 4.534 MHz
 Harmonics = 10

SINAD = 56.4 dB
 THD = -68.0 dB
 SNHR = 56.7 dB
 SFDR = 71.7 dB

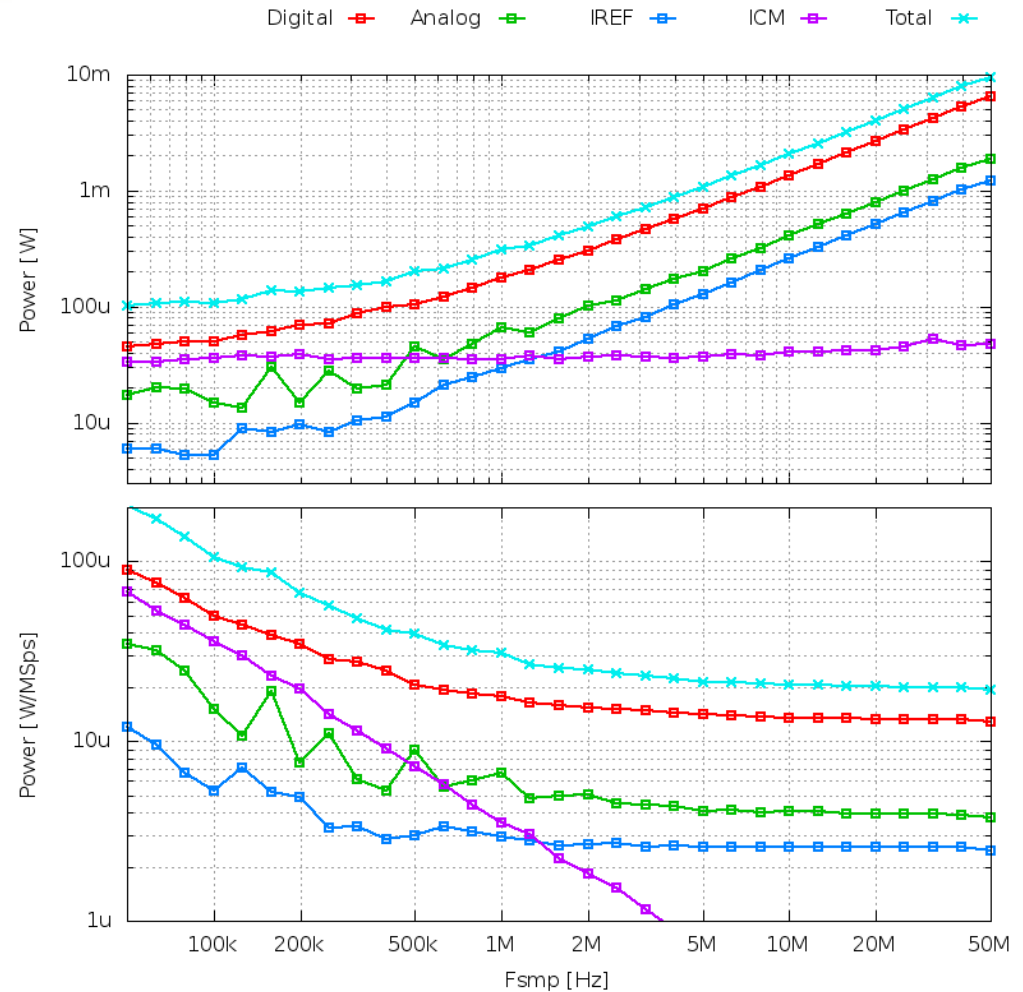


- ENOB of ≥ 9.2 was measured up to Nyquist frequency after improving test setup – more improvement needed?

Preliminary measurements

10-bit SAR ADC - Power consumption vs sampling frequency

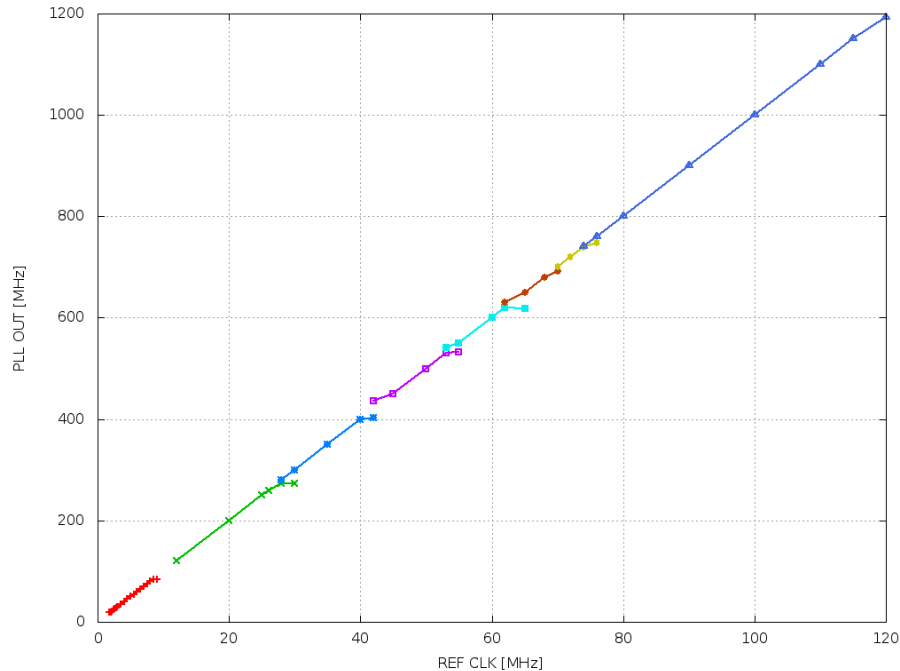
- Power measured for 8 ADC channels
- At 40MS/s power consumption is about 1 mW per channel – in agreement with simulations



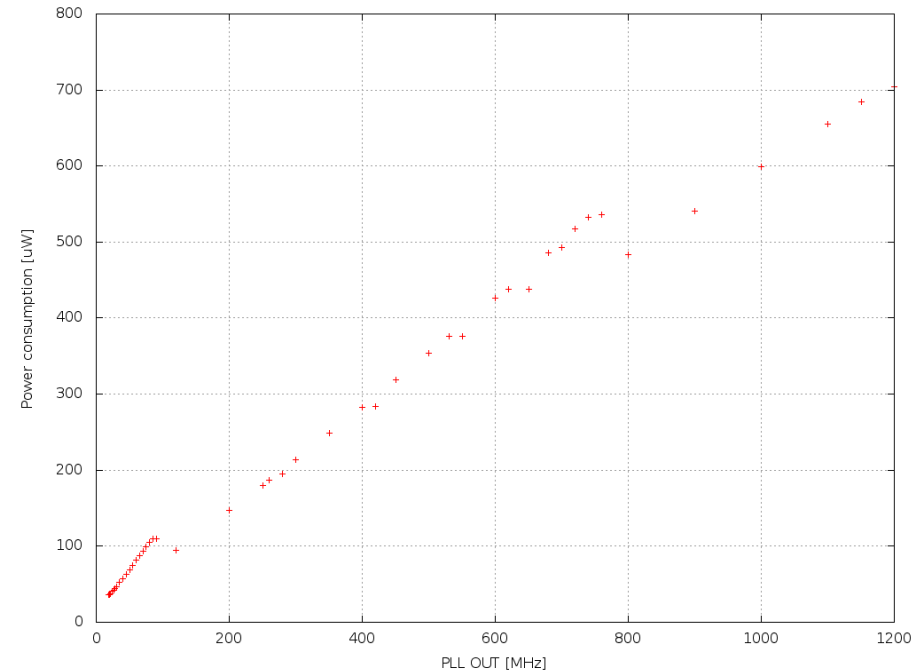
Preliminary measurements

PLL – Transfer function, power consumption

PLL transfer function – CLK out vs CLK in



Power consumption measurements



- PLL measurements have just started (~ 2 days) and are in progress...
- PLL output CLK in frequency range 15MHz-1.2GHz already observed
- There are some gaps between frequency ranges...
- Automatic mode detection looks promising
- SLVS driver works at least up to 1.2 GHz (used for PLL output)

Summary and Plans

- Presently FCAL uses in test-beams the readout modules based on developed at AGH-UST ASICs in CMOS AMS 0.35um
- Development of new ASICs for LumiCal readout in IBM 130 nm in progress:
 - First prototype of front-end electronics submitted and should be available in ~June 2013
 - First prototypes of 10-bit SAR ADC, PLL, SLVS already produced and presently under test:
 - 10-bit SAR ADC: first results show its functionality, the effective resolution slightly less than simulated - quantitative measurements in progress...
 - PLL tests just started...
 - SLVS interface works well
 - Depending on test progress and results we plan next submission at the turn of 2013/2014



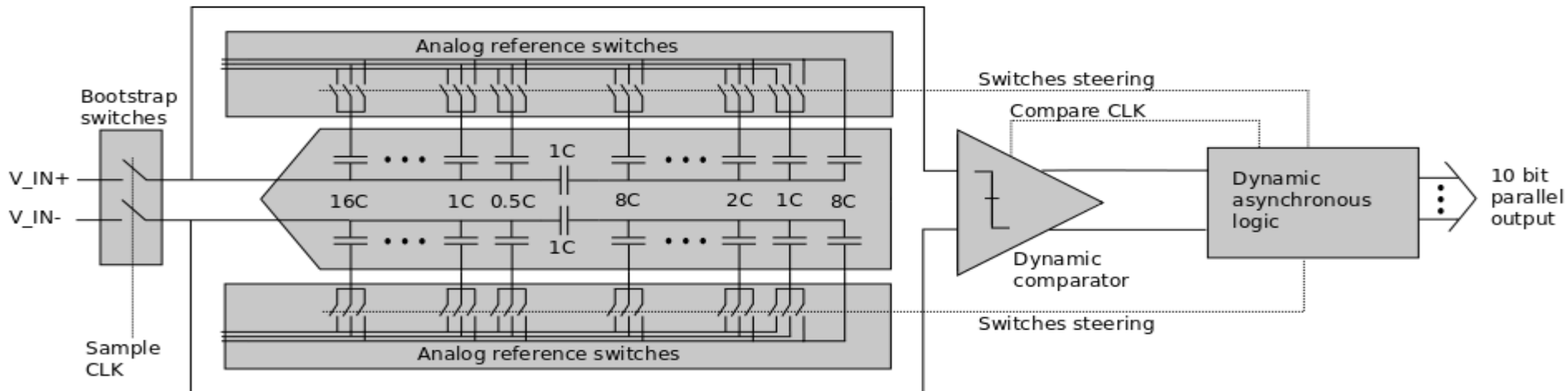
Backup slides

Backup slides

Developments in IBM CMOS 130nm

Design of SAR ADC - Implementation issues

- Asynchronous logic
 - no fast clock needed for bit cycling
 - only sampling pulse needed
 - sampling pulse (trigger) does not need to be periodic
- Dynamic comparator
 - allows to obtain zero static power consumption and so "power pulsing" is given for free
- Split DAC architecture
 - allows using higher unit capacitance for the given total DAC capacitance. It helps to bypass the problem of relatively high C_{min} available in CMOS technologies – allows to decrease the effective "LSB capacitance" and so power consumption

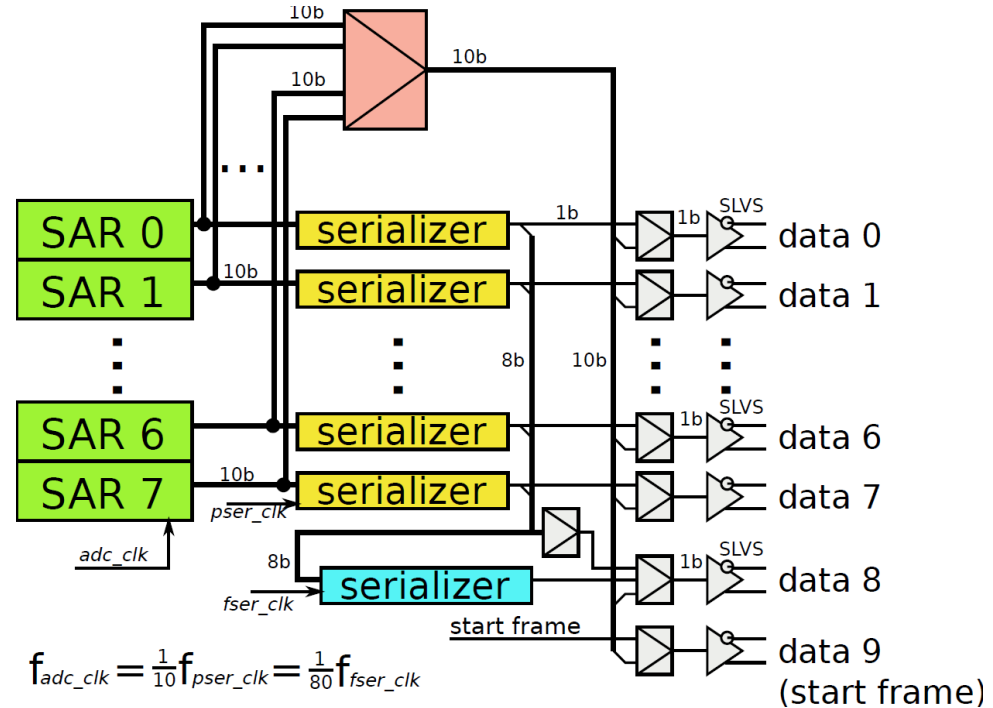


Developments in IBM CMOS 130nm

Development of multichannel SAR ADC

Specifications :

- 8 channels of 10-bit SAR ADC
- Technology IBM 130 nm
- Layout with 146um ADC pitch
- Multimode digital multiplexer/serializer:
 - Serial mode: one data link per all channels (external clk division or PLL clk generation)
 - Parallel mode: one data link per channel (external clk division or PLL clk generation)
 - Test mode: single channel output (max fsmp ~50 Msps)
- PLL for data serialization
- High speed SLVS interface (~1GHz)
- Power pulsing

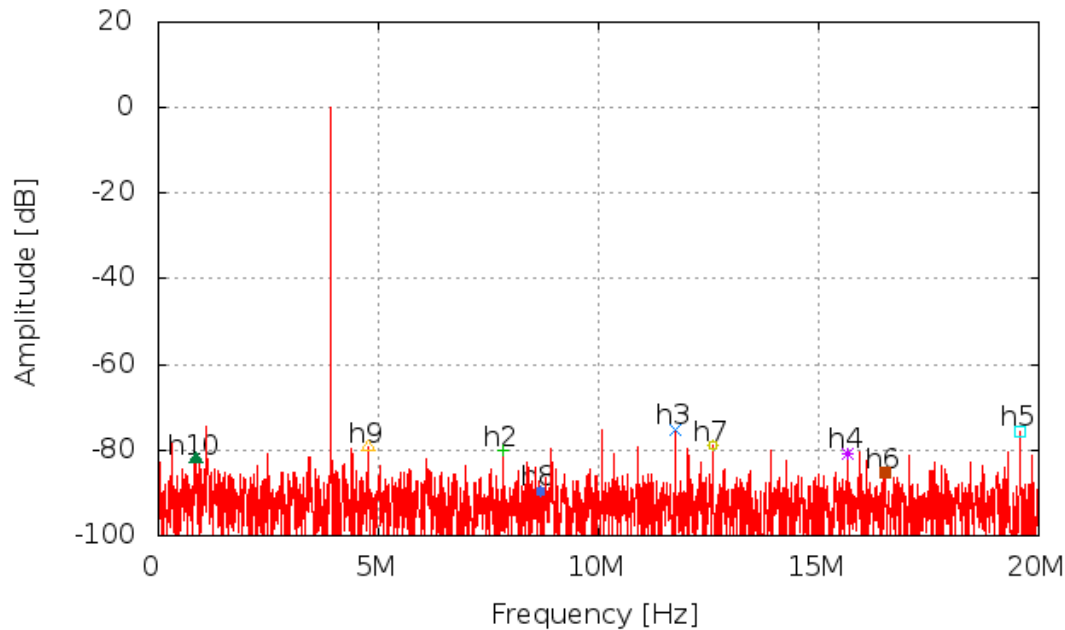


Preliminary measurements

10-bit SAR ADC - Dynamic measurement at 40Ms/S

Sampling Rate = 40.0 MHz
 Input Freq = 3.916 MHz
 Harmonics = 10

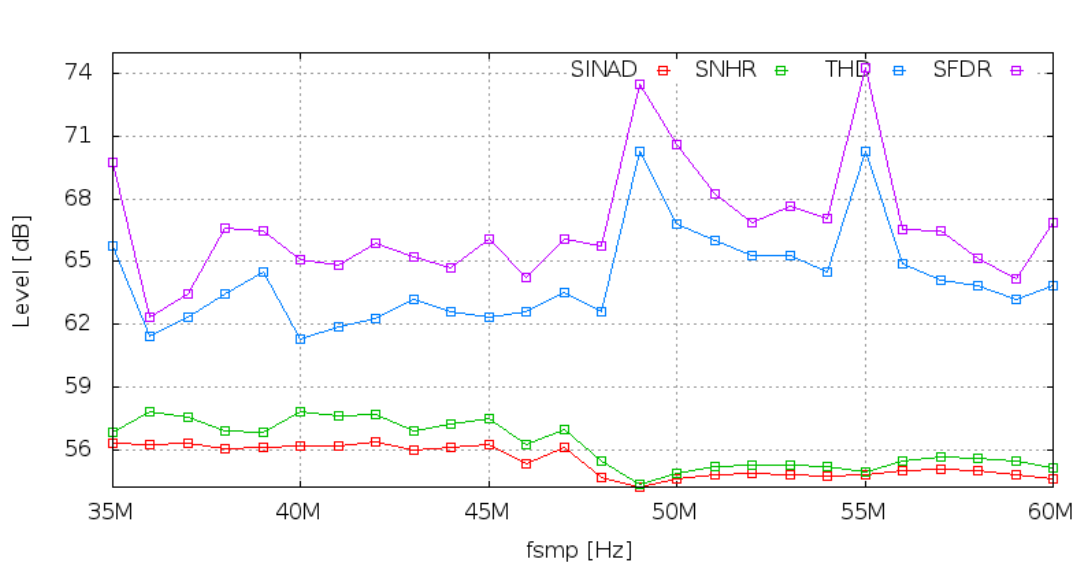
SINAD = 57.0 dB
 THD = -69.6 dB
 SNHR = 57.3 dB
 SFDR = 74.6 dB



- First dynamic measurements show that ADC is fully functional and gives reasonable resolution results
- Quantitative measurements in progress...

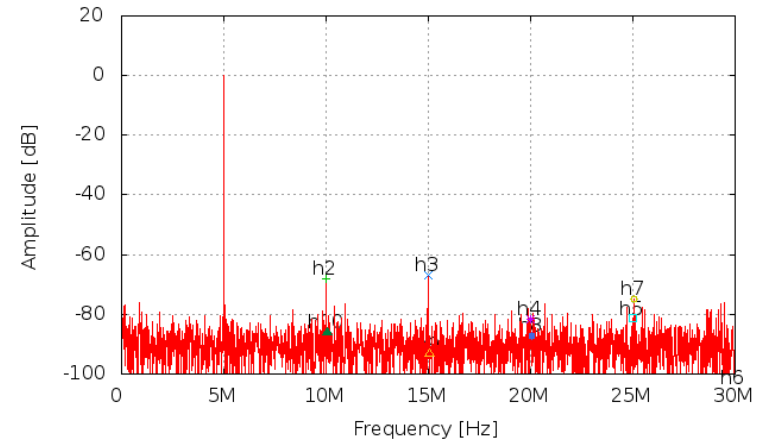
Preliminary measurements

10-bit SAR ADC - Maximum sampling frequency



Sampling Rate = 60.0 MHz
 Input Freq = 4.995 MHz
 Harmonics = 10

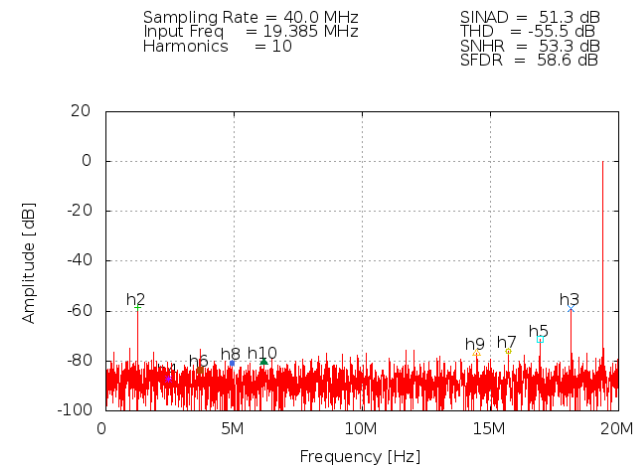
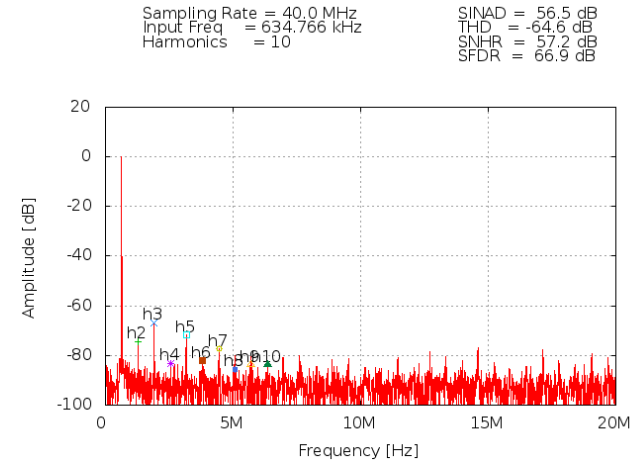
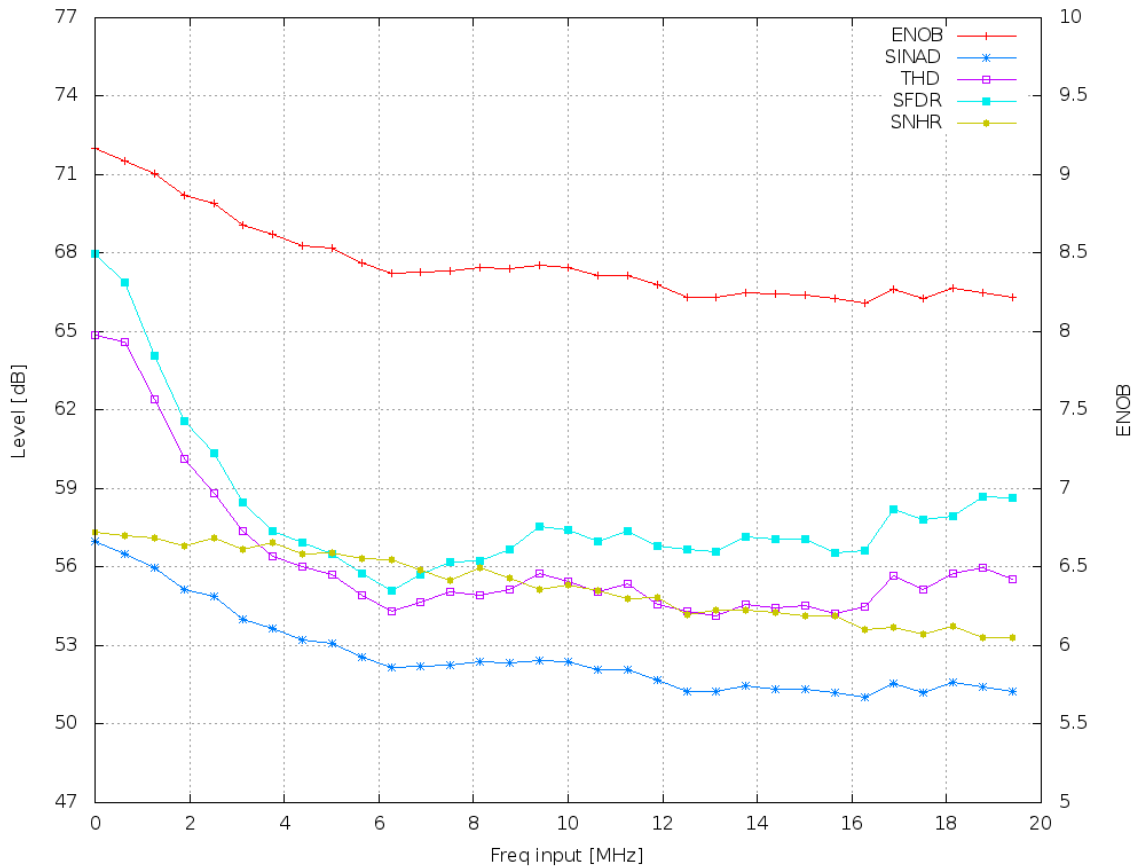
SINAD = 54.6 dB
 THD = -63.8 dB
 SNHR = 55.1 dB
 SFDR = 66.9 dB



- SINAD decreasing above 45 MHz
- It is suspected that measured ENOB was limited by the setup

Preliminary measurements

10-bit SAR ADC - Dynamic measurements – f_{in} scan

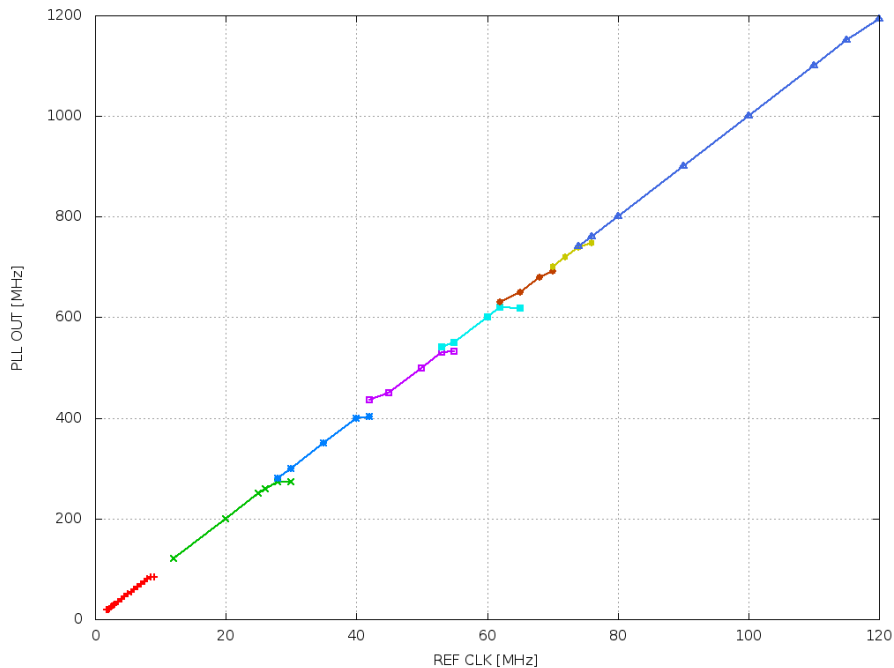


- For low f_{in} ENOB of ≥ 9.2 was measured
- It is suspected that ENOB decrease with f_{in} is partially/mainly due to setup

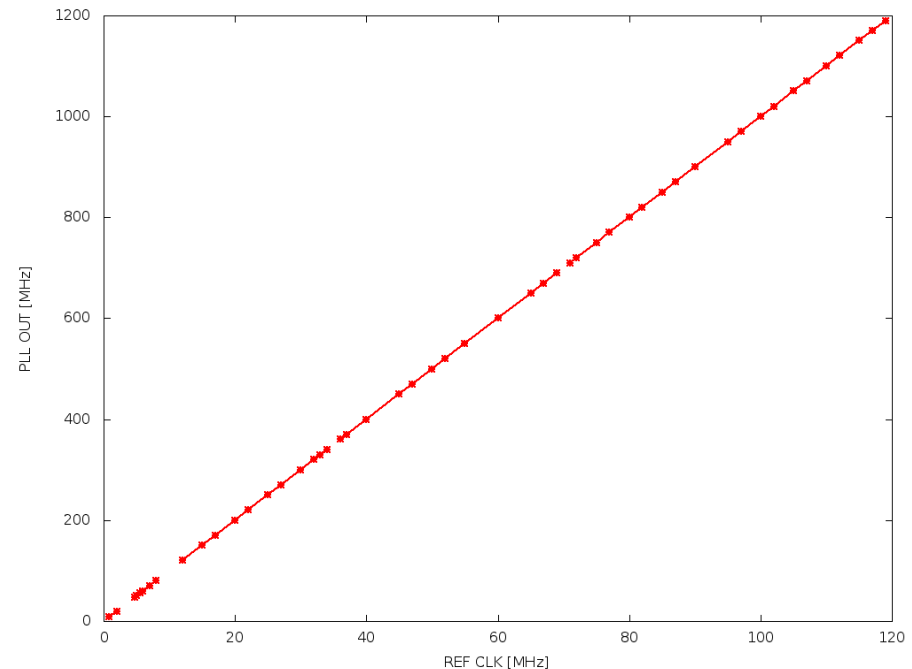
Preliminary measurements

PLL – Transfer function (CLK out vs CLK ref)

Manual mode setting



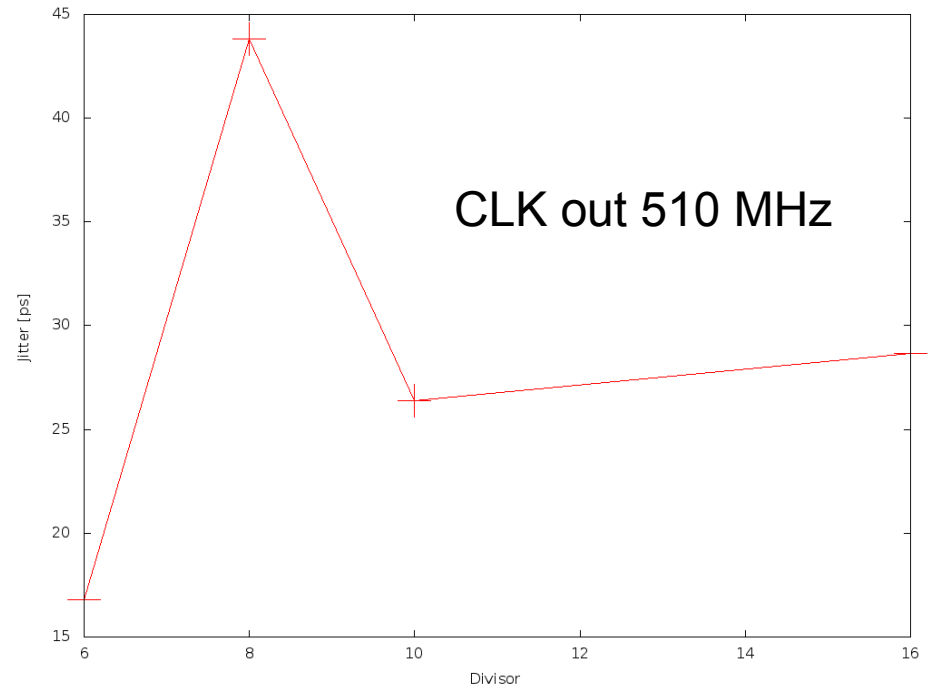
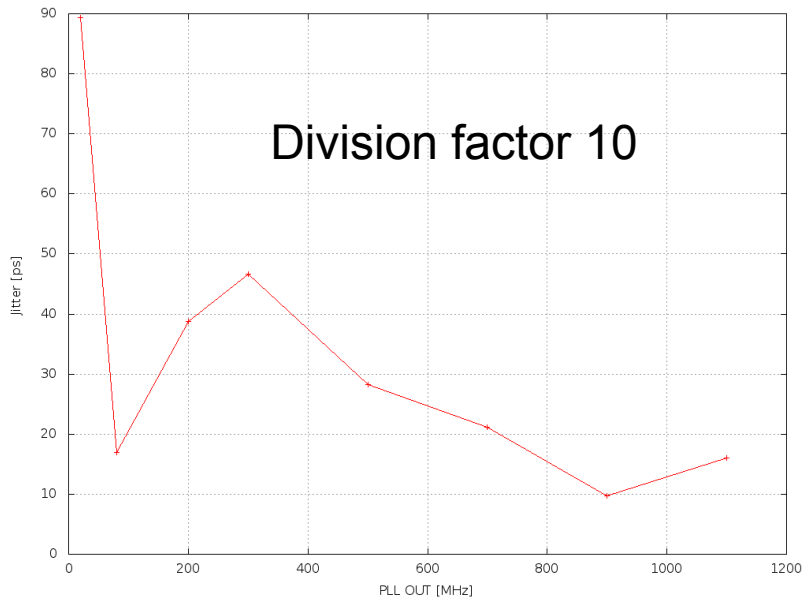
Automatic mode setting



- PLL measurements have just started (~ 2 days) and are in progress...
- PLL output CLK in frequency range 15MHz-1.2GHz already observed
- There are some gaps between frequency ranges...
- Automatic mode detection looks promising
- SLVS driver works at least up to 1.2 GHz (used for PLL output)

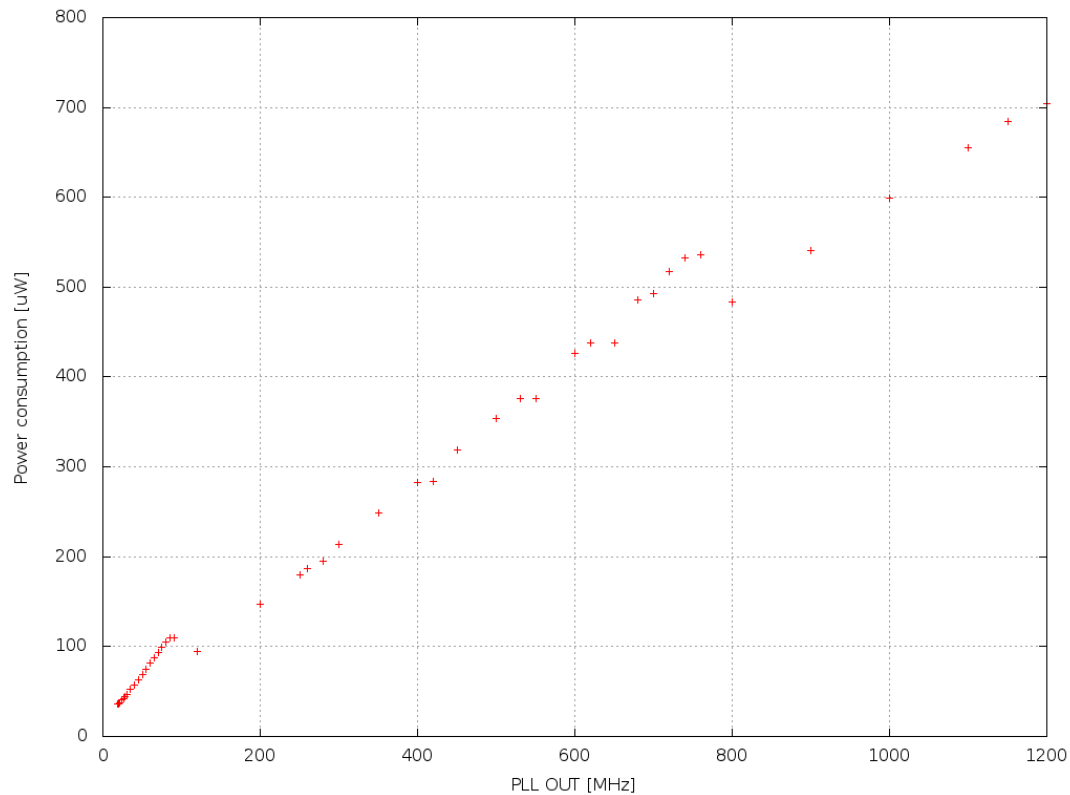
Preliminary measurements

PLL - Jitter



- Measured jitter at least few times higher than simulated (to be verified...)

Preliminary measurements PLL - Power consumption



- Power consumption seems to be higher than simulated (to be verified...) but anyway very low