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Characterization results and first applications of KLauS - an ASIC for SiPM charge and fast discrimination readout

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***Abstract*—KLauS is an ASIC produced in the AMS 0.35μm SiGe technology to read out the charge signals from silicon photomultipliers. Developed as an analog front end for future calorimeters with high granularity as pursued by the AHCAL concept in the CALICE collaboration, the ASIC is supposed to measure the charge signal of the sensors in a large dynamic range and with a high precision. In order to compensate bias and temperature fluctuations of each sensor individually, an 8-bit DAC to tune the voltage at the input terminal is implemented. Using an integrated fast comparator with low jitter, the time information can be measured with sub-nanosecond resolution. The low power consumption of the ASIC can be further decreased using power gating techniques. Future versions of KLauS are under development and will incorporate an ADC with a resolution of up to 12 bit together with blocks for digital data transmission. Most recent characterization results for the KLauS chip are presented as well as results from a KLauS-based test setup developed for mass characterization of scintillator tiles used in the AHCAL test beam program.**

I. Introduction

KLauS (Kanäle für Ladungsauslese von Silizium Photomultipliern) is an analog ASIC for current mode charge read out of silicon photomultipliers (SiPMs). The 12 channel test chip aims at providing a readout system of scintillating tiles with silicon photomultipliers, integrated in a calorimetry system for a future linear collider experiment. The AHCAL concept developed within the CALICE collaboration plans to build such a system, using tiles of plastic scintillator, silicon photomultipliers and integrated electronics in a sandwich calorimeter. One of the main constraints in such a system is the very low allowable power consumption of the electronics. Using power gating techniques, the total power consumption is decreased to 25μW per channel for the nominal ILC bunch crossing scheme, allowing to switch off the electronics 99% of the time.

II. Channel description

Fig. 1 shows the channel diagram of KLauS. The input stage copies the signal current to the analog integration and shaping path for charge measurements, and to the trigger path for timing measurements. Each of the 12 channels of the ASIC hold a 8-bit digital to analog converter to adjust

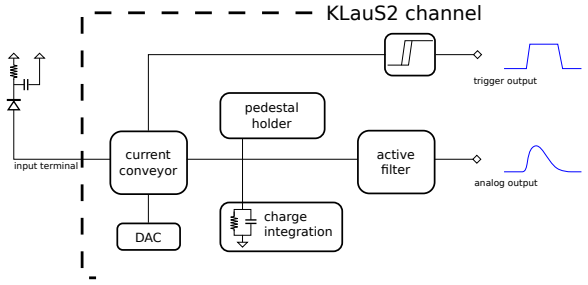

Fig. 1. Channel diagram of KLauS. SiPM is indicated as a diode.

the DC input terminal voltage to compensate for variations in the operating voltage of the silicon photomultipliers due to sensor production or temperature fluctuations. The topology of the input stage is a current conveyor specialized for power gating operation, allowing a very low input impedance for the channels and efficient charge collection by the later integration stage. This yields a high signal to noise ratio even for low gain silicon photomultipliers. The input stage topology is sketched in Figure 2. The input impedance is decreased by boosting the g_m of the input transistor M1 using a current mode feedback. The signal current is copied to a feedback path by transistors M2 and M3 and generate a voltage change at the gate of M1. Transistors M4 together with the input transistor M1 act as source followers and allow to adjust the DC input terminal voltage using the *DAC* input terminal of the current conveyor. For measurements of the signal charge, the signal current is copied using the pair M2, Mi in Figure 2 and integrated in a passive integration stage. A discrete gain switching unit allows a dynamic range of more than 200pC for large area SiPMs. The pedestal voltage is defined and stabilized using a sub-threshold operational amplifier in the analog signal path with a bandwidth in the order of kHz. The integrated charge is converted to a pulse height voltage signal using an active shaper with configurable time constant. As the time constants of integration circuit and shaping stage coincide, the output pulse can have a short decay time and no undershoot to reduce pile up effects from the SiPM dark pulses. This allows precise charge

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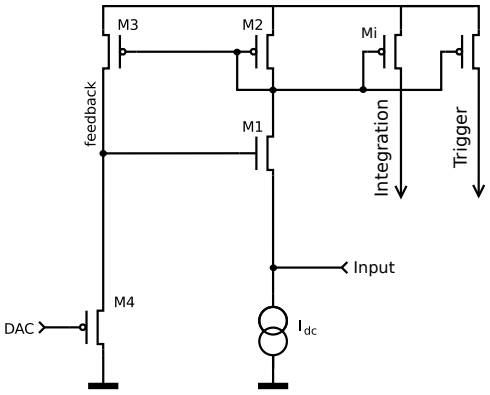

Fig. 2. KLauS input stage topology

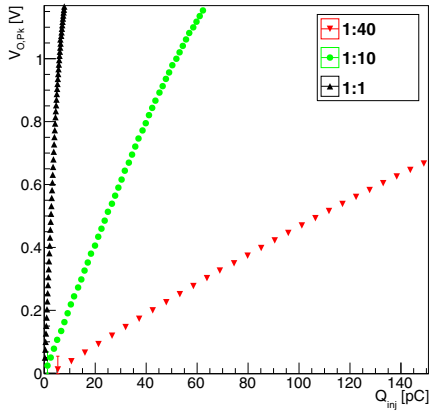

Fig. 3. Peak voltage response for the different scaling configurations in a charge injection measurement with $C_{inj} = 33$pF. The 1 volt pedestal is subtracted

measurements even for dark count rates in the order of several MHz, as commonly seen in 3×3mm^2 silicon photomultipliers.

For timing measurements, the signal current is copied to a comparator path. A monoflop circuit is implemented to filter noise triggering pulses at the falling edge of the input signal. For a typical MIP signal of 660fF, the electronic time jitter was measured to be less than 60ps [2]. The charge noise of the comparator was measured to be in the range of 10fC.

To decrease the power consumption, the different blocks of the channel can be power gated. The nominal bunch crossing scheme of the ILC foresees a bunch train spacing of 200ms and a bunch train length of about 2ms. Therefore the power consuming blocks of the readout electronics can be switched off up to 99% of the time, allowing to keep the power consumption within the constrained value of 25μW per channel. Later signal processing stages of the analog front-end can be switched off completely during the time without beam. However, the input stage has to maintain a stable DC voltage at the input terminal connected to the silicon photomultipliers at all times to keep the sensors in stable gain conditions. Therefore the DC current of the input stage is only decreased in power-gating mode and compensation circuitry is implemented to reduce the voltage differences between *on* and *off* state.

III. Characterisation Results

To simulate the ASIC response to silicon photomultiplier signals, charge injection measurements were performed. Fig. 3 shows the output response for the different scaling settings in a charge injection measurement. The used injection capacitance of 33pF corresponds to the typical detector capacitance of 1×1mm^2 silicon photomultipliers. For large area detectors with a capacitance of 440pF, a linear range of 220pC was measured [2]. The equivalent noise charge generated by the ASIC for the high gain scaling configuration was determined to be 21500e$^-$ at an input capacitance of 33pF, allowing a precise estimation of the sensor gain using single photon spectra even for low gain SiPMs. For a Hamamatsu S11028-025 MPPC at nominal gain conditions, the signal to noise ratio was measured to be larger than 8 for a single pixel signal, dominated by the MPPC signal fluctuations as SiPM excess noise and dark count pileup contributions. The ASIC contributes about 12.5% to the width of the 1 P.E. peak in the single photon spectrum.

Each of the 12 channels of the ASIC have an integrated 8-bit DAC to tune the DC voltage of the input terminals connected to the sensors within 2V at an integrated non-linearity smaller than 2.5%, with a resolution of approximately 9mV per LSB. Figure 4 shows a voltage scan at the input terminals for all channels of the ASIC.

The power pulsing capability of the ASIC allows to decrease the power consumption to a minimum. With the nominal bunch crossing scheme for the ILC [1] summarized in section II, the power consumption is decreased to 25μW per channel. For all configuration settings, the terminal voltage at the input terminals of the channels varies less than 20mV when comparing the 'on' and 'off' state of the chip, keeping the

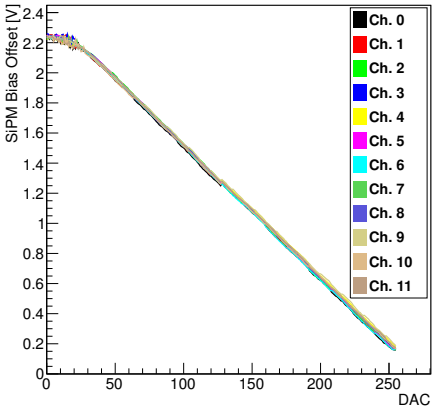

Fig. 4. Voltage at the input terminal of the KLauS channels for varied DAC configuration values

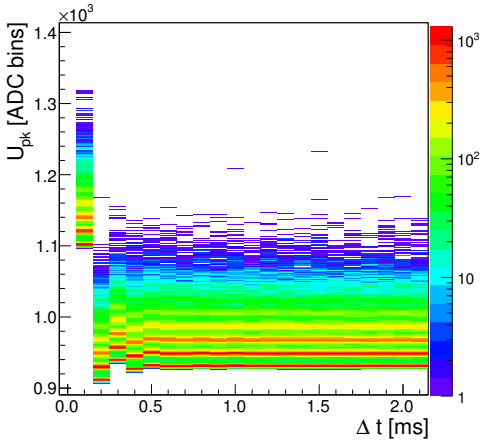

Fig. 5. Peak voltage spectra in power-gated mode. The number of entries in each ADC bin and time slice are indicated color-coded.

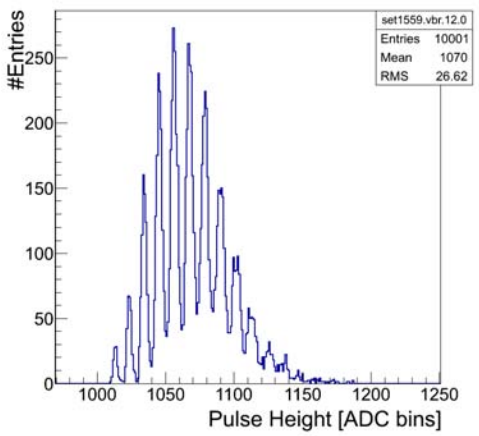

Fig. 6. Single photon spectrum measured with a KETEK PM1125 SiPM

gain of the sensors stable at all times. Figure 5 shows single photon pulse height spectra using a 50μm pitch Hamamatsu MPPC and a pulsed LED for different times after switching on the chip. The MPPC is illuminated with a LED at different times after the rising edge of an external power-gating clock signal and the peak voltage at the output terminal is measured using a peak sensing ADC. Single photon spectra are visible 100μs after switching on. Comparing the peak widths in the spectra for continuously running and power-gated mode, the electronic noise is decreased by about 20% as low frequency noise contributions are removed due to short duty cycle.

IV. Current Applications

The CALICE collaboration is running an extensive test beam program, for which the scintillator tiles and attached SiPMs have to be characterized and tested for functionality. Furthermore, methods to characterize the large quantity of tiles for a full detector within a reasonable timescale are to be evaluated. The properties of KLauS, especially the high signal to noise ratio and the pileup compensating shaper, make the ASIC very suited for testing the characteristics of the scintillating tiles. Two prototype setups using the KLauS ASIC have been set up, allowing semi-automated characterization of 12 tiles in parallel. A small system allowing temperatures characterization of 12 tiles, and a larger scale setup have been built. Figure 7 shows a picture of the large scale setup in commissioning inside a light proof box. It consists of a palette into which 216 tiles can be inserted, a moving stage and a positioning head. The readout electronics and a calibrated fiber systems are moved automatically to the 18 measurements stations of the palette, each consisting of 12 readout channels. The tiles are lit with a pico-second UV laser and single photon spectra, as well as dark rate spectra are measured for various operating voltage points. Figure 6 shows a sample spectrum measured for tiles using a KETEK PM1125 SiPM with a nominal gain of $7 \cdot 10^5$. Silicon Photomultiplier gain and light yield are calculated to estimate the optimal bias voltage for

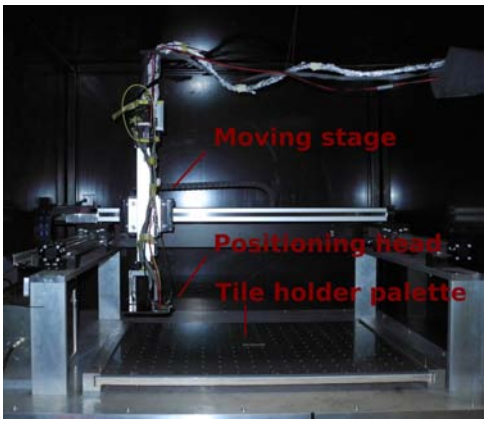

Fig. 7. Large scale tile characterization prototype.

each tile in the calorimeter stack. A full tile characterization is performed within 2-4 seconds making use of the 12 channel parallelization.

V. Future Developments

In order to develop a full readout system in a mixed mode ASIC, an ADC is being developed. For the later application, different quantization resolutions are needed. The measurement of single photon spectra to calibrate the SiPM gain, a high resolution quantization of 12bit is required. For timing measurements with a quantization of 400ps per bin, 10 bit resolution is sufficient. The energy measurement for calorimetry require only 8bit quantization as the fluctuations of the landau distributed signals are large. Addressing the constraints on the power consumption and the relatively low maximal event rate in the order of MHz, a pipelined, partially cyclic structure of successive approximation & registration (SAR) ADCs is proposed. Its basic structure is depicted in Fig. 8. The SAR ADCs are designed for low power consumption and making use of the pipelined structure, the time and energy informations can be converted partially in parallel. Together with a peak sensing unit, the ADC will be capable of measuring full events

with a rate of 1-3 MHz. This leads to a minimum of analog memory cells prior to the conversion stages. For the 12bit high resolution mode where conversion speed is not constrained by the bunch crossing scheme, the second SAR stage will be cyclic. Future versions of the KLauS frond-end as well as

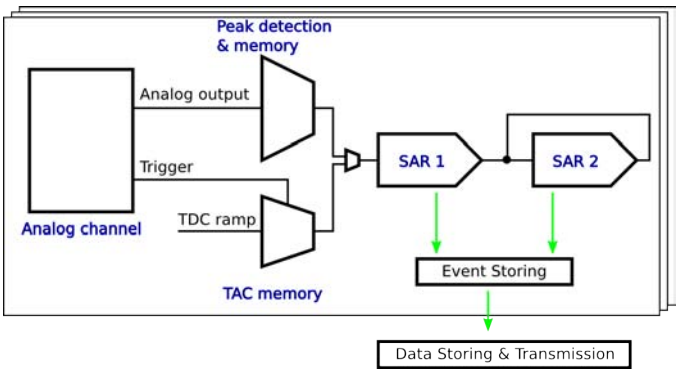

Fig. 8. Structure of the ADC being developed for future versions of KLauS

the ADC are being designed in UMC 0.18μm technology. This allows to decrease the power consumption further by only using 3.3V supply where necessary, and to make use of smaller digital circuit and twin well transistors for shielding of substrate noise from the digital parts.

VI. Conclusions

The KLauS ASIC is a low power analog front-end for Silicon Photomultiplier readout in HEP calorimetry applications developed in AMS 0.35m SiGe technology. Each channel includes a 8bit ADC to allow adjustment of the SiPM bias voltage, providing means to correct for temperature and breakdown voltage fluctuations. The internal comparator provides a trigger signal with a time jitter of less than 60ps for a typical MIP signal. The implemented power-gating scheme provides ultra low power consumption of 25μW to comply with the constraints of a future linear collider experiment's calorimeter. The characterization measurements of the power-gating functionalities show a fast start up time of the circuit after a power-gate clock edge. The high signal to noise ratio for single photon signals make the ASIC suitable for characterization measurements of the AHCAL calorimeter tiles, also providing high quality pulse height spectra for low gain silicon photomultipliers. Future versions of the ASIC are being developed including an ADC and peak sensing unit. A pipelined SAR structure to achieve a low power consumption and sufficient digitization speed.

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