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Radiationhard components for the control system of a future ATLAS pixel detector

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Radiationhard components for the control system of a future ATLAS pixel detector

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ABSTRACT: The upgrade of the ATLAS experiment for the High Luminosity LHC (HL-LHC) will include a new pixel detector. A completely new detector control system (DCS) for this pixel detector will be required in order to cope with the substantial increase in radiation at the HL-LHC. The DCS has to have a very high reliability and all components installed within the detector volume have to be radiationhard. This will ensure a safe operation of the pixel detector and the experiment. A further design constraint is the minimization of the used material and cables in order to limit the impact on the tracking performance to a minimum. To meet these requirements we propose a DCS network which consists of a DCS chip and a DCS controller. In the following we present the development of the first prototypes for the DCS chip and the DCS controller with a special focus on the communication interface, radiation hardness and robustness against single event upsets.

KEYWORDS: Detector control systems (detector and experiment monitoring and slow-control systems, architecture, hardware, algorithms, databases); Digital electronic circuits

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1 Introduction

This paper describes the design of components for a new control system for the ATLAS pixel detector which is under development for the HL-LHC. The current baseline design of the future pixel detector consists of up to five barrel and endcap layers out of which the two innermost barrel layers are insertable and thus interchangeable. The pixels of the outer detector layers are of a size of $50 \times 250 \mu\text{m}^2$. The detector covers the area up to $|\eta| \leq 2.5$ with detector modules. In the barrel the detector modules are mounted on staves, in the endcaps on disks. Depending on the layer up to 32 detector modules form a stave. This results into approximately 6000 detector modules, that need to be powered, controlled and readout.

Each stave is connected to the readout system in the counting room via an End-of-Stave (EoS) card, see figure 1. Each half stave or disk sector, is connected to the readout chain, power supplies and the control system. The actual signal readout is based on optical links. The outer pixel layers will use the Giga Bit Transceiver (GBT) [1] chip set as the EoS controller. The data are sent to the data acquisition (DAQ) crates via an opto electrical transceiver, located a few meters away from the pixel detector. The pixel modules require two supply voltages: a depletion voltage for the pixel sensors, and a low voltage for the analog and digital circuits of the front end readout chips. For the low voltage supply two powering schemes are under investigation: a serial powering scheme and a parallel powering scheme using DC-DC converters. Both of these powering schemes are taken into account for the design of the detector control system. Furthermore the electronics at the EoS card and the opto electrical transceiver need to be supplied with low voltage. The DCS monitors the detector modules, the EoS card, the optical interface and the environmental parameters.

The requirements on the DCS include a very reliable operation in the harsh radiation environment at the HL-LHC. For the innermost pixel layer the electronics must withstand an ionizing dose of 570 MRad, a fluence of 13.4×10^{15} 1 MeV neutron equivalent/cm² from non ionizing particles (NIEL) and a flux of $2.4 \times 10^9 \frac{1}{\text{cm}^2\text{s}}$ [2] able to produce Single Event Effects (SEE) (hadrons with

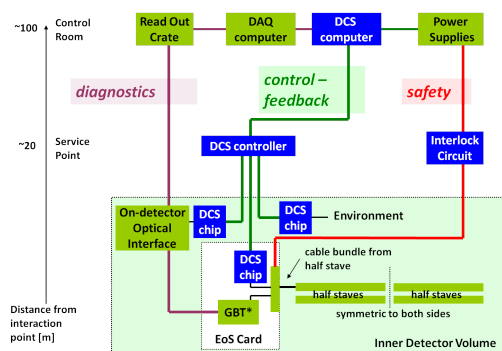


Figure 1. DCS architecture.

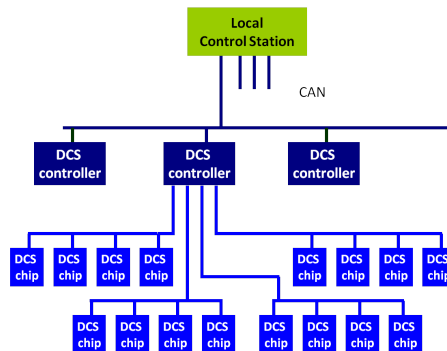


Figure 2. DCS network.

a momentum above 20 MeV/c). The development of the powering scheme as well as the new DCS is constrained by the currently available space for services in the ATLAS central detector region, even though the number of readout channels will increase substantially.

2 DCS architecture and DCS network

The DCS architecture [3] is based on three completely independent paths into the detector. Each path stands for a different level of reliability, there is a safety, a control & feedback and a diagnostic path. All tasks of the control system (see figure 1) are mapped onto these paths.

The safety path is a hardwired interlock circuit, that can directly turn off detector parts in case of danger. It has the highest level of reliability and must be in operation at all times. It has a low granularity in order to minimize the required material in the inner detector.

In the control & feedback path all parameters, that are essential for the operation of the detector, are monitored and controlled. Therefore it requires a high reliability. The control & feedback path must be available for all use cases, e.g. the assembly of the detector, qualification tests and the commissioning phase. Hence it must be independent of the readout chain. The granularity for control and its feedback is either per detector module or per half stave. In order to meet the constraint on the number of wires in each area of the detector the concept for the control & feedback path is a DCS network, that is described below. To perform all of the necessary monitoring and controlling, the control & feedback path must be able to measure voltages, currents, temperatures and humidities, to switch channels on or off and to change target values.

The diagnostics path provides detailed information, that can be merged into the data stream on request e.g. during calibration. The information will be given per front end chip. This service will only be available during the operation of the readout chain.

Due to the strong limitations on the number of lines for the DCS it is not possible to wire all sensors installed in the detector to the counting room. The information provided by the control & feedback path must therefore be processed and digitized close to the detector modules. The processing and digitalization of data will be done by the DCS chip, that will collect information from the modules and send commands to the modules. The DCS chip will also be used to supervise the EoS controller, the optical interface and to perform the environmental measurements (see blue DCS chip boxes in figure 1). Outside of the central detector region at a distance of about 20 m

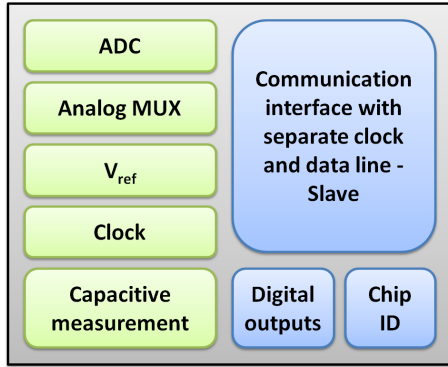


Figure 3. Schematic of the DCS Chip.

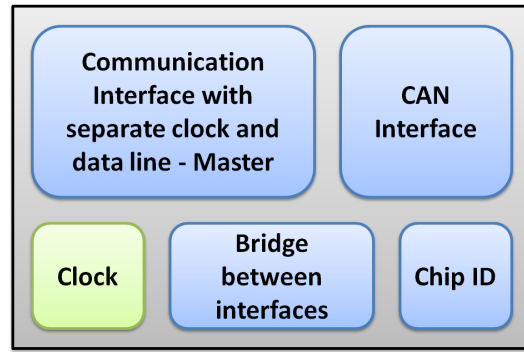


Figure 4. Schematic of the DCS Controller.

from the pixel detector the DCS chip lines will be combined at a DCS controller, so that 4×4 DCS chips are connected to one DCS controller. A fieldbus shared by several DCS controllers is used for the connection to the DCS computers located in the control room. Figure 2 gives an overview of the DCS network in the control & feedback path consisting of DCS chips and DCS controllers. It represents a compromise between the highest possible reduction of cables and the minimization of the risk to lose the control of DCS items.

3 The DCS chip

The DCS subjects, that are supervised and monitored by the DCS chip, are the detector modules, the EoS controller, the optical interface and the environmental parameters. Therefore the tasks of the DCS chip are to measure voltages, temperatures and humidities, to control the bypass for serial powering and to reset the EoS controller or the optical interface. Due to its location the DCS chip needs to be as radiation hard as the components of the innermost layer of the pixel detector (see Introduction). The number of lines to the outer world and to the detector modules should be low and the chip must be suitable for the serial and parallel powering concept (very different voltage levels of the front end electronics). Furthermore the power consumption needs to be low for an operation without cooling.

The design of the DCS chip consists of an analog part and a digital part (see figure 3). The analog part consists of a 10-bit differential ADC, an analog multiplexer, a reference voltage, a clock to synchronize the ADC and two identically working RC oscillators for the readout of capacitive humidity sensors. The digital part includes storage registers for the ADC data and digital outputs, that are necessary to forward commands to the DCS subjects. Altogether at least 35 ADC channels and 17 digital outputs for the bypass control of serial powering and for the reset of the EoS controller are required on each chip. Furthermore the DCS chip has to have a communication interface, which includes a clock line in order to avoid timing problems due to radiation damage. A transmission rate of at least 100 kbit/s over 20 m cables is foreseen.

To obtain the high radiation hardness necessary for the DCS chip, it will be produced in the same deep submicron process, that is used for the front end readout chips. Besides a radiation hard chip production process the registers of the chip and the interface have to be protected against single

The DCS chip core features:

- I2C-HC slave
- Inputs for ADC data
- 3 digital outputs
- 2 16-bit counters

The DCS controller core features:

- Standard CAN node
- I2C-HC master
- Bridge to translate between the interfaces

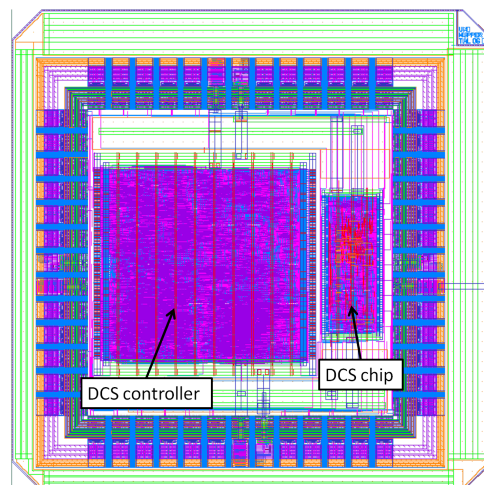


Figure 5. Layout of the CoFee1 chip.

event upsets (SEU). This is especially important for the registers of the digital outputs because it would be fatal for the operation of the detector to wrongly switch modules on or off. Power, data and clock will have separate lines. Data is sent via a differentially wired I²C bus to a master located outside of the central detector. To avoid errors due to SEU, the actual processing done on the DCS chip is limited to the essential minimum. This also reduces the power consumption.

4 The DCS controller

The DCS controller is a node connecting the signals from several DCS chips with the control station in the counting room by a single bus. It has to withstand the radiation level inside of the ATLAS cavern, since it is located at a service point inside of the detector. Therefore it is produced in the same deep submicron process used for the DCS chip and equipped with redundant registers that improve the robustness against SEU. The DCS controller (see figure 4) will mainly be a digital design. Its sole analog components are a system clock and a physical layer (driver circuit) for the differential communication lines. For the communication interface to the counting room the CAN (Controller Area Network) [4] protocol was chosen. It is very robust against errors and is compatible with the existing ATLAS DCS infrastructure. For the CAN node a local system clock is needed as CAN does not provide a separate clock via the interface. The clock is also needed for the implementation of the DCS chip interface because the DCS controller provides the DCS chips with a clock line. Furthermore a bridge is implemented to transform the received data from one interface protocol into another. The DCS controller is also equipped with a chip ID.

5 The CoFee1 chip

The CoFee1 chip is a digital prototype for the DCS chip and the DCS controller, see figure 5.

Due to cost efficiency both cores were implemented in one chip. Triple modular redundancy (TMR) was implemented to ensure the robustness of the design against SEU. A special version of

the I²C interface (I2C-HC) is implemented for the digital communication between the DCS chip (slave mode) and the DCS controller (master mode).

I2C-HC is a standard I²C interface extended by a (12,8) Hamming code [5], that can correct a single error. The probability of an undetected error in 10 years and for 100 chips was calculated to be 4×10^{-7} for the I2C-HC interface implemented on the CoFee1 chip. For the implemented CAN interface the probability of an undetected error in 10 years and for 100 chips was calculated to be 1.82×10^{-19} .

The CoFee1 chip was submitted in June 2010 and will be produced in a 130 nm technology.

6 Summary and outlook

The ATLAS pixel detector at the HL-LHC requires a completely new detector control system. The DCS architecture is based on three independent paths: safety, control & feedback, and diagnostics. In order to minimize the material and stay within the available volume a DCS network consisting of DCS chip and DCS controller has been developed for the control & feedback path. These two chips, the DCS chip and the DCS controller, digitize, collect and transmit monitoring data and commands. Their requirements have been defined and a first radiation hard prototype for their digital components, the CoFee1 chip, has been submitted for production.

Once the CoFee1 chip has been tested for functionality, intensive SEU studies will follow in order to verify the theoretical numbers given above. It also will be possible to build and test the communication chain of the control & feedback path and a DCS network with the CoFee1 chips. The design of the analog components (physical layer for the interfaces and the ADC) has already started.

Acknowledgments

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