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Studies for the detector control system of the ATLAS pixel at the HL-LHC

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ABSTRACT: In the context of the LHC upgrade to the HL-LHC the inner detector of the ATLAS experiment will be replaced completely. As part of this redesign there will also be a new pixel detector. This new pixel detector requires a control system which meets the strict space requirements for electronics in the ATLAS experiment. To accomplish this goal we propose a DCS (Detector Control System) network with the smallest form factor currently available. This network consists of a DCS chip located in close proximity to the interaction point and a DCS controller located in the outer regions of the ATLAS detector. These two types of chips form a star shaped network with several DCS chips being controlled by one DCS controller. Both chips are manufactured in deep sub-micron technology. We present prototypes with emphasis on studies concerning single event upsets.

KEYWORDS: Control and monitor systems online; Radiation-hard electronics; Detector control systems (detector and experiment monitoring and slow-control systems, architecture, hardware, algorithms, databases); Digital electronic circuits

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Contents

1 Introduction

To cope with the increased luminosity of the HL-LHC[1] several upgrades for the ATLAS experiment are scheduled. In line with these upgrades the inner detector of the ATLAS detector will be replaced entirely. As being a part of the inner detector, a new pixel detector is currently under development. The basic unit is a detector module consisting of a sensor with pixel cells of $\leq (50 \times 250)\,\mu m^2$ and two to four front end read out chips, which are bump bonded to the sensor cells. Several designs for a new pixel detector are currently under discussion however all are based on the stave concept. In this concept the detector modules are mounted on support structures, staves, with integrated cooling pipes which are installed parallel to the beam pipe. At the ends of each stave, an End-of-Stave card (EoS-Card) is assembled to supply the power for the modules and to link them with the optical transceiver which is sending the data to the counting room via optical fibers. The staves are installed next to each other forming cylindrical shells, which are concentrically around the interaction point and the beam pipe. To detect events with a high pseudo rapidity, disks or cone shaped structures carry the detector modules in the end caps. All together the pixel detector will cover a pseudo rapidity up to $\eta = 2.5$. As being the detector with the smallest distance to the interaction point, electronics of the pixel detector have to be designed to withstand a high dose of radiation. According to the expected irradiation of the pixel detector in the ATLAS TDR [1] and the increase in design luminosity by a factor of 10, we estimate a radiation dose of 300 MRad for the new pixel detector at the HL-LHC.

To ensure stable and reliable operation of the new ATLAS pixel detector also a completely new detector control system (DCS) is necessary. To be able to fit into the new ATLAS detector, this

[1] High Luminosity Large Hadron Collider

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Component	Monitored values		Controlled values
Modules	HV	Current & Voltage	Voltage setting & On/Off
	LV	Current & Voltage^{m}	Voltage setting & On/Off^{s}
	Temperature^{m}		
End of Stave Cards	Current & Voltage^{m}		Voltage setting & On/Off
	Temperature^{m}		
			Reset^{s}
On detector Opto transceiver	Current & Voltage^{m}		Voltage setting & On/Off
	Temperature^{m}		
			Reset^{s}
Environment & Cooling	Humidity^{m}		
	Temperature^{m}		

Table 1. Table of DCS values that are relevant for save detector operation. The table shows which values have to be monitored and/or which values have to be steered. (^{m}: monitored by DCS chip, ^{s}: steered by DCS chip.)

DCS has to meet several requirements such as low material cost to ensure a minimal impact onto the measurements of the other ATLAS sub-detectors. A low power consumption of DCS electronics located inside the detector is also necessary as active cooling for the DCS can not be guaranteed at all times. Further the same radiation hardness as the ATLAS pixel electronics has to be ensured in those DCS components close to the interaction point as well as compatibility with the global ATLAS DCS framework. Under these circumstances the DCS has to reliably monitor and steer all quantities relevant for the operation of the pixel detector (see table 1). All of these quantities have to have individually defined properties in severity, availability, granularity and location of processing. For the powering of the pixel detector there are two concepts at the moment: a serial powering concept or a parallel powering concept based on the usage of DC-DC converters.

2 DCS concept

The new DCS is divided into three paths which have different tasks. The first and most reliable path is the safety path. The safety path is a hard wired interlock system to which the user has only limited access. It is running all the time, even when the detector is switched off and has individual lines for all its provided services. This leads to the highest reliability but also the lowest granularity of all three paths which is per cooling loop or half stave[2]. The interlock system has the ability to switch off parts of the detector or the entire detector if a safe operation cannot be guaranteed. The second path is the control and feedback path. This path is made up by the 'DCS network' which will be described in the next subsection. It is handling all the use cases (e.g. calibration, connectivity tests and data taking) and it steers and monitors the detector modules, EoS-Cards and the optical interface. Its reliability is the second highest in the DCS as it is independent of the data path of the pixel detector. The granularity is per half stave or module[3] and thus higher than in

[2]The exact topology has yet to be defined.
[3]The exact topology has yet to be defined.

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the safety path. The third and last path is the diagnostics path. This path is only available during calibration periods as its data is merged into the data readout of the pixel detector. Thus it has the lowest reliability but the highest granularity which is per front end chip.

2.1 DCS network

As mentioned above, the control and feedback path is made up of the 'DCS network'. This network is a compromise between minimizing material and highest possible granularity and reliability in control of DCS items. There are two major components in the DCS network, the DCS controller which is located at a service point in the muon chambers ($\sim 20\,\mathrm{m}$ from the interaction point) and the DCS chip located at the EoS-Card (less than 1 m from the interaction point). These two chips form a star shaped network. Four bus lines, with four DCS chips each, are connected to one DCS controller which is connected to the DCS computers in the counting room. Due to the length of the cables between the DCS chip and the DCS controller data is transmitted via differential lines to allow rates up to 125 kbaud. The data transfer inside the DCS network is realized by the I2C-HC protocol. I2C-HC is a modified I^2C [2] protocol which was extended with a (12,8) Hamming code [3] to allow correction of single and detection of dual bit flips by adding four parity bits to the end of each data package. To transmit data from the DCS controller to the DCS computers in the counting room, a customized CAN protocol [4] with lowered voltage levels is used.

To be independent from the power supply of the detector and to make the DCS data communication more reliable, the DCS chip and the DCS controller have their own power, data and clock lines. Additionally to minimize the size of the chips and the risk of falsified data, the computations in the DCS chip and controller are reduced to a minimum and all data processing is done in the counting room.

2.1.1 DCS chip

The DCS chip is located on the EoS-Card and it controls the corresponding half stave. Its tasks are to monitor and steer the quantities described in table 1. Therefore it is equipped with several analog and digital blocks (see figure 1): A 10 bit ADC measures voltages, and temperatures via NTCs[4]. The sampling rate of the ADC will primarily be determined by the transmission rates in the DCS network. Due to the clock rate of the I2C-HC bus, the sampling rate will be in the range between 5 kHz and 10 kHz[5]. To provide the necessary amount of analog inputs on the chip an analog multiplexer with 16 inputs multiplexes the analog channels of the DCS chip to the ADC. Environmental humidity is measured by two identically working RC oscillators which are connected to two 16 bit counters by which one of the capacitors is a humidity sensor and the other a reference capacitor. The digital core of the chip is working as a slave to the DCS controller to which it communicates via the I2C-HC encoder. To switch modules on and off each DCS chip has 8 digital outputs.

Switching modules on and off is a very critical process and allows no errors. Due to the location so close to the interaction point, where the radiation levels are very high, several precautions have to be made to ensure reliable operation of the DCS chip. Therefore the DCS chip is manufactured in a commercial 130 nm CMOS process which is known to be very radiation tolerant [5].

[4] Negative Temperature Coefficient

[5] In case of an ADC clocked by the I2C-HC bus.

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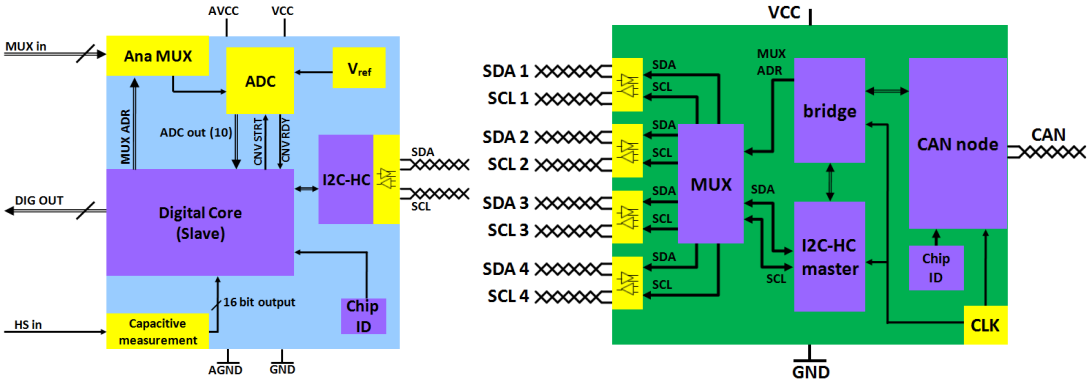

Figure 1. Sketch of the components of the DCS chip (left) and the DCS controller (right).

Besides that the DCS chip's registers are made up with triple modular redundancy (TMR) to eliminate the danger of SEU[6]. This means that every register has two clones in the chip. A majority voter on each triple register corrects every single bit flip as long as the other two bits are not flipped.

As the DCS chip needs to be optimized for low power consumption, it is not continously clocked. To operate the DCS chip it has to be provided with an external clock which comes from the DCS controller during communication between chip and controller. The neccessary clock for the majority voter is generated by the rising edge of the error signal which is delayed to use it as a clock for the correction of the falsified register.

2.1.2 DCS controller

The DCS controller builds the bridge between the DCS chip and the DCS computers in the counting room. It is located in a service point 20 m from the interaction point inside the muon chambers. The tasks of the DCS controller are to receive data via the CAN bus from the DCS computers and pass these data to the correct I2C-HC bus with the corresponding DCS chip attached to. To carry out these tasks the DCS controller has the following components built in (see figure 1): A CAN node in the controller receives data packages from the CAN bus, decodes and passes them to a bridge. This bridge extracts parts of the data package's address which is given to a multiplexer together with the rest of the package's data. With the extracted address parts the multiplexer decides to which of the four I2C-HC buses it transmits the data translated by a I2C-HC master block in the chip. Once the connection path from the CAN node to a DCS chip has been established, it stays active until the communication process, which also includes an answer from the DCS chip, is complete. The DCS controller also supplies the clock for the DCS chip via the SCL lines on the I2C-HC bus.

To ensure radiation tolerance, the DCS controller is manufactured in the same process as the DCS chip and also contains the TMR mechanism.

3 Current prototypes

Currently there are prototypes of three components of the DCS being analyzed. The DCS chip's and DCS controller's digital blocks were synthesized into two individual cores. Furthermore a

[6] Single Event Upsets

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custom made chip containing a physical layer, amongst others, was produced. In the digital chips all registers are designed with TMR and although the prototypes do not contain all features, a complete communication chain can be established.

The current prototype of the DCS chip is manufactured in the 130 nm process mentioned above and currently under investigation. It contains a digital core which works as a slave to the DCS controller prototype and an I2C-HC encoder. Communication with the prototype via I2C-HC is single ended due to the missing analog blocks in the chip. To transmit data differentially further hardware is necessary. The digital core of the prototype has all necessary digital I/O ports to simulate the read out of the proposed ADC mentioned in section 2.1.1. It also has three digital outputs to simulate the switching of modules and two 16 bit counters for the capacitive humidity measurements.

Tests have shown that the DCS chip prototype works. Stable communication can be established and all built in components behave as expected with a data rate up to 250 kbaud. The DCS chip prototype was submitted in June 2010 and is being tested since its delivery in November 2011.

The current prototype of the DCS controller is also manufactured in 130 nm and being tested with the other prototypes. It contains the crucial components to create a working DCS network which are a CAN node, an I2C-HC master and a bridge module to connect both of them. Together with the DCS chip prototype mentioned above it was possible to assemble a complete read out chain. The DCS controller prototype was submitted and delivered together with the DCS chip prototype.

The third prototype which is currently being tested is an custom made design called PhysLay that contains as its main component a physical layer for the differential communication of the DCS chip and DCS controller prototypes. In later submissions this physical layer shall be implemented into all chips of the DCS network. Besides that the PhysLay chip contains a DAC in form of a 4-bit R-2R network and two clock generators.

The Physical Layer part is made up of three components: To interpret the voltages on the differential lines, a differential amplifier was designed. A Schmitt-Trigger, connected to the output of the amplifier, generates steeper edges. The third component is the signal driver which transmits the data to the differential bus. To create a differential bus that allows multiple peers with bidirectional data transfer the physical layer for the DCS network was inspired by the CAN bus. This bus has the advantage of having a dominant and a recessive state which meets the given requirements. To have a threshold different from 0 V, the differential amplifier was designed with an offset of 100 mV. In the dominant state the driver circuit in the physical layer creates a voltage of 300 mV on the differential lines. In the recessive state the driver output is in a high impedance state and the termination resistors at the ends of the bus lines cancel any voltage on the differential lines out to 0 V. So the receiver threshold of 100 mV is in the lower third of those two states.

In first tests the signal transmission and receiving over short distances worked reliably with a transmission rate up to 1 Mbaud. The prototype was also operated together with the DCS chip and DCS controller and a complete branch of the DCS network was assembled. The communication worked stable with the proposed data rate of 250 kbaud over 10 m cable length.

There are two different clock generator circuits implemented in the chip to analyze the circuits oscillating behavior and power consumption. Both circuits contain an inverter and a Schmitt-Trigger, with the only difference in the fan out of the inverter. Initial tests with quartz oscillators

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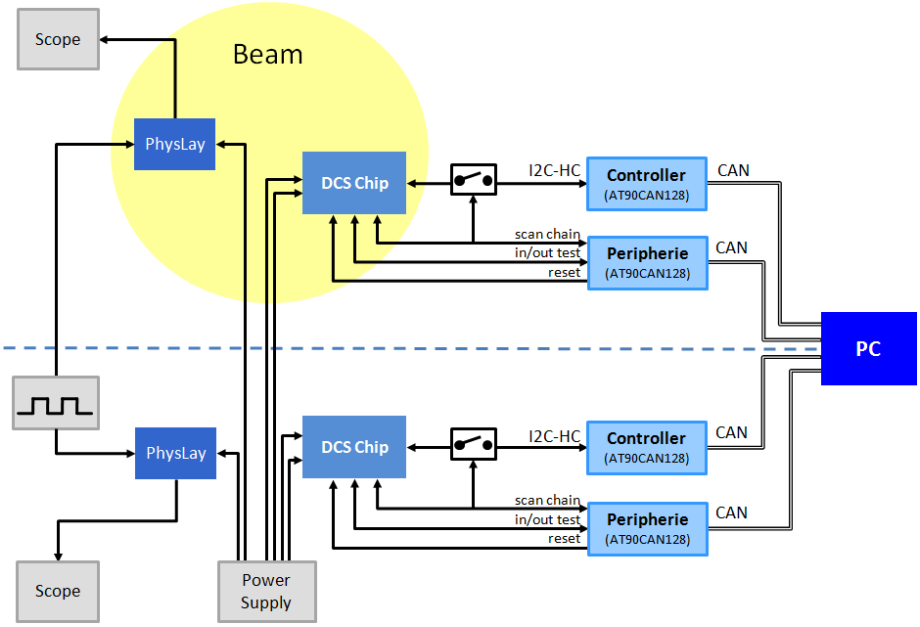

Figure 2. Sketch of the irradiation assembly of the DCS chip and the PhysLay chip.

of 4 MHz showed that the concept is working on both circuits, but the oscillation buildup and the power consumption have yet to be studied.

The R-2R network is made up of resistors of 5 kΩ and 10 kΩ and is used to determine whether this technology is suited to generate analog voltages for the ADC in the DCS chip. In this prototype the R-2R network generated analog voltages according to the voltage pattern at the inputs with deviations below 1%. This requires some improvement.

The PhysLay chip was submitted in November 2010 in 130 nm process and is being tested since its arrival in April 2011.

4 Irradiation tests

To test the reliability of the prototypes under similar conditions as in the future detector the DCS chip and the PhysLay chip were subject to an irradiation test at the Paul-Scherrer-Institute (PSI) in Villigen, Switzerland. The Proton Irradiation Facility (PIF) at PSI allows studies on a beam of 100 MeV protons with fluxes up to $5 \cdot 10^8 \frac{\mathrm{p}}{\mathrm{cm}^2 \cdot \mathrm{s}}$. To study the effects of the radiation on the operation of the chips such as single event upsets (SEU) all chips were operated and their operation and power consumption were monitored during the whole irradiation. As seen in figure 2 each irradiated chip has a reference chip to exclude impact of the environment at the PIF onto the measurements. Several chips were irradiated in runs of 1 h length and fluxes between $1 \cdot 10^6 \frac{\mathrm{p}}{\mathrm{cm}^2 \cdot \mathrm{s}}$ and $5 \cdot 10^8 \frac{\mathrm{p}}{\mathrm{cm}^2 \cdot \mathrm{s}}$.

4.1 Irradiation of the DCS chip

In the irradiation of the DCS chip communication to the DCS chip was managed by a micro controller instead of the DCS controller. To recheck the set of outputs and to vary the states of the

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inputs of the DCS chip a second micro controller was used (see figure 2). Both these controllers were connected to a read out PC by CAN buses.

For the measurement process a Lab-View software was designed to interpret scripts containing commands for all read and write functions of the DCS chip. These scripts are executed in parallel for each DCS chip so that reference chip and irradiated chip execute the same commands. After a script is processed its execution is restarted. During the irradiation two measurement methods were used: Monitoring of DCS communication and scan chain measurements. In the normal operation measurement the DCS chip was operated as foreseen in the DCS network. For realistic operation commands that read out or set the IO ports of the DCS chip change their values frequently. After the execution of each command the error counters of the chips are read out to check for false communication. In the scan chain method all registers of the chip are connected to one shift register. During the execution of the measurement script all registers of the chip are filled with zeros and after a delay of a few seconds read out via the scan chain. With this method the cross section of SEU in the chip can be measured before the TMR mechanism re-corrects them.

Overall three DCS chips were irradiated with doses up to $6.37 \cdot 10^5$ Rad. During all measurements of normal operation not one error or falsified measurement was observed which means that all inputs and outputs were read out and set correctly, and all data transfer from and to the chip was without errors.

With the scan chain method several SEUs were detected but fewer than expected for the highest flux of $5 \cdot 10^8 \frac{\mathrm{p}}{\mathrm{cm}^2 \cdot \mathrm{s}}$ (see cross section for similar proton energies in [6]). Taking the number of SEUs and the chip size a cross section for SEUs in the used 130 nm process can be estimated to a value between $1.0 \cdot 10^{-14} \frac{\mathrm{cm}^2}{\mathrm{bit}}$ and $6.6 \cdot 10^{-14} \frac{\mathrm{cm}^2}{\mathrm{bit}}$.

4.2 Irradiation of the PhysLay chip

In this test the focus was on the irradiation effect on the steepness of the edges the chip produces and thus their alteration during the irradiation was measured. Therefore the physical layer was supplied with a square pulse of $1\,\mu$s width on its input and the differential lines were connected to a short twisted pair line between the termination resistors. This pulse leads to an increase of the voltage level between the differential lines of the chip. As soon as the differential lines have a level difference ≥ 100 mV the output of the physical layer changes to the high level with a delay of the signal's run time in the chip. During the measurement high speed oscilloscopes were used to sample the input, the output and the differential lines of the reference chip and the irradiated chip (see figure 3). The oscilloscope screens were saved once every minute.

During all runs the rise and fall times remained constant within measurement errors. The same applies to the voltage difference of the differential lines and the amplitude of the output signal of the physical layer. The only change that could be observed was a decrease in the signal delays especially between the input and the output of the physical layer. Though the effect of these delay variations can only be seen in the latter runs with high fluxes. The origin of these effects has yet to be determined.

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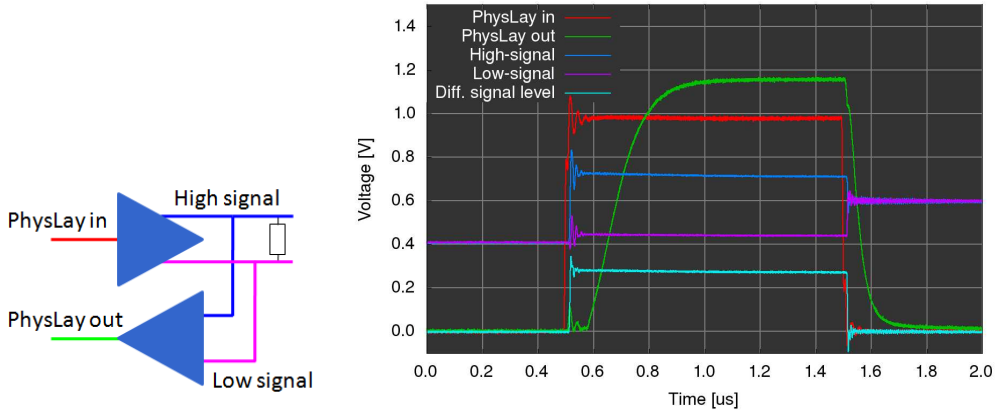

Figure 3. Sketch and measured signals of the physical layer with an input signal of a 1μs square pulse. The measured signals are: Input pulse (red), read back output of the physical layer (green), differential lines (blue and purple) and the voltage difference between the differential lines (light blue, calculated by the oscilloscope).

5 Summary and outlook

The new ATLAS pixel detector at the HL-LHC requires a new detector control system. In the University of Wuppertal a DCS concept with three independent paths (safety, control & feedback and diagnostics) is under development. To minimize material cost inside the detector, the control & feedback path consisting of the DCS network is being realized in the smallest form-factor available, ASIC chips manufactured in a 130 nm process. These ASIC chips (DCS chip and DCS controller) span a network that monitored and steers certain quantities inside the detector. With prototypes of these chips a DCS network was tested successfully in our labs. To ensure reliable operation in the radiation exposed environment of the ATLAS pixel detector, prototypes of the DCS chip and the network's physical layer have been tested under irradiation at the PSI. All tested chips passed the irradiation.

Further irradiation tests for the DCS controller are scheduled as well as new prototype ASICs containing components for analog circuits of the DCS network.

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