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Prototypes for components of a control system for the ATLAS pixel detector at the HL-LHC

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ABSTRACT: In the years around 2020 an upgrade of the LHC to the HL-LHC is scheduled, which will increase the accelerators luminosity by a factor of 10. In the context of this upgrade, the inner detector of the ATLAS experiment will be replaced entirely including the pixel detector. This new pixel detector requires a specific control system which complies with the strict requirements in terms of radiation hardness, material budget and space for the electronics in the ATLAS experiment. The University of Wuppertal is developing a concept for a DCS (Detector Control System) network consisting of two kinds of ASICs. The first ASIC is the DCS Chip which is located on the pixel detector, very close to the interaction point. The second ASIC is the DCS Controller which is controlling 4x4 DCS Chips from the outer regions of ATLAS via differential data lines. Both ASICs are manufactured in 130 nm deep sub micron technology. We present results from measurements from new prototypes of components for the DCS network.

KEYWORDS: Analogue electronic circuits; Radiation-hard electronics; Detector control systems (detector and experiment monitoring and slow-control systems, architecture, hardware, algorithms, databases); Digital electronic circuits

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1 Introduction

Along with the Luminosity upgrade of the LHC to the HL-LHC, the entire inner detector of the ATLAS experiment will be replaced to cope with the increased radiation levels and to provide better resolution in vertex finding. The innermost part of the inner tracker (ITK) will be a new PIXEL detector. This detector will most likely consist in the central part of four barrel shaped layers and six disks on each side. The detector will cover a pseudo rapidity up to $\eta = 2.5$. The base unit of the disks and the outer barrel section consists of a sensor chip with pixel cells of $(50 \times 250)\,\mu\mathrm{m}^2$, bump bonded to front end read out chips. For the inner barrel layers sensor chips with pixel cells of $(25 \times 150)\,\mu\mathrm{m}^2$ are forseen. In the barrel section these modules are mounted on support structures, so called staves, which include a cooling pipe and are installed in parallel to the beam pipe. At the end of each stave an End-Of-Stave (EoS) card houses the power supply and the connection to the optical read out. Being the detector closest to the interaction point, the PIXEL detector has to withstand the highest levels of radiation in ATLAS. Simulations have shown, that a fluence of up to $2 \cdot 10^{16}\,\mathrm{cm}^{-2}$ of hadrons with energies $> 20\,\mathrm{MeV}$ have to be expected for the PIXEL detector for a scheduled integrated luminosity of $3000\,\mathrm{fb}^{-1}$ [1]. Assuming a luminosity of $\mathscr{L} = 5 \cdot 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ this yields an average flux of $\phi = 3.3 \cdot 10^{8}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ of hadrons with energies $> 20\,\mathrm{MeV}$. During the operation of the experiment the ATLAS detector can not be accessed for a long period of time, hence the PIXEL detector has to be controlled entirely from the outside of

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Component	Monitored values		Controlled values
Modules	HV	Current & Voltage	Voltage setting & On/Off
	LV	Current & Voltage^m	Voltage setting & On/Off^s
	Temperature^m		
End of Stave Cards	Current & Voltage^m		Voltage setting & On/Off
	Temperature^m		
			Reset^s
On detector Opto transceiver	Current & Voltage^m		Voltage setting & On/Off
	Temperature^m		
			Reset^s
Environment & Cooling	Humidity^m		
	Temperature^m		

Table 1. Table of DCS values that are relevant for save detector operation. The table shows which values have to be monitored and/or which values have to be steered. (^{m}: monitored by DCS chip, ^{s}: steered by DCS chip.)

the detector. To ensure a reliable and stable operation of the PIXEL detector, a detector control system (DCS) is needed, that monitors and steers all the environmental conditions listed in table 1. For all these quantities, the severity, availability, granularity and location of processing have to be defined. The powering scheme of the PIXEL modules has not yet been defined. Options are serial and parallel powering. The latter is based on the usage of DC-DC converters. The control system will have to be able to handle both options. An additional requirement on the control system is the minimization of the material budget (cables, components) within the detector volume, in order to reduce the impact on the data to a minimum. The control system has to be operational even if the cooling of the detector fails, which makes low power consumption essential to prevent overheating of the detector. Being located as close to the interaction point as the PIXEL electronics, the control system has to withstand the same radiation levels.

2 DCS concept

The DCS is split into three parts, each with a separate signal path. The safety path forms a hard wired interlock system, that has the ability to switch of parts of the detector, if the environmental conditions exceed certain threshold values and a safe operation of the detector can no longer be guaranteed. This system has the highest reliability, but, due to required material budget, the lowest granularity (half stave). It is always in operation, even if the detector is switched off. The safety path is not directly controllable by the control room operator, since access to the DCS crates would be required.

The second part is the control and feedback path. This path is the interface of the operator to the detector, handling the control room use cases like calibration, connectivity tests and data taking. It steers and monitors the detector modules, EoS-Cards and the optical interfaces. It is made up by the DCS network which is described in the next section. The operation of the control and feedback path is mandatory for the operation of the detector. Although this path is not hardwired it is still designed for high reliability. It has its own lines for powering and data transmission, making it independent of the detectors power supply and data read out. The granularity is higher compared

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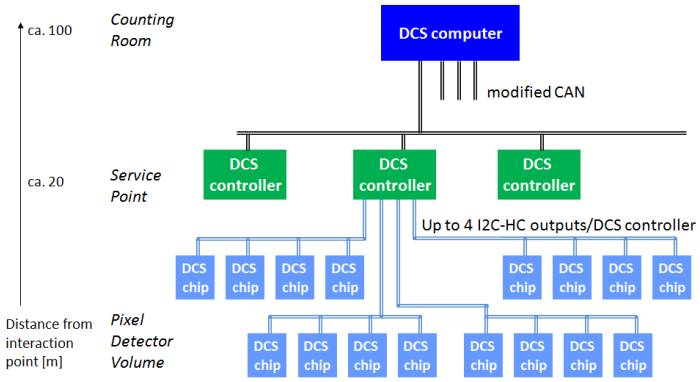

Figure 1. Schematic of the DCS Network.

the safety path (per module or half stave), due to local processing of measurements and steering inside the detector.

The third part is the diagnostics path. This path is included into the optical detector read out and therefore only available when no physics data are taken. A very high granularity (per front end chip) is achieved, without additional material, by embedding the data read out into the optical link.

2.1 DCS network

The DCS network forms a network, as depicted in figure 1, with two types of nodes and two types of buses. The first node is the DCS controller located in a service point in the outer regions of the ATLAS detector ($\sim 20\,$m from the interaction point). It is connected to the DCS computers in the counting room via a CAN[1] bus over a distance of $\sim 80\,$m. The second node, the DCS chip, is located on the EoS-Cards ($\sim 1\,$m from the interaction point). DCS chip and DCS controller are connected by the I2C-HC bus, an extended I^2C [3] protocol with additional four check bits in each message forming a (12,8) Hamming code [4]. This protocol is able to detect messages with up to two false bits and correct messages with one erroneous bit. Each I2C-HC bus will host four DCS chips and four I2C-HC buses will be connected to a DCS controller, resulting in one DCS controller per 16 DCS chips. This distribution of lines is a compromise between the number of required cables and the loss of detector channels in case of a cable failure. Both buses, I2C-HC and CAN are transmitted differentially leading to four lines for each I2C-HC bus and two lines for each CAN bus.

To enhance the reliability of the network, all nodes have their own lines for power and data, as mentioned above. Most of the processing of data is done outside of the experiment cavern. This simplifies the chips and reduces significantly bit flips due to the radiation. The nodes are designed as ASICs, as this results in the smallest available form factor and the highest tolerance against radiation effects.

[1] Controller Area Network [2]

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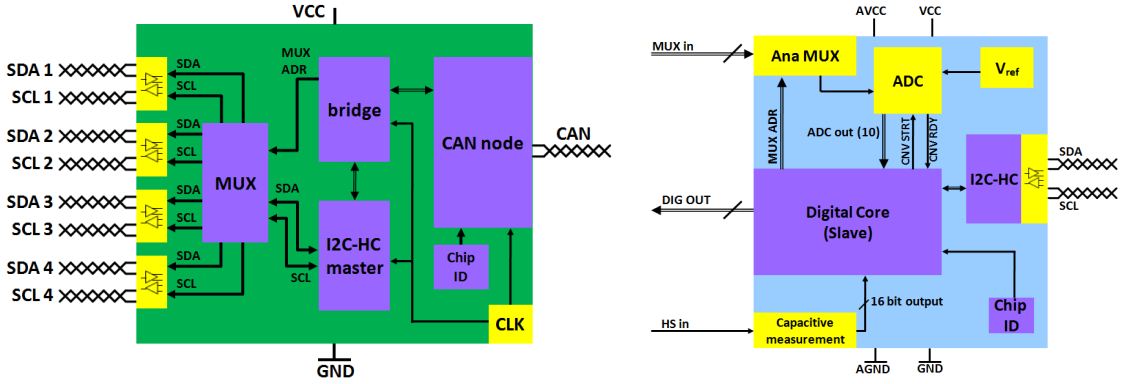

Figure 2. Sketch of the components of the DCS controller (left) and the DCS chip (right)

2.1.1 DCS controller

The DCS controller, which is diagrammed in figure 2 (left), builds the bridge between the two network protocols in the DCS network. Therefore it contains the logic for a CAN node and an I2C-HC master. A multiplexer is included as well, that connects the I2C-HC master to one of the four I2C-HC buses. In addition a clock generator is necessary for the CAN node. For the differential transmission over the I2C-HC bus, the DCS controller holds a physical layer for both bus lines SDA and SCL on each output of the multiplexer, resulting in 8 differential ports.

As the DCS controller is located inside of ATLAS, it has to be tolerant against the radiation levels inside the detector. Although the radiation levels at the location of the DCS controller are not as high as on the EoS-Card close to the interaction point, the DCS controller has the same protection mechanisms against radiation as the DCS chip (see next section).

2.1.2 DCS chip

The DCS chip, diagrammed in figure 2 (right), receives commands from the DCS controller via the I2C-HC bus. These commands trigger the measurement of the environmental conditions and switching or resetting of detector modules and the optical link. For the measurement of temperatures (via NTCs) and voltages the DCS chip is equipped with a 10 bit ADC and a 16 channel analog multiplexer. To measure the humidity in the detector, it includes two circuits for capacitance measurements. The resetting and switching of detector modules and the optical link is done by the digital outputs of the DCS chip. No clock generator is integrated into the DCS chip, in order to minimize the power consumption. The clock for the ADC and the digital core are provided by the SCL line of the I2C-HC bus, which limits the sampling rate of the ADC to 5 kHz to 10 kHz. Switching and resetting components during the operation of the detector is a very critical process, since this can damage parts of the detector. Therefore the chip has to work extremely reliable in the in the high radiation levels and particle flux so close to the interaction point. Therefore it has to be radiation hard and hardened against single event upsets (SEU). To achieve the necessary tolerance, the chip is manufactured in a 130 nm process, which is known to be very radiation hard. In addition every register in the chip logic is made up with triple modular redundancy (TMR). This means, that every register in the chip has two clones and a majority voter. In case of a bit flip in the chip the

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majority voter writes the the unchanged value of the two redundant registers back into the flipped one. The clock for the voter logic is generated by the delayed rising edge of the error signal.

3 Prototypes

Currently there are prototypes of three chips, one analog and two synthesized designs. All of these chips are manufactured in a commercial 130 nm process. The synthesized digital designs contain logic parts of the DCS controller and DCS chip and the analog design contains a physical layer for the I2C-HC bus. Although the prototypes of the DCS chip and controller do not contain all features, a complete communications chain could be set up.

3.1 CoFee 1

The CoFee 1 chip is the first prototype of a DCS chip and contains the logic for a node for the I2C-HC bus and for the control of an ADC and digital outputs, as described in section 2.1.2. All registers in the chip have TMR. Further information on the layout and the tests of the DCS chip prototype can be found in [6].

3.2 CoFee 2

The second chip, the CoFee 2, is the prototype of the DCS controller. This chip contains the CAN node, the bridge and the I2C-HC master which are the obligatory circuits to create a communication chain of the DCS network. Again this design has no analog blocks and so all data bus lines are single ended and the clock has to be generated externally. To verify the TMR implementation and the SEU rates during irradiation, this chip was produced in two versions: one with TMR and one without. Because of the increased amount of logic in the TMR version of the chip, its foot print is with $1.7 \times 1.7\text{mm}^2$ larger than the one of the non TMR chip, which is $1 \times 1\,\text{mm}^2$.

3.3 Physical Layer

The Physical Layer chip contains, amongst others, a differential line transceiver for the I2C-HC bus. This transceiver was designed to create a bidirectional bus with a dominant and a recessive state, so that the nodes on the bus cannot be destroyed by erroneous bus states. For details about the Physical Layer chip, please refer to [6].

4 Tests with prototypes

All of the prototypes mentioned above have been or are currently being tested individually and in combination with each other. Besides the tests in our laboratory, also irradiation tests have been performed. The chips were irradiated with 100 MeV protons at the Proton Irradiation Facility (PIF) at the Paul Scherrer Institute (PSI) in Switzerland. The PIF provides fluxes up to $4.25 \cdot 10^9\,\text{cm}^{-2}\text{s}^{-1}$ for the 100 MeV protons. The expected flux of hadrons with energies $\geq 20\,\text{MeV}$, in the proximity of the beam pipe is $3.3 \cdot 10^8\,\text{cm}^{-2}\text{s}^{-1}$. Hence the beam provided by the PIF is well suited to simulate the conditions in the ATLAS PIXEL detector during operation of the LHC.

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4.1 Dry runs in the lab

All prototype chips are tested individually after their delivery from the manufacturer. In these tests the basic functionality and long term stability of operation is tested under laboratory conditions. These tests were passed by all of the prototypes described above, except for the TMR version of the CoFee 2 chip. In this chip the transmission of CAN messages does not work correctly, so only writing commands can be executed by the DCS controller. Modifications of the supply voltage for the chip improved the error rate of the chip but could not fully recover stable operation. The source of these errors could be traced to an issue in the clock tree definition during the chip synthesis. The non-TMR version of the CoFee 2 chip has shown to have the same issue but due to the smaller design this had no effect on the stable operation.

A complete read out chain of the DCS network has been set up with the prototype chips: from the DCS computer over the DCS controller (CoFee 2 without TMR) and the Physical Layer (for differential transmission of the I2C-HC bus) to the DCS chip (CoFee 1) . The differential transmission of the I2C-HC bus was tested for different bus frequencies and cable lengths. At 100 kHz the bus worked reliably up to the maximal used cable length of 170 m. 200 kHz stable communication could be established up to cable lengths of 80 m. As the distance between the two chips (DCS controller and DCS chip) is around 20 m these results are more than sufficient.

4.2 Irradiation 2011

In an irradiation campaign in summer 2011 the CoFee 1 chip and the Physical Layer chip were irradiated. Both chips were operated and monitored during the irradiation. During the whole campaign the functionality of the chips was not affected by the beam. For details about the irradiation campaign in 2011, please refer to [6].

4.3 Irradiation 2012

In the irradiation campaign in summer 2012 the CoFee 2 chips and a chip with a shift register with 1500 cells were irradiated. As a reference a second identical setup was operated outside of the radiation area (see figure 3).

To increase the number of irradiated flip flops, four of the shift register chips were mounted on a carrier PCB in a 2×2 arrangement. This assembly provides 6000 flip flops in the beam, which were read out and filled with a ..0011.. bit pattern every one (higher fluxes) to two (lower fluxes) minutes. The energy and the flux of the beam were varied between 30.74 MeV to 99.7 MeV and $1 \cdot 10^8\,\mathrm{cm^{-2}s^{-1}}$ and $1 \cdot 10^9\,\mathrm{cm^{-2}s^{-1}}$, respectively. The results of these measurements can be seen in figure 4. In the left hand plot one can see that the number of SEUs in the chip rises with the amount of the radiation the chip is exposed to. The systematic uncertainty of the fluence has been estimated to $\sim 20\%$ and is assumed to originate from saturation effects in the ionization chambers measuring the beam flux. The impact of the fluence uncertainty to the number of bit errors was also taken into account for fitting the cross section. As the right hand plot shows, the cross section of SEUs is independent of the proton energy in the measured range. This agrees with previous measurements [7]. With this assumption, the cross section of SEUs in D-flip-flops from the CERN design kit [8] for the 130 nm process has been determined to $\sigma = (5.11 \pm 0.91) \cdot 10^{-14}\,\mathrm{cm^2 bit^{-1}}$ for a homogenous distribution of logical 1 and 0 in the registers. This value can be split into the

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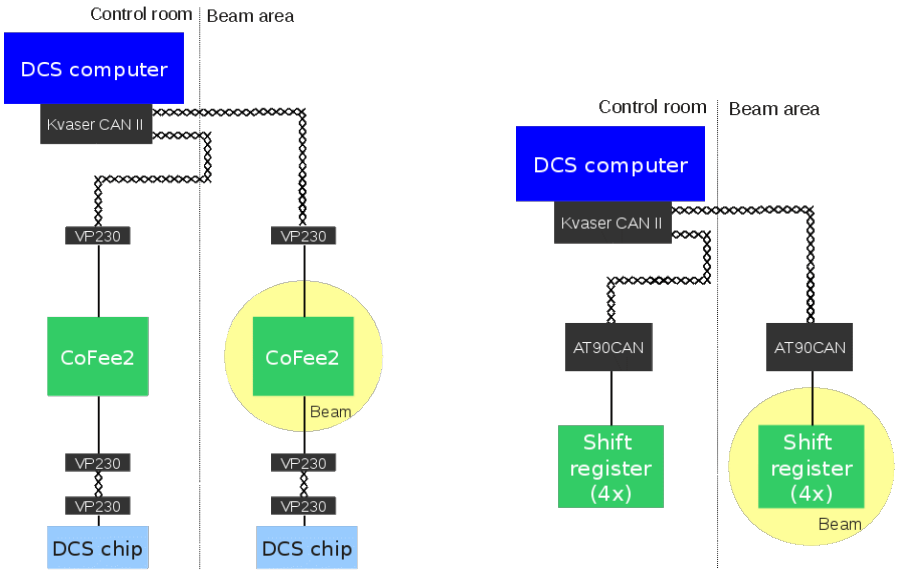

Figure 3. Schematics of the irradiation setups including the reference setup from the irradiation measurements in 2012 at PSI. The black boxes (Kvaser CAN II, VP230 and AT90CAN) are commercial parts to allow operation of the irradiated chips via CAN bus.

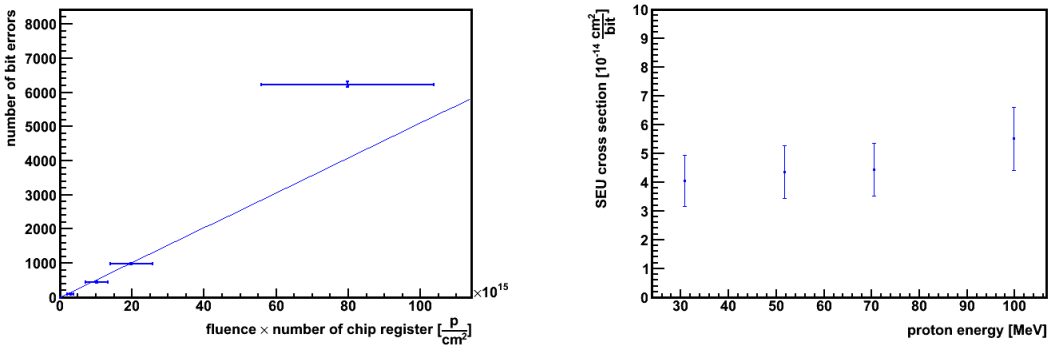

Figure 4. Results from the irradiation measurements with the shift register. The upper plot shows the number of SEUs depending on the fluence with the fitted gradient that gives the cross section and the lower plot shows the cross section of SEUs depending of the proton energy.

cross section for bit flips from 0 to 1 ($\sigma_{0->1} = (3.23 \pm 0.36) \cdot 10^{-14}\,\mathrm{cm^2 bit^{-1}}$) and bit flips from 1 to 0 ($\sigma_{1->0} = (7.26 \pm 0.38) \cdot 10^{-14}\,\mathrm{cm^2 bit^{-1}}$).

The two versions of the CoFee 2 chip were irradiated with fluxes between $5 \cdot 10^8\,\mathrm{cm^{-2} s^{-1}}$ and $4.25 \cdot 10^9\,\mathrm{cm^{-2} s^{-1}}$. Even though these fluxes are much higher than the expected fluxes in the regions where the DCS Controller is located, they were chosen to verify the implementation of the TMR in the chip's logic and to obtain a statistically significant result. During the irradiation time of 4 h each, the chip without TMR was operated normally, whilst the chip with TMR could only receive messages, as described above. During the irradiation, 68 bit flips were observed in the

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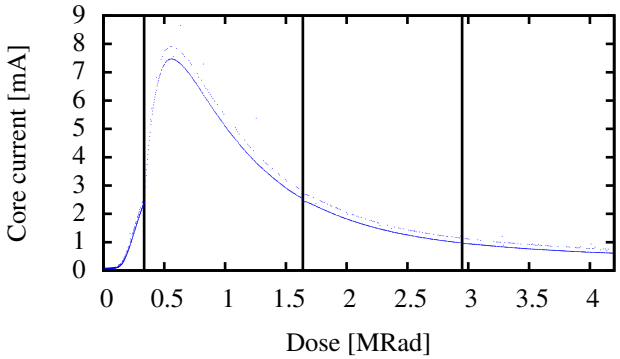

Figure 5. Current consumption of a CoFee 2 core with TMR during irradiation. The plot is a combination of four runs of 1 h each. Between the runs the beam was switched off for some minutes. The changes of the runs are indicated by the vertical lines in the plot. The second thin line above the data points originate from an alias effect between the change of the operation mode of the chip and the measurement frequencies.

CoFee 2 without TMR, of which six lead to a hang up of the chip.[2] Thus mechanisms like TMR are essential for stable and reliable operation of the DCS. The chip with TMR showed no errors in the execution of the transmitted commands. In order to compare the two chips directly, an additional run of 1 h was started for the chip without TMR operating it in the same way as the chip with TMR. Four SEU events were observed during this time.

During the whole irradiation period the power consumption of the chips was monitored. For each chip the core current was measured. The plot in figure 5 shows a combination of four runs for the CoFee 2. The power consumption first rises very steeply up to $\sim$8 mW, and peaks at $\sim$ 0.56 MRad. Then it falls slowly to less than 1 mW. This behavior originates from two competing effects [9]. First charge is trapped in the STI[3] and creates additional parasitic channels in the MOSFETs.[4] These additional channels allow more current to flow through the transistor and the power consumption rises. At higher doses, free charge carriers in the interfaces of the STI recombine, cutting of the parasitic channels. Thus the parasitic current drops and so does the power consumption. These effects can cause peaks in the power consumption of the detector, if they occur at the same time in many chips. As the power consumption rises with the radiation dose in the electronics, this is very likely with the homogenous radiation exposure in the ATLAS PIXEL detector.

5 Summary and outlook

The university of Wuppertal is designing a new detector control system for the new ATLAS PIXEL detector, which will be required for the operation at the HL-LHC. The concept of this new DCS foresees a splitting into three parts (safety, control & feedback and diagnostics). The control & feedback path, which consists of the DCS network, is realized with ASICs in a 130 nm process. These ASICs measure the necessary values in situ to reduce the material budged of the DCS sys-

[2] The impact of the clock distribution problem in the chip without TMR could be excluded by verifying the measured SEU rate with the expected SEU rate (measured with the shift register).

[3] Shallow Trench Isolation

[4] Metal Oxide Semiconductor Field Effect Transistor

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tem. Prototypes of the ASICs have been used to set up a working DCS network in the laboratory. Irradiation tests have been performed at the PSI in order to determine the reliability of the chips at high particle flux. The SEU cross section has been determined, for the used design kit, to $\sigma = (5.11 \pm 0.91) \cdot 10^{-14}\,\mathrm{cm}^2\mathrm{bit}^{-1}$. The chips equipped with triple redundant registers (TMR) have been tested successfully up to particle rates of $4.25 \cdot 10^9\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$, which is about 10 times as high as espected at the HL-LHC. The measured SEU cross section yields a double bit flip probability for the DCS controller of $P_{\not z\,TMR} = 0.068$ for 10 years of operation at the HL-LHC. A double bit flip could cause a failure of the TMR equipped DCS controller. Further irradiation measurements have to verify this calculation. For the final versions of the chips, irradiation tests for long term aging of the integrated circuits, have to be performed. In these tests the reliability of the detector control system with respect to the radiation doses occuring, in the runtime of the experiment (up to 1.5 GRad [10]), have to be verified.

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