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Index Terms— Static Random Access Memory (SRAM), Single Event Upset (SEU), Tungsten, Proton, Large Hadron Collider (LHC), European Organization for Nuclear Research (CERN).

I. INTRODUCTION

THE Large Hadron Collider (LHC) at the European Organization for Nuclear Research (CERN) is controlled by numerous partly- or full-custom electronic systems which ensure its function and protection. These systems are mostly based on Commercial-Off-The-Shelf (COTS) components.

A new power converter control system (FGClite) [1] currently under construction will be one of the highly distributed systems used to control the accelerator. The FGClite will be exposed to a complex mixed-field radiation environment, composed of particles (mostly hadrons) originated from the interaction of the accelerated particles with the accelerator elements with energies extending up to several GeV [2]-[4]. From the system reliability standpoint, it is extremely important to be able to assess the error rate variations of the individual components used, as well as the full FGClite system, in particle energy ranges representative to the final operating environment. For the majority of components, error rates tend to saturate in the range of several

tens to several hundreds of MeV and most radiation facilities allow experimental characterizations to be performed up to these energies. On the other hand, some components have been reported to have cross-sections which do not saturate in this range [5]. The impact of this increase on a total system error rate can be significant in environments for which the particle fluxes above several hundreds of MeV are not negligible as it is the case for avionic/stratospheric altitudes or a particle accelerator such as the LHC. Thus, safety margins have to be applied to the test data to account for this increase. A general study and an analysis of the environment impact on error rate are presented in [6].

This work presents a 16Mbit Static Random Access Memory (SRAM) from Renesas Electronic Corp., which was selected as the central memory for the storage of critical system data in the FGClite system. The interest in this component comes from its known immunity to Single Event Latch-up (SEL) and an alpha/neutron Soft Error Rate (SER) several orders of magnitude lower than standard SRAMs available on the market [7], [8].

An increasing proton Single Event Upset (SEU) cross-section as a function of energy for this memory was measured during irradiations in two facilities: PSI [9] and TRIUMF [10] up to 480MeV. Such an increase has already been shown on test structures in [11]. Ref. [5] experimentally showed the effect of particle energy on SEL cross-section in commercial SRAMs containing tungsten. A detailed SEL model and its energy dependence are discussed in [6]. This study presents a first real case example of commercially available SRAM memory showing the effect of tungsten on the proton SEU cross-section. Data presented in this work confirm previously predicted cross-section increase for memories with high critical charges shown in [12]. The underlying physical phenomena explaining the experimental data are analyzed here using Monte-Carlo simulations. The implications of this increase in a particle accelerator environment are shown to be significant for the total SEU rate to be expected during LHC operation.

This paper is organized as follows: section II presents the details concerning the device under test, section III shows the test setup and measured cross-sections in several test facilities, while section IV focuses on the proton cross-section increase as a function of energy. The last section presents the summary and future work.

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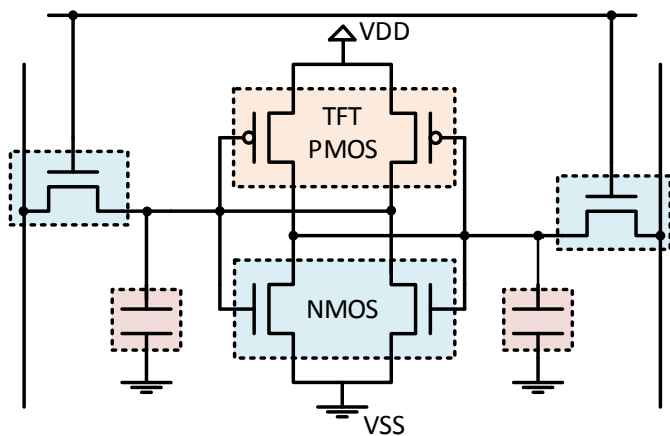


Fig. 1 The bit-cell architecture showing the N-channel MOSFETs (two pull-down transistors and two access transistors), two TFT P-channel and two DRAM capacitors connected to circuit storage nodes.

II. DEVICE DESCRIPTION

The device under study is a 150nm, 1M x 16bit low power SRAM manufactured by Renesas Electronic Corp [13]. The Back-End-Of-Line (BEOL) is composed of six poly-silicon layers, one tungsten (Metal1 or M1) and two Aluminum metallization layers (M2 and M3). The bit-cell dimensions are $1.00 \times 0.98 \mu\text{m}$ and the die dimensions of are $5.62 \times 5.84 \text{mm}$, (32.78mm^2) [14]. The chip external power supply voltage was biased at 3.3 V during all irradiations presented in this paper.

A single bit-cell is formed from Thin Film Transistor (TFT) P-channel MOSFETs stacked above N-channel MOSFETs. The physical separation of P- and N-channel transistors erases the parasitic thyristor inherent to the standard CMOS structures, thus SEL cannot occur. Each bit-cell uses two DRAM capacitors placed in the BEOL in order to decrease the memory sensitivity to Soft Errors [14]. Such technology has proven to significantly decrease alpha and neutron Soft Error Rates (SER) for CMOS SRAM technologies [15], [16]. Fig. 1 shows the schematic of the bit-cell with four NMOS transistors (two pull-down and two access transistors), two TFT pull-up PMOS transistors and two DRAM capacitors connected to the cell nodes, increasing its storage charge capacity.

III. TEST SETUP AND CROSS-SECTIONS

A. Proton irradiations

Components for radiation tests have been procured from two different lot date codes: 1328 and 1343. Several DUTs were irradiated with a mono-energetic proton beam at two different radiation facilities: 16 devices at PSI at energies equal to 60, 100 and 230MeV and 6 devices at TRIUMF at 230, 355 and 480MeV. A static test procedure was applied to avoid measuring errors from peripheral electronics (address decoder, sense amplifiers, etc.)

Fig. 2 shows the SEU proton cross-sections as a function of energy compared with irradiations performed previously by NASA at IUCF [17] in Jun 2007. Data collected at PSI/TRIUMF are fully consistent and the observed differences to measurements from [17] are most likely due to the

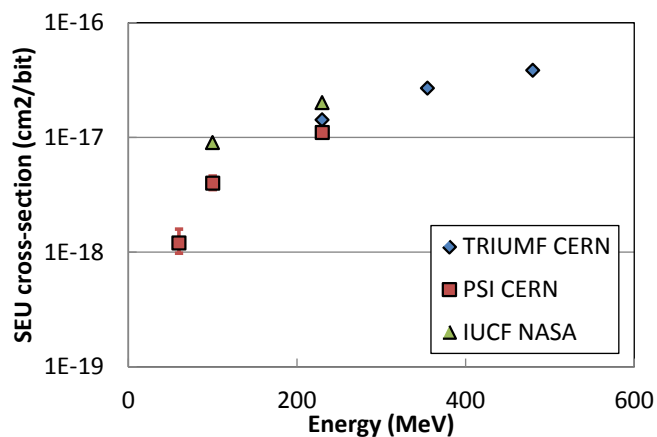


Fig. 2 Proton SEU cross-sections in cm^2/bit measured at two different test facilities: PSI (Oct 2013), TRIUMF Dec 2013 and compared to data collected by MEI Technologies/NASA at IUCF (Jun 2007) [7]. The error bars (90% confidence level) are shown only for CERN irradiations.

Energy (MeV)	60	100	230	355	480
max MBU multiplicity	1	2	4	3	4
MBU percentage	0%	3%	11%	10%	16%

Table 1 Maximum MBU multiplicity and MBU percentage as a function of proton energy for irradiations at PSI and TRIUMF.

process/component differences between 2007 and 2013. The external bias voltages during CERN and NASA irradiations are the same.

A moderate influence of the test pattern was observed within the range of $\pm 25\%$ (all '0' being the most, all '1' being the least sensitive). Noteworthy is the fact that the proton SEU cross-section does not saturate up to 480 MeV while the standard commercial CMOS SRAMs tend to saturate in the range of 50 to 100 MeV. No Single Event Latch-up was recorded. It has to be underlined that the measured proton bit-cross-section is 3 to 4 orders of magnitude lower than other standard commercial SRAMs available on the market. When combined with the immunity to SEL, this makes this component very appealing for use in radiation environments. For the SEU measurements, components were exposed multiple times to fluences equal to 10^{11} protons per cm^2 (doses between 1 and 10 krad(Si) depending on the energy). Until the Total Ionizing Dose (TID) failures above 35 krad(Si), no effect of the dose on the cross-section value was observed.

TID failures were observed for doses in the range between 35 and 55 krad(Si) – in total 11 out of 24 components failed. Above these doses, a small number of bit-cells (between 2 and 20) were stuck at previous values and could not be re-written with a new test pattern. For 74% of damaged cells, a bit was stuck to '0'; for 23% of cells, a bit was stuck to '1', for 2.5% two stuck bits were observed. This can be explained by a leakage increase of either the NMOS or PMOS transistors within the memory cell but without better technological information it is impossible to determine which transistor type is failing. Probably because of the increased leakage within the memory cell, the drive current of the access NMOS transistors is not sufficient to force the bit-cell value to a requested state.

In addition, an analysis of multiple events has been performed. As the information about the scrambling and used multiplexer scheme was not available, the correspondence

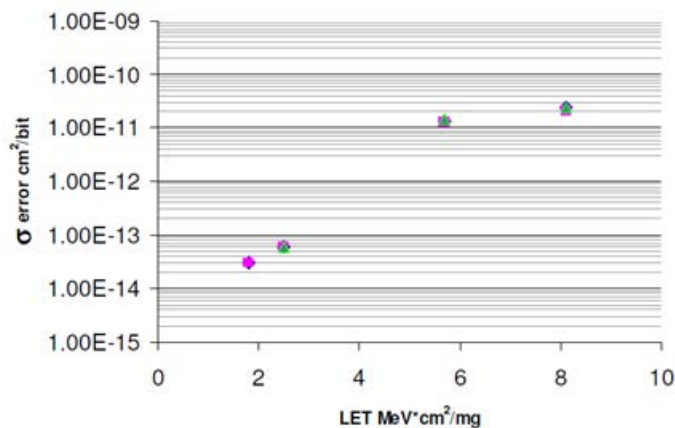


Fig. 3 Heavy ion SEU cross-section as a function of the particle LET value reported in [17].

between the logical and physical memory layout is not known. The analysis was performed for multiple errors in one logical word that will be called Multiple Bit Upsets (MBUs) [12].

Table 1 shows the percentages of MBUs among all events for different measured energies and the maximum multiplicity of events. With increasing energy, an increasing number of MBUs is observed and events affect more memory cells.

In [12], a detailed analysis of the MBU cross-section of an SRAM is discussed. For the considered bit-cell geometry, it was shown by Monte-Carlo simulations that for high Q_{crit} memories ($>20fC$), the Single Bit Upset (SBU) cross-section does not change significantly while the difference can reach one order of magnitude in MBU cross-section for components with/without tungsten.

B. Heavy Ion irradiations

Interestingly, irradiations performed by NASA with heavy ions presented in Fig. 3 [17], have shown low cross-sections for this component already for very low LET values in the range of 1 to 10 $MeV \times cm^2/mg$. When comparing this with a very low proton cross-section from Fig. 2, one can find two potential explanations:

1. The component is very sensitive (low critical charge) with a very small critical volume, having an extremely low cross-section at high energies. The increase of the proton cross-section could be explained by increasing number of secondaries created by inelastic collisions with protons, thus giving a higher probability of charge deposition in a small sensitive volume.

2. The component has a high critical charge value and high SEU cross-section onset (LET threshold) with a relatively larger sensitive volume, in which case data from TAMU should be further explained in this case.

Knowing that each bit-cell contains two DRAM capacitors that increase its critical charge, the second possibility seems to be more likely. A simple first approximation model, presented below, confirms this hypothesis. In [14], it is stated that the NMOS transistor drain dimensions are the minimum possible for 150nm CMOS technology, i.e. equal to around $0.15 \times 0.2 \mu m$ ($3.0 \times 10^{-2} \mu m^2$). Considering the heavy-ion data (Fig. 3) and the cell layout, the sensitive surface per bit-cell is equal to $2.0 \times 10^{-3} \mu m^2/bit$ for $8 MeV \times cm^2/mg$ which is 15x smaller than the drain dimension of a storage transistor. It

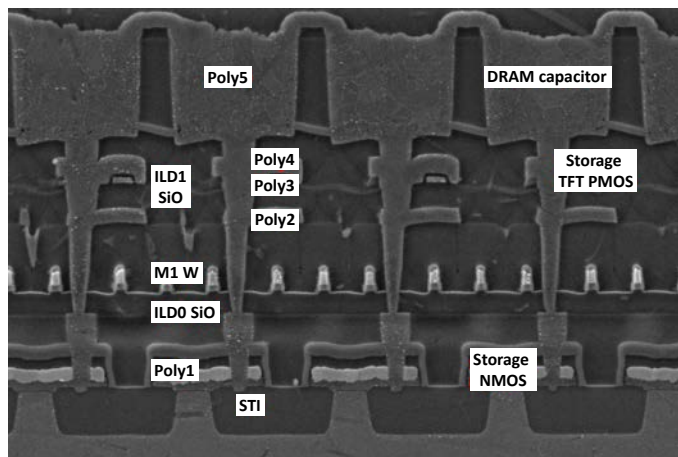


Fig. 4 Renesas memory cross-section through the metallization and active layers showing different regions.

would mean that a direct off-state drain ion strike does not cause a bit-flip and the reported SEUs in Fig. 3 account for events due to nuclear inelastic interactions of heavy ions with the component materials. Similar data have been reported in [18]-[19]. In addition, if the heavy ion LET threshold value would be as low as $2 MeV \times cm^2/mg$ and we would consider the saturation of the heavy-ion SEU cross-section being at $6-8 MeV \times cm^2/mg$ and the proton SEU cross-section would saturate already at 50 MeV.

IV. PROTON SEU CROSS-SECTION INCREASE

A. BEOL analysis

A potential explanation for the proton cross-section increase above 100MeV is thus the contribution of high LET secondary heavy ions being produced by the incoming beam from the BEOL metals. Fig. 4 shows a cross-section through the metallization and active layers that was obtained from an analysis of the Renesas component. It was discovered that the Renesas technology uses a relatively large volume of tungsten: 1) the M1 metal layer is made out of tungsten (58%) with top and bottom planes made out of titanium (42%), 2) the vias between metal lines are TiW plugs and 3) The Poly1 polysilicon lines are covered with SiW silicide to increase their conductivity. When considering tungsten, the proton-induced fission reaction cross-section increases by up to a factor of over a factor 100 between 100 MeV and the saturation value reached at $\sim 3GeV$ according to FLUKA simulations [6]. The highest LET of the simulated fission fragment with FLUKA was equal to $37 MeV \times cm^2/mg$. This enhancement can contribute to the increase of the proton cross-section above 100MeV shown in Fig. 2.

B. FLUKA simulation

1) Simulation setup

The FLUKA Monte-Carlo simulation code described in detail in [20]-[22] was used to model experimental proton cross-sections.

The code reproduces the experimental beam conditions (particle type, particle energy and incidence). To a first approximation a simple Rectangular Parallelepiped (RPP) model is used for the energy deposition. The dimensions of this sensitive RPP volume were chosen in the following way:

x/y dimensions are equal to 0.35/0.45 μm ($\sim 2\times$ transistor drain dimensions) and the depth is equal to 0.4 μm knowing that a special shallow well geometry is used by Renesas to decrease the collection of charges [23]. These dimensions are in agreement with values reported in [24] for similar technologies. The real depth of the BEOL is taken into account. The composition of the BEOL was simplified to only include silicon dioxide and tungsten. A tungsten layer is modeled in place of the M1 metal layer and its depth is equal to 170nm and is equal to the depth of M1 metal layer added to the tungsten Silicide placed on active silicon/poly-silicon regions. The modelling of vias is omitted in this first approximation. Provided that the tungsten fragments have ranges of 10-20 μm in average, all fragments can reach the SV [6].

The next step in the modelling process requires determining the correct critical charge value, for which:

1. 10fC were attributed to an usual critical charge of an SRAM bit-cell
2. 16fC were attributed to higher capacitance of multiple poly-silicon layers used in the memory cell to interconnect devices between active silicon and TFT PMOS transistors on the Poly3/Poly4 level
3. 40fC were attributed to the additional DRAM capacitor manufactured on the Poly5 level. This charge corresponds to the 20fF of capacitance charged with the chip core voltage to 2V. This value is comparable to the eDRAM capacitor manufactured in the 130nm technology.

Table 2 compares values between different SRAM technologies and their critical charges for standard SRAM and additional DRAM capacitors. The estimated value of 66fC compares well with other technologies.

As the tungsten fission cross-section increases significantly as a function of energy above 100MeV, the fitting of the critical charge was performed at the lowest measured energy of 60MeV for which the tungsten contribution is assumed to be insignificant. At this energy, the simulated cross-section is equal 1.67×10^{-18} cm^2/bit for structure without tungsten layer and 1.93×10^{-18} cm^2/bit for structure with tungsten which gives 16% of total contribution in the cross-section due to tungsten recoils.

Ref.	Manuf/Techno/cell area	Architecture	Capacitor (fF)	Voltage (V)	Stored charge (fC)	
					Cell	Capacitor
[15]	STM /90nm /0.99 μm^2	eDRAM	10-14	1.2	N.D.	14-17
[15]	STM /130nm /2.50 μm^2	eDRAM	36	1.2	N.D.	43.2
[7]	Renesas /150nm /0.98 μm^2	TFT+DRAM	20	2.0	26	40
[4]	Atmel /250nm / 10 μm^2	Standard	x	2.7	10	x

Table 2 Summary of different SRAM technologies using the DRAM capacitors to decrease the SER sensitivity. A standard technology is given for comparison purpose.

2) Effect of tungsten on the SEU cross-section

A first set of simulations considers the BEOL composed of the silicon dioxide (SiO_2) and was performed as a function of energy for different critical charges: standard SRAM architecture (10fC), TFT architecture (26fC) and enhanced by the DRAM capacitor (66fC). The evolution of the proton cross-section as a function of energy for different critical charges is presented in Fig. 5. For a critical charge of 10fC (compatible with standard SRAMs of this technology), the

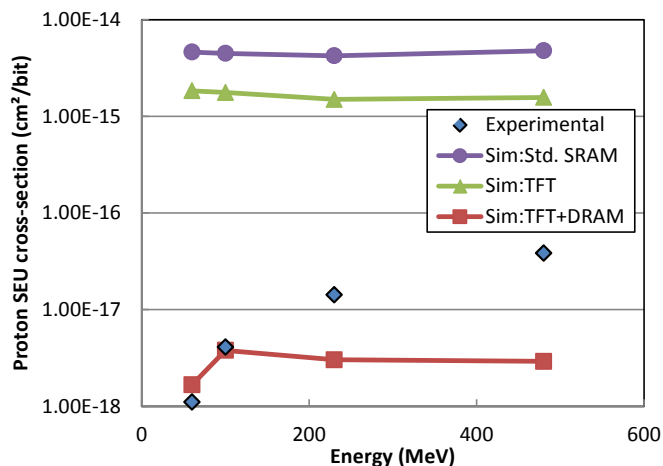


Fig. 5 Experimental data compared to the simulated proton SEU cross-sections as a function of energy for a BEOL composed of SiO_2 and for different critical charge values corresponding to a Standard SRAM (10fC), TFT technology (26fC) and TFT+DRAM technology (66fC).

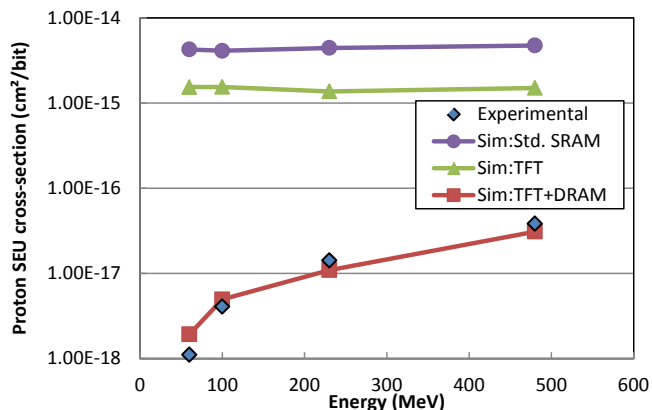


Fig. 6 Experimental data compared to the simulated proton SEU cross-sections as a function of energy for a BEOL composed of SiO_2 and W layer and for different critical charge values corresponding to a Standard SRAM (10fC), TFT technology (26fC) and TFT+DRAM technology (66fC).

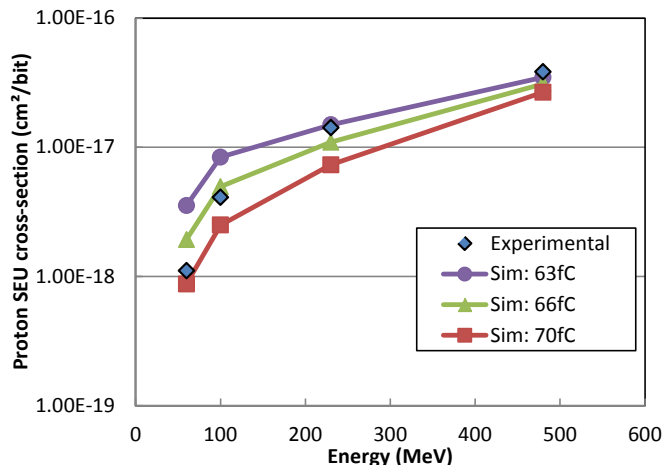


Fig. 7 Experimental data compared to the simulated proton SEU cross-sections as a function of energy for a BEOL composed of SiO_2 /tungsten and for different critical charge values close to the estimated value of 66fC.

proton cross-section remains practically constant for the energy ranges 60 to 500MeV. When increasing the critical charge above 20fC, the proton cross-section is constant or even slightly decreases with the energy as inelastic proton-

silicon collisions tend to create more light secondary particles with lower LET whose deposited energy in the sensitive volume does not exceed the critical charge. A visible increase in the measured proton cross-section cannot be explained with pure proton-silicon interactions.

A second set of simulations considers a BEOL composed of silicon dioxide with an additional layer of tungsten. For low critical charges, for which the cross-section is dominated by the p-Si reactions, the response is independent of energy similar to the case for structure without tungsten as the cross-section is dominated by silicon recoils. However, for a large critical charge, a significant relative increase with energy is observed, clearly showing the dominance of tungsten in the total error rate as shown in [11]. This can be seen in Fig. 6. An additional set of simulations were then performed around the previously estimated value of the critical charge of 66fC. Fig. 7 shows a very good agreement between simulation and experimental data, and confirming the cross-section increase of a factor of 25-30 observed experimentally between 60MeV and 480MeV. The experimental proton upset cross-sections are plotted counting all upsets. In the FLUKA simulations, the MBUs have not been modelled.

3) Contribution of tungsten regions to SEU cross-section

In a next step, the FLUKA bit cell model was refined to separately take into account the regions of tungsten silicide, the vias and the M1 layer. Fig. 8 shows the cross-section of the FLUKA memory bit-cell model. The light colour region is the memory bit-cell area and dark colour areas represent regions with tungsten contribution. Tungsten silicide covers the poly-silicon regions of the word line and two pull-down NMOS transistors which are shown in Fig. 8a. Each bit-cell uses four tungsten vias to connect to M1: bit line true, bit line false and two ground contacts (the two closest contacts from the neighbouring cell were also modelled) which are shown in Fig. 8b. There are four metal lines per cell (the fifth one from neighbouring cell is also considered) which are shown in Fig. 8c.

The simulations were run for a primary beam energy equal to 480MeV for which the contribution of tungsten to the total error rate was observed to be the highest. Table 3 shows the contributions of different SEU origins in the total error rate. The SEUs stemming from the silicon recoils account only for 9.5% to the total errors rate and as expected the cross-section is dominated by the presence of tungsten. The largest contribution comes from the SiW layer covering the Poly 1 layers as this region has a significant volume and is placed in direct contact with the sensitive volume. The contributions between M1 and vias are directly proportional to the volume of tungsten in each of these regions.

4) Implications of cross-section increase in LHC radiation environment

Fig. 9 shows the comparison between the experimental data and simulation in the extended energy range up to 10GeV simulated for the Renesas memory cell. Around 3GeV, the proton-induced fission in tungsten starts to saturate and its increase is only very moderate above this energy. This result has a significant impact on the error rate estimation for radiation environments such as the LHC for which over 10% of the total high energy hadron flux is located in the GeV energy range [6]. This value can reach even 50% for certain

LHC locations close to high-luminosity experiments. The standard testing procedures consider irradiation at 230MeV and assume to represent the saturation of the SEE cross-section at this energy. From such radiation tests, the error rate is estimated by convoluting this cross-section at saturation with the particle energy spectrum of the environment.

Considering two cross-sections presented in Fig. 9: a) experimentally measured SEU cross-section at 230 MeV and b) the simulated cross-section up to 10GeV, the expected error rate is 5.1 times higher for the second one than anticipated from a 230MeV cross-section measurement for the LHC tunnel conditions in which the majority of the FGCLite systems will operate. The LHC tunnel spectrum is similar to atmospheric one at the altitude of 20 km for which the error rate underestimation from 230 MeV will be comparable. The ground level and in the proton belt, spectra are softer, meaning the contribution of high energy particles is less significant, and the increase in the calculated error rate is thus smaller.

This example shows the importance of the cross-section analysis as a function of energy for some of the considered environments. A detailed analysis of the cross-section shape influence on the error rate computation for the LHC environment can be found in [6].

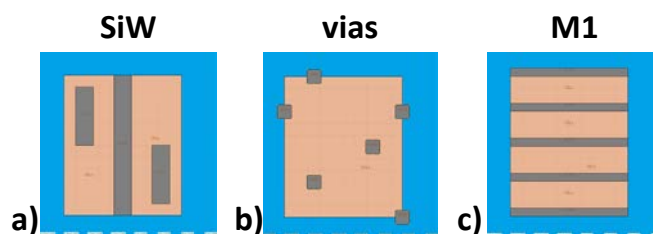


Fig. 8 Cross-section through the different BEOL layers containing tungsten: a) tungsten silicide (SiW), b) tungsten vias and c) metal 1 (M1) layer.

SEU origin	Si recoil	W from SiW	W from via	W from M1	Total
Contribution	9.5%	76.9%	5.5%	8.1%	100.0%

Table 3 Simulated contribution of different regions in the total upset rate for 480MeV protons.

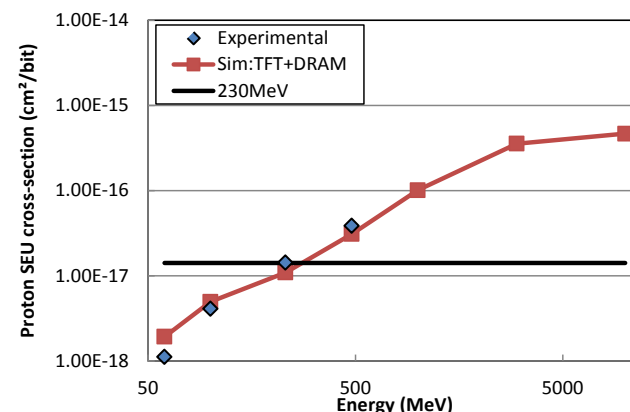


Fig. 9 Experimental data compared to the simulated proton SEU cross-sections as a function of energy for a BEOL composed of SiO₂/tungsten and for different critical charge values corresponding to a Standard SRAM (10fC), TFT technology (26fC) and TFT+DRAM technology (66fC). The experimental cross-section at 230MeV used for usual error prediction has been marked.

V. SUMMARY & FUTURE WORK

This work analysed the radiation performance of an SRAM bit-cell architecture hardened based on TFT PMOS transistors and additional DRAM capacitors. FLUKA simulations show that by increasing the critical charge, the contribution of silicon recoils to the error rate decreases while errors due to tungsten in the BEOL become dominant (above between 100 and 230MeV in the case of studied device). This leads to a proton cross-section increase with energies up to 500 MeV measured experimentally and beyond to around 3GeV predicted by model. This result is compatible with the estimations published in [11]-[12] where for SRAMs with low critical charge, no cross-section difference is expected as a function of energy and this difference appears when the critical charge increases.

There are two potential axes of future experimental characterizations that are considered to extend this work: 1) to perform proton measurements with GeV energies to prove the increasing trend in the SEU cross-section and 2) to perform heavy ion irradiation with higher LET values to assess the component heavy-ion cross-section at saturation and confirm that the low LET ion induced SEUs are caused by inelastic interactions.

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