ATCA-based ATLAS FTK input interface system

for clustering and data formatting prior to hardware-based tracking

1. General introduction and design concept
2. Implementation details
3. Status of system level demonstration at CERN

奥村恭幸
(OKUMURA, Yasuyuki)
University of Chicago
for FTK_IM & Data Formatter team

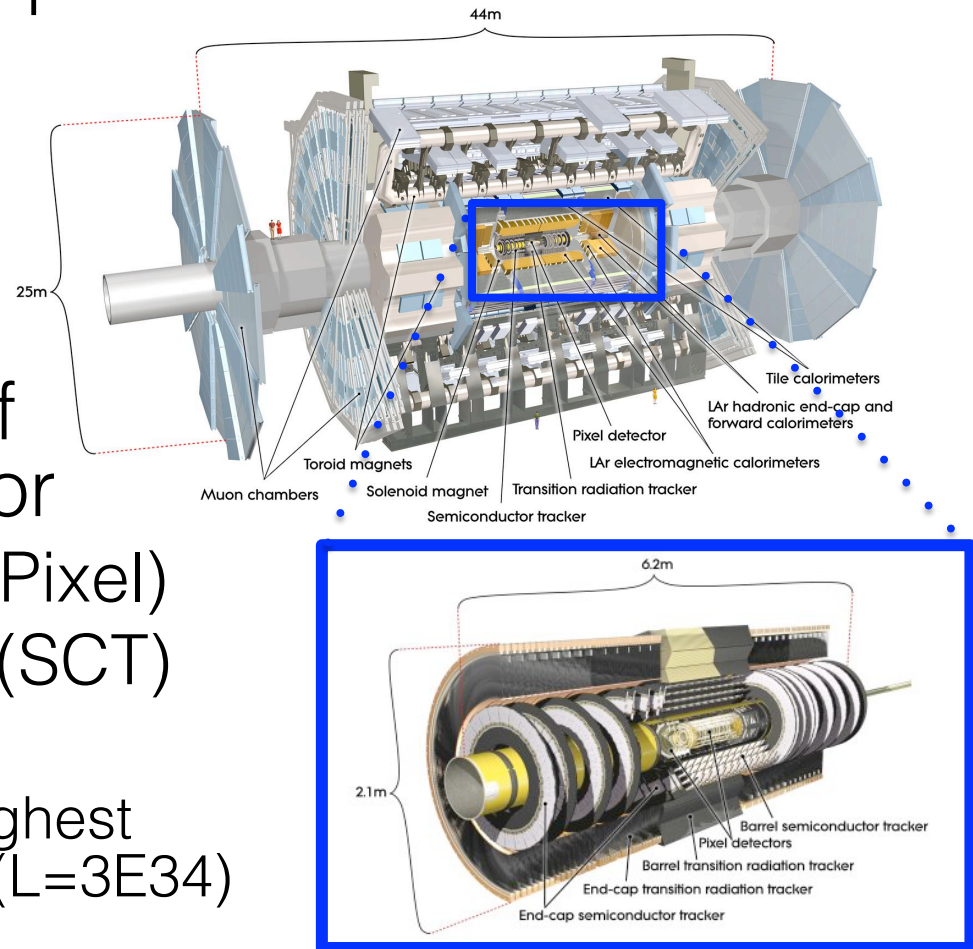# *ATLAS / silicon trackers*

- ATLAS is a general Purpose detector
  - Trackers
  - Calorimeters
 - Muon spectrometers

- 100 million channels of silicon tracking detector
  - 2D Pixel detector (IBL, Pixel)
  - 1D microstrip detector (SCT)
  - covering $|\eta| < 2.5$
    - 100k hits/event at the highest LHC phase I luminosity (L=3E34)

Fast TracKer in ATLAS Trigger

- ATLAS Trigger consisting of Level 1 (L1) hardware trigger and software based Higher Level Trigger (HLT)
- FTK is hardware-based tracking system for HLT algorithm
  - Process tracking all events accepted by Level-1 trigger (up to 100 kHz) within O(100μs)
  - With input of entire silicon channels with full resolution
  - Provide full track list for entire detector for those with $p_T > 1$ GeV with quasi-offline quality
- The availability of track information at beginning of HLT will help improvement of HLT for such as b-tag, tau-id, vertexing and more

FTK efficiency wrt offline ~ 93%
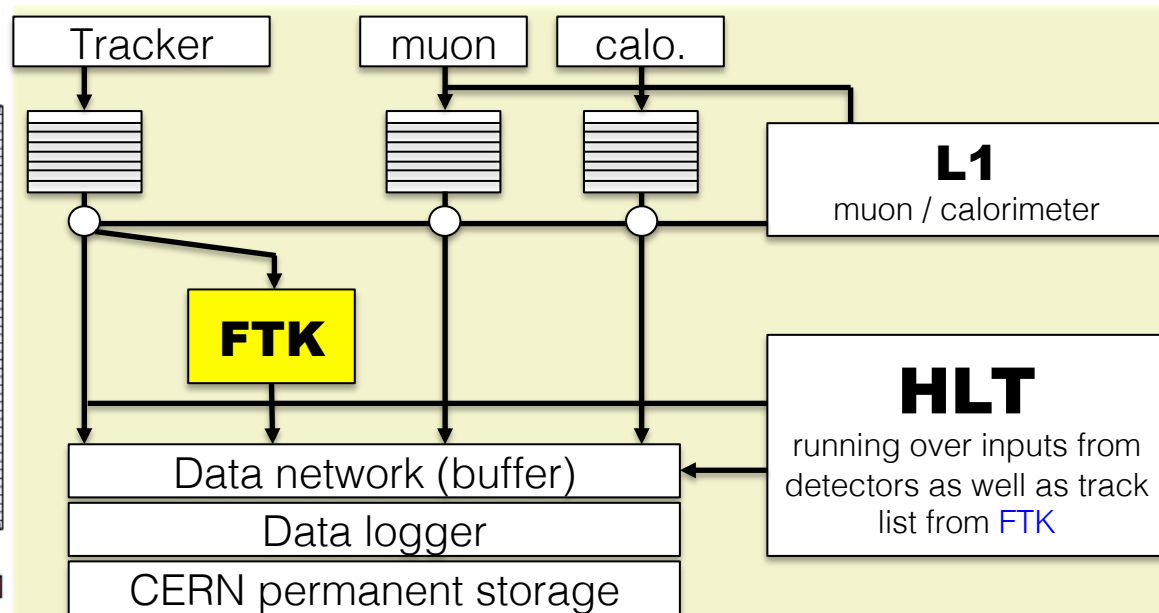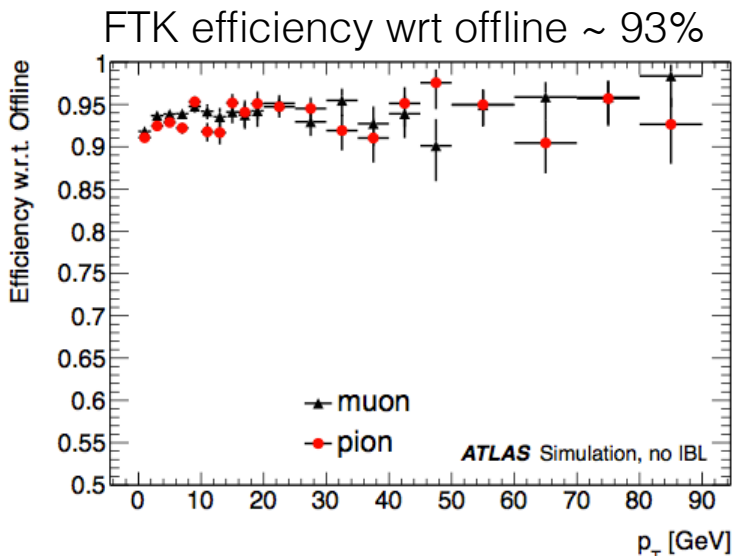
Integration and commissioning of FTK will start in 2015 during LHC Run2

Fast Tracker system diagram

- Pipeline of dedicated electronics

  1. Interface to Readout Driver (ROD)
  2. **Clustering / Data Formatting**
  3. Pattern matching
     – Associative Memory chips
  4. Track Fitting
     – FPGA based algorithm processing units
  5. Interface to HLT algorithms
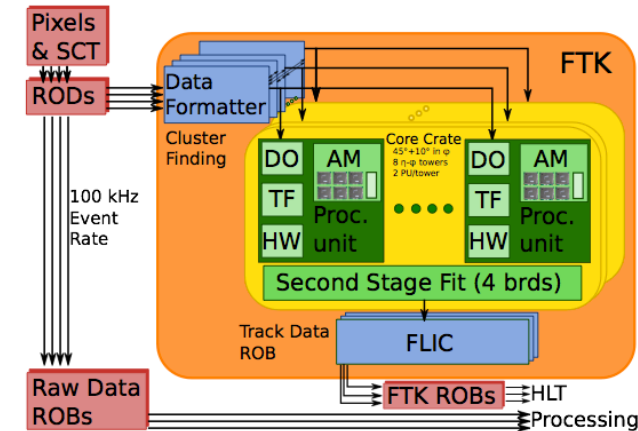
- Track Finding & Fitting is implemented in 64 η-ϕ overlapping FTK trigger towers as parallel processing unit
 - Finite size of beam luminous region / curvature of charged track
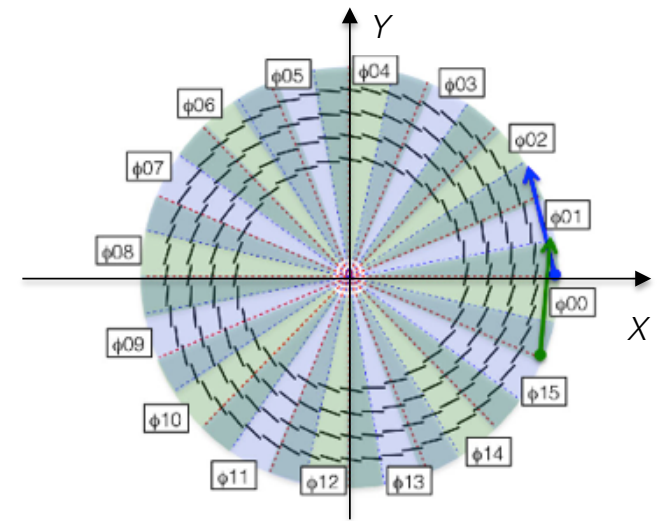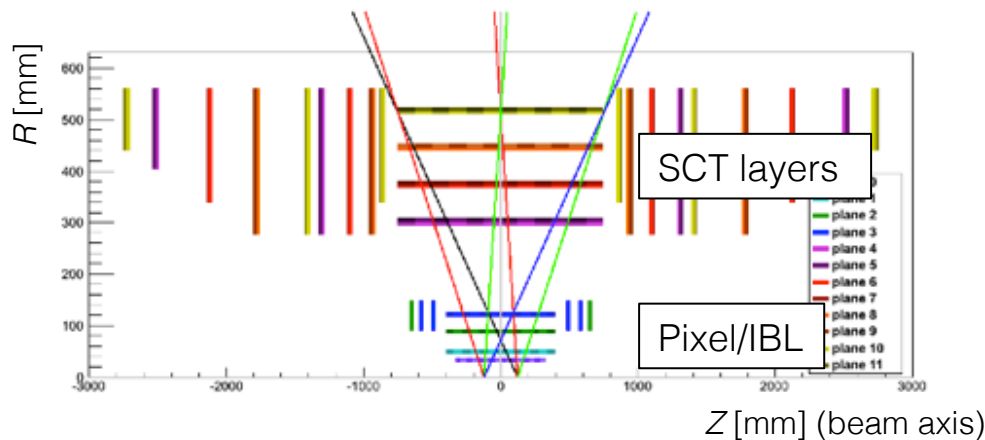
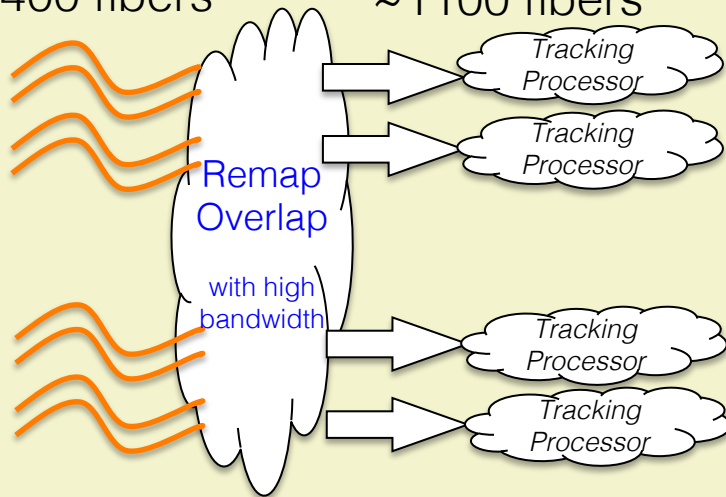# *Data Formatting requirement drives system design concept*

Requirement of Data Formatting prior to tracking

– Remapping input data into 64 FTK tower structure

  • ~400 fiber input from ROD~1,100 output fibers to downstream tracking boards

– Overlapping at boundary region of towers

– Handle large data volume
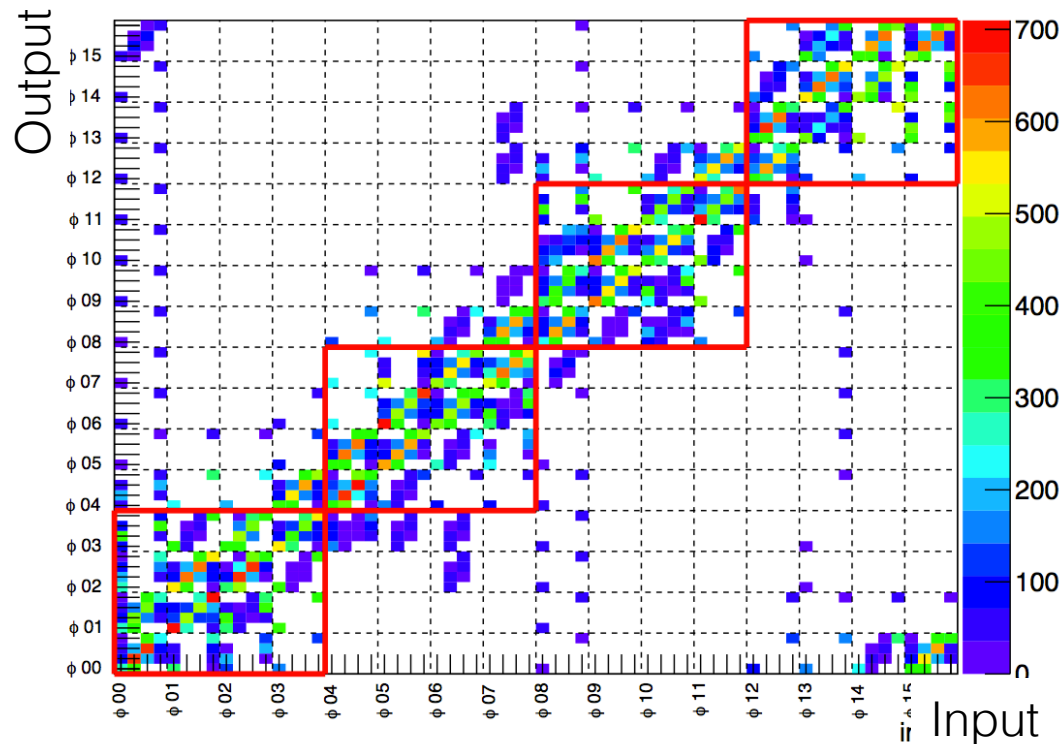
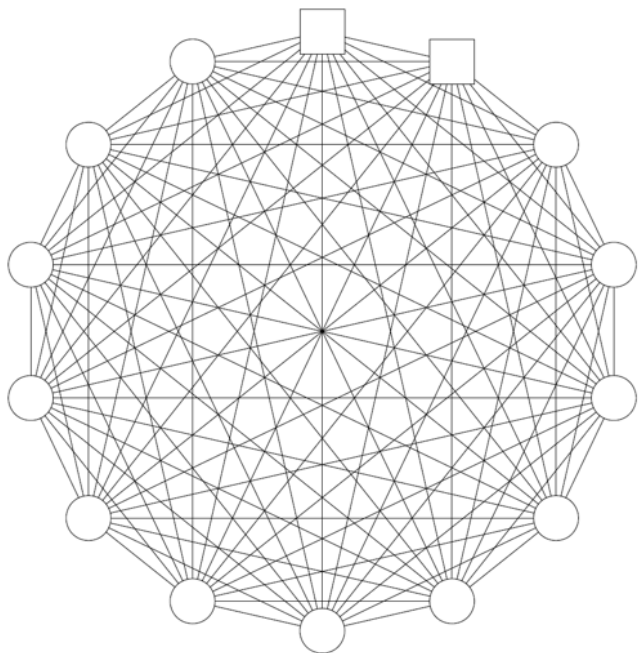**Four-shelf system** with **flexible connectivity in each crate** and **inter-crate links**

Full mesh ATCA

Advanced Telecommunication Computing Architecture (AdvancedTCA / ATCA) backplane supports Full Mesh network topology with high speed

Zone2 Connector
for full mesh

Network topology among the 14 boards in ATCA backplane
Up to 40 Gb/s point-to-point serial links

System level design

- Four shelf-system with internal connections
  - Eight boards per shelf, and 32 boards in total
    - Full-mesh communication with use of backplane
    - Inter-crate connections with optic fibers

From
ROD

To Downstream
FTK tracking
boards

~400
input
fibers

ROD data
(raw hits)

~1100
output
fibers

FTK eta-phi
Tower data
(clusters)
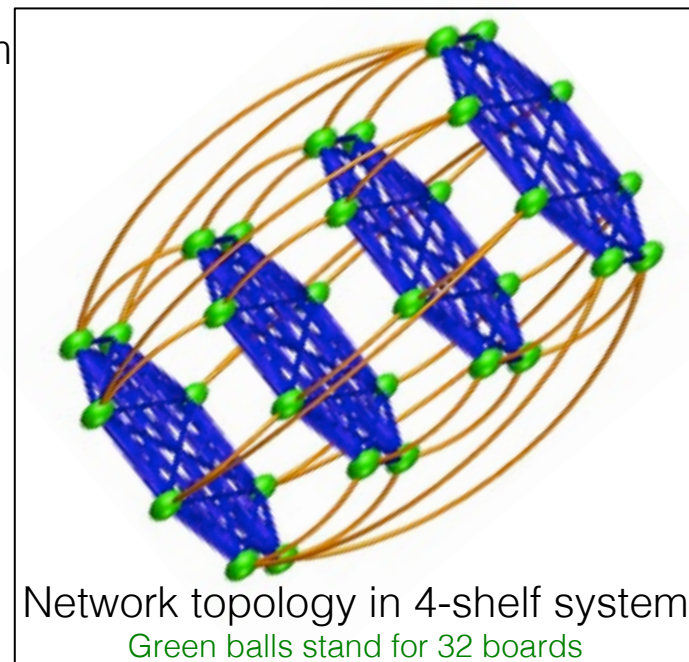
Network topology in 4-shelf system
Green balls stand for 32 boards

Board level design concept

- One board consists of three main components:
  1. Input clustering mezzanine cards (FTK_IM)
  2. Main data formatter board (Main board)
  3. Rear Transition Module (RTM) for optical fiber I/Os

Main data formatter board   RTM

Prototype available for testing

Block Diagram with Virtex7 FPGA

Photo of the prototype system

Data Formatter board is designed as general purpose board nicknamed "**Pulsar II**". See J.Olsen's talk (tomorrow 10:15) "Pulsar II: An FPGA-based Full Mesh ATCA Processor Board" and http://www-ppd.fnal.gov/ATCA/ for details for design, test, and application cases
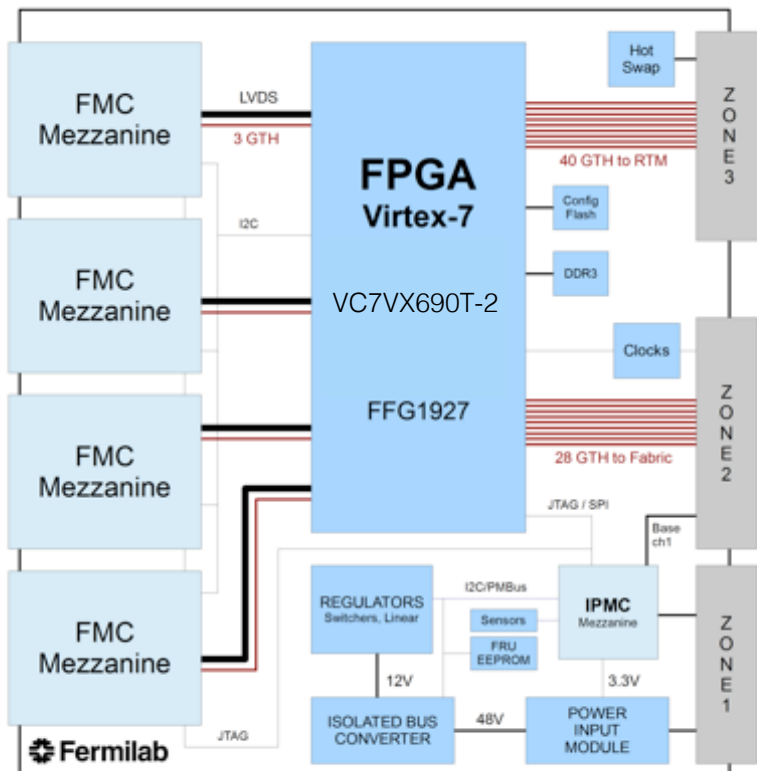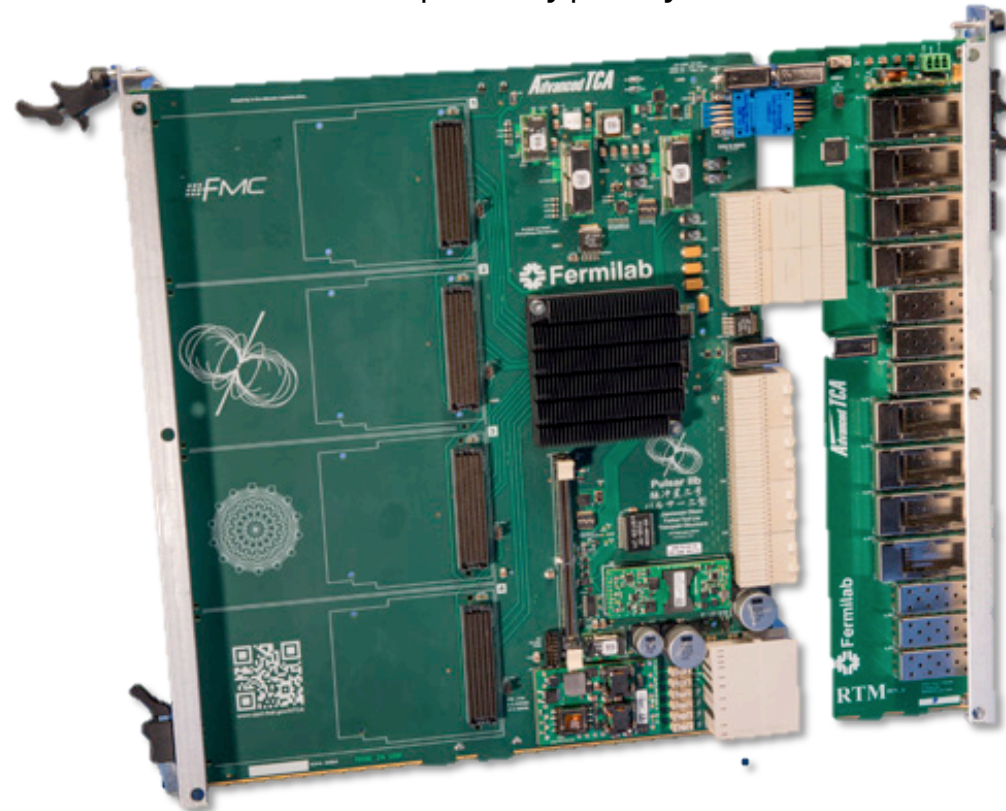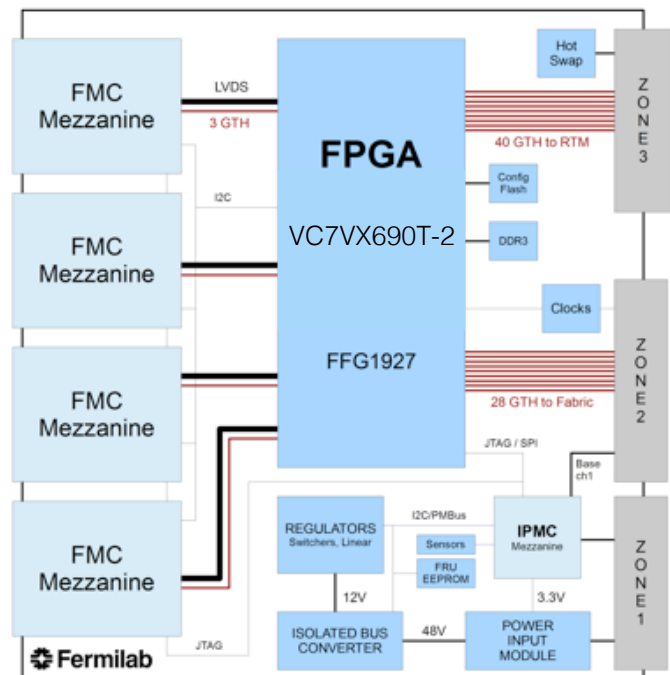
Challenge for Data Formatting - 1 : High speed implementation

- High speed lines are implemented with GTH transceivers implemented in FPGAs

- Measured bit error rate upper limit

  - ATCA backplane channels
    - BER < 2E-16 @ 10 Gb/s
  - RTM channels
    - BER < 5E-16 @ 10 Gb/s

- The requirement for FTK Data Formatter operation is 6Gb/s for them

The designed and tested speed performance well exceeds the FTK Data Formatting needs
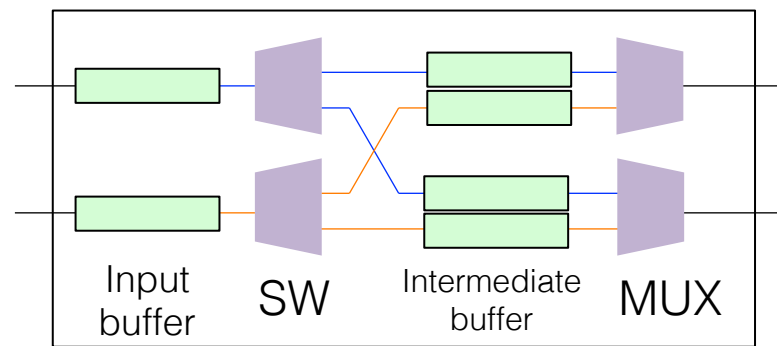
Challenge for Data Formatting - 2 : Routing logic implementation

- An alternative switch architecture with a banyan network
  - Each switch element contains FIFOs for internal data buffering
  - Efficient non blocking switch structure (unlike a simple "crossbar" network switch architecture) with reasonable resource usage
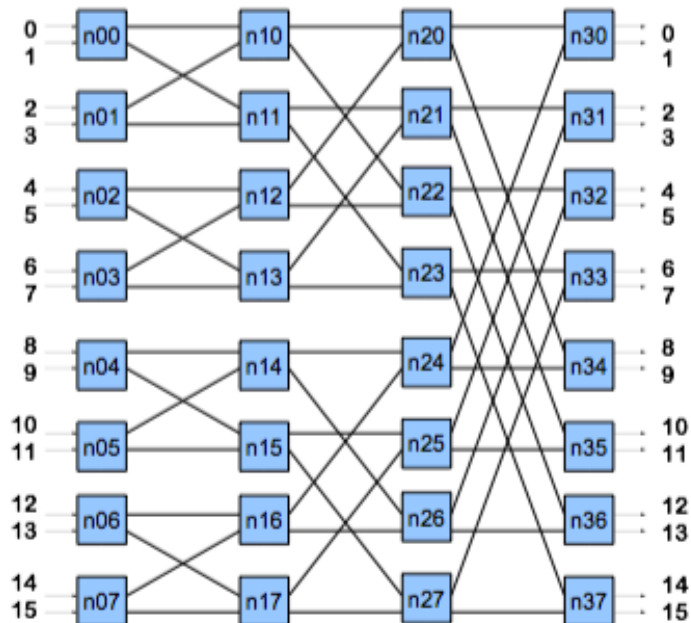
Example of 16-in & 16-out

2-in 2-out switch element

- Full implementation fits in available resources (~70%)

Input mezzanine (FTK_IM)
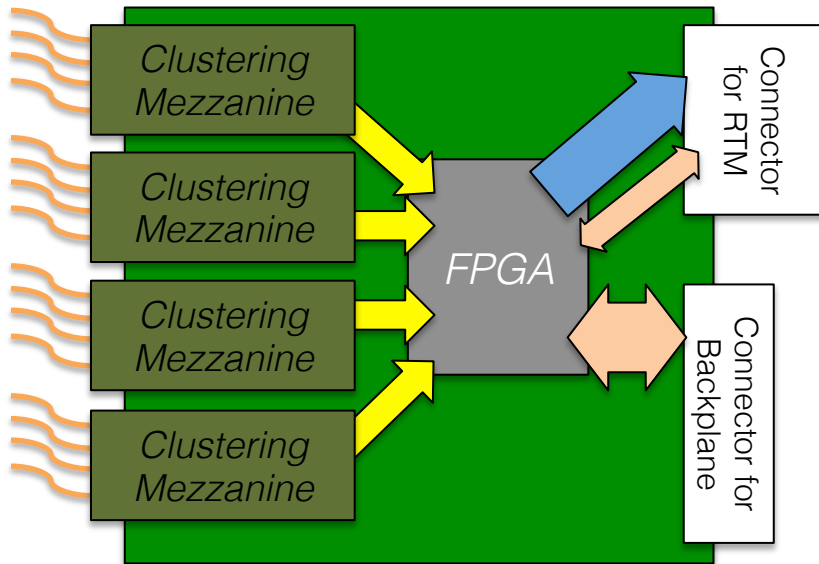
Receive data from Silicon RODs
- Up to four links per mezzanine
- Up to 16 links per main board with 4 IMs

Clustering prior to data formatting
- Reduce data volume without loss of efficiency
- Improve resolution

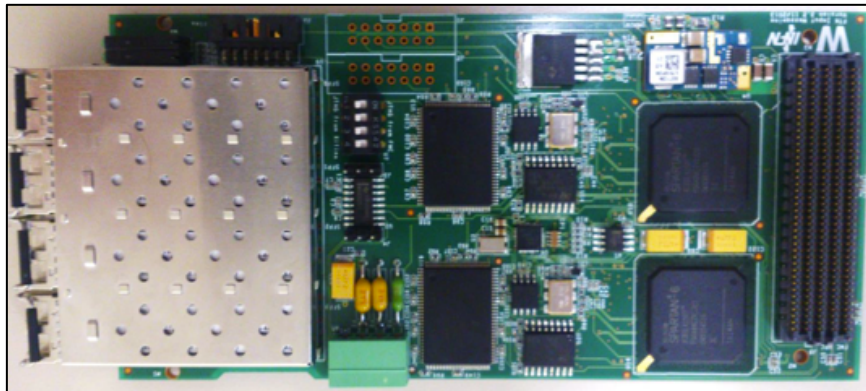**Send cluster to Data Formatter FPGA**

Photo of the prototype mezzanine card
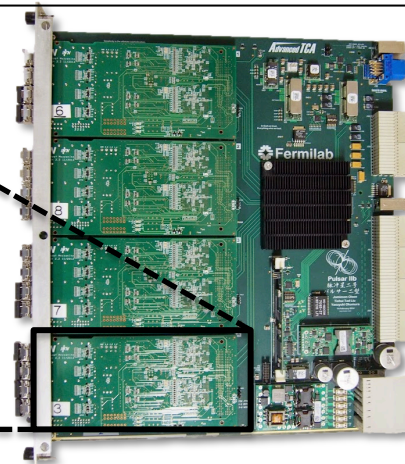
Input Mezzanine Card (FTK_IM)

- FTK Input Mezzanine card design:
  - Four Optical modules drivers for input optical fiber links
    - GTP transceiver channels (3.1 Gb/s @ maximum)
  - Two Spartan-6 FPGAs
    - Two input lanes per FPGA
  - Interface to main board with FMC standards
    - Power distribution
    - Clock sharing
    - JTAG / I²C
    - LVDS parallel data bus
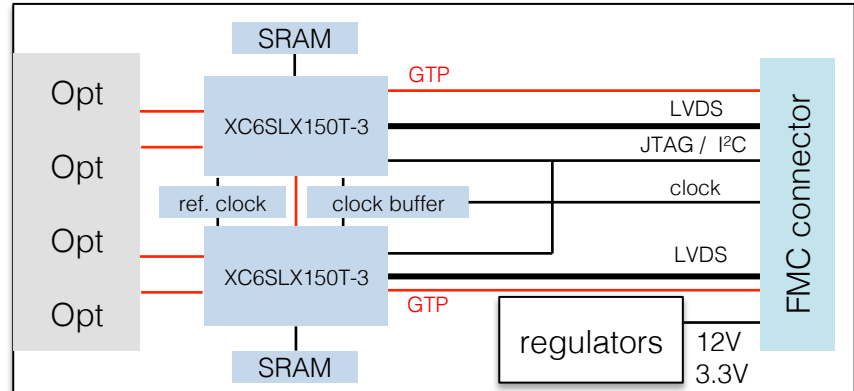
- Two decoupled cluster finder and centroid calculator
  - Major challenge is to maintain manageable process time of cluster finding with the highest target luminosity

Clustering algorithm

- Map pixel hits in 2D structure of cells in FPGAs so that hit selection can be done <u>two-dimensionally,</u> avoiding too many hit loops

    1. Define clustering window (21x8) w.r.t. the first hit (denoted as reference hit)
        - Coordinate is defined relative to the first hits (sliding window technique)
    2. Load all hits in the window size into logic cells mapped in FPGA
    3. Select <u>all hits neighboring to the seed / selected hits</u> for the cluster
    4. Read selected hits as a cluster (to be sent to the centroid calculator)
    5. Start to build the next clusters with remaining hits

10

10

8
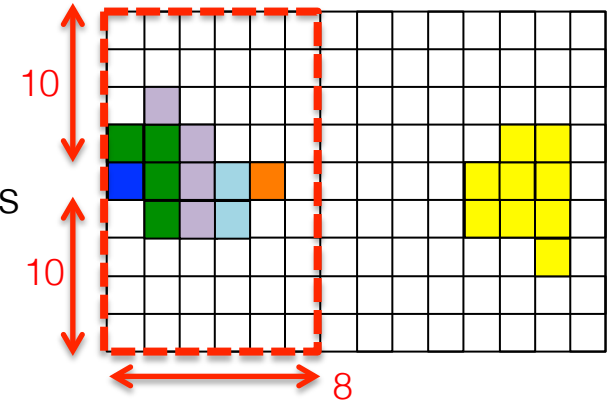
■ First hit as seed for the clustering
■ Hits selected in the second clock cycle
■ Hits selected in the third clock cycle
■ Hits selected in the forth clock cycle
■ Hits selected in the fifth clock cycle

■ Hits belonging to a different cluster

- Full implementation fits in available resources (~ 60%)

User interface for control path

- Control path to boards over Ethernet links
  - DF FPGA will have IP address
    - Can be controlled over Ethernet packet
    - CMS IPbus is used for this access
  - Each board DF FPGA drive the I^{2}C bus on the board to control FTK_IM
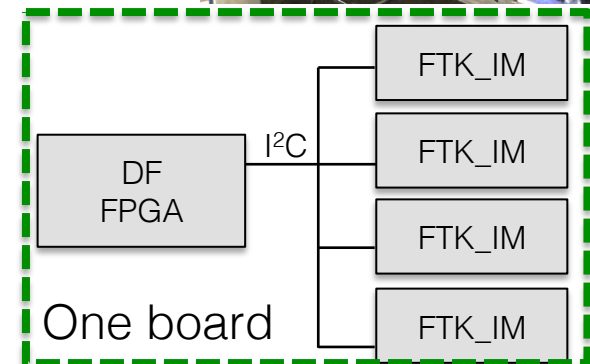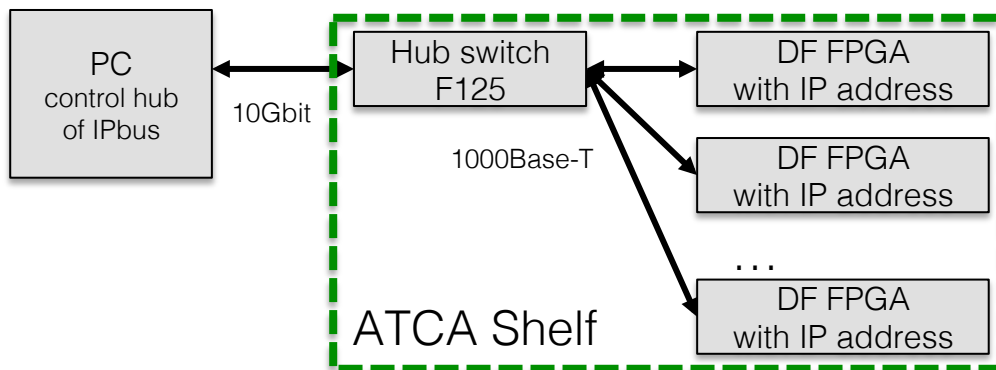
Methodology for testing

- Basic board performance tests has been done for design verification
  - First power-on
  - FPGA configuration
  - High speed I/O testing
    - Bit error rate test
    - RX margin analysis
  - Firmware testing in single board bench

- Extensive Interface functionality test
  - ROD – FTK_IM with SLINK (2Gb/s)
  - FTK_IM – DF with LVDS parallel bus (6.4Gb/s/card with 200Mb/s/pair)
  - DF – Downstream FTK processor with SLINK (6.4Gb/s)

Operation demonstration

- Test bench with 6U shelf at CERN for integration testing has been established

- Achievements as of today
  - IPbus / I^2C user interface implemented in CERN network, used for configuration, monitoring, and debugging
  - Dataflow demonstration with test vector simulated at L=3.0E34 /cm^2/s
    - Started with minimal setup :
      - One FTK_IM and one Data Formatter board at 80 kHz L1A rate
      - Four FTK_IMs and speeding up is on-going
    - 2D clustering for Pixel and 1D clustering for SCT in FTK_IM
    - Configurable switching data formatting on Data Formatter
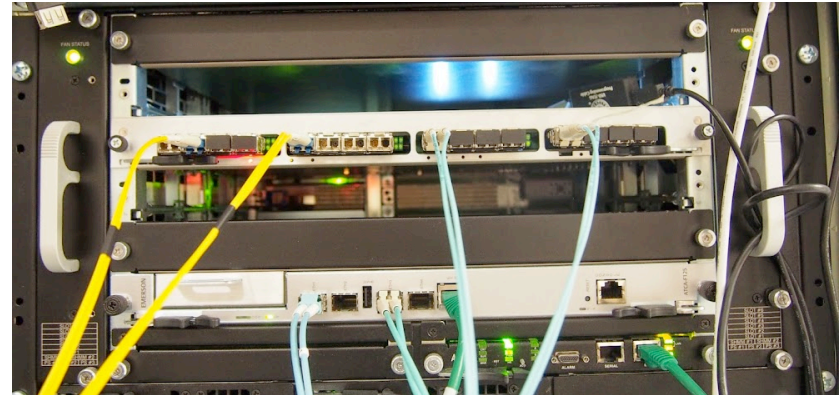
Summary

- ATLAS FTK input interface system has been designed
  - Clustering and Data Formatting
  - Full mesh ATCA-based design
    has been taken as a natural solution
- Prototype board has been manufactured and the basic board performance has been tested extensively
- Solutions for Data Formatting and Clustering implementation challenges are being tested
  - Full implementation fits available resource in chosen FPGAs
- Operation demonstration is on-going at CERN
- Next milestones towards commissioning in 2015 Run2
  - Demonstration with larger system (full-crate / multi-crate)
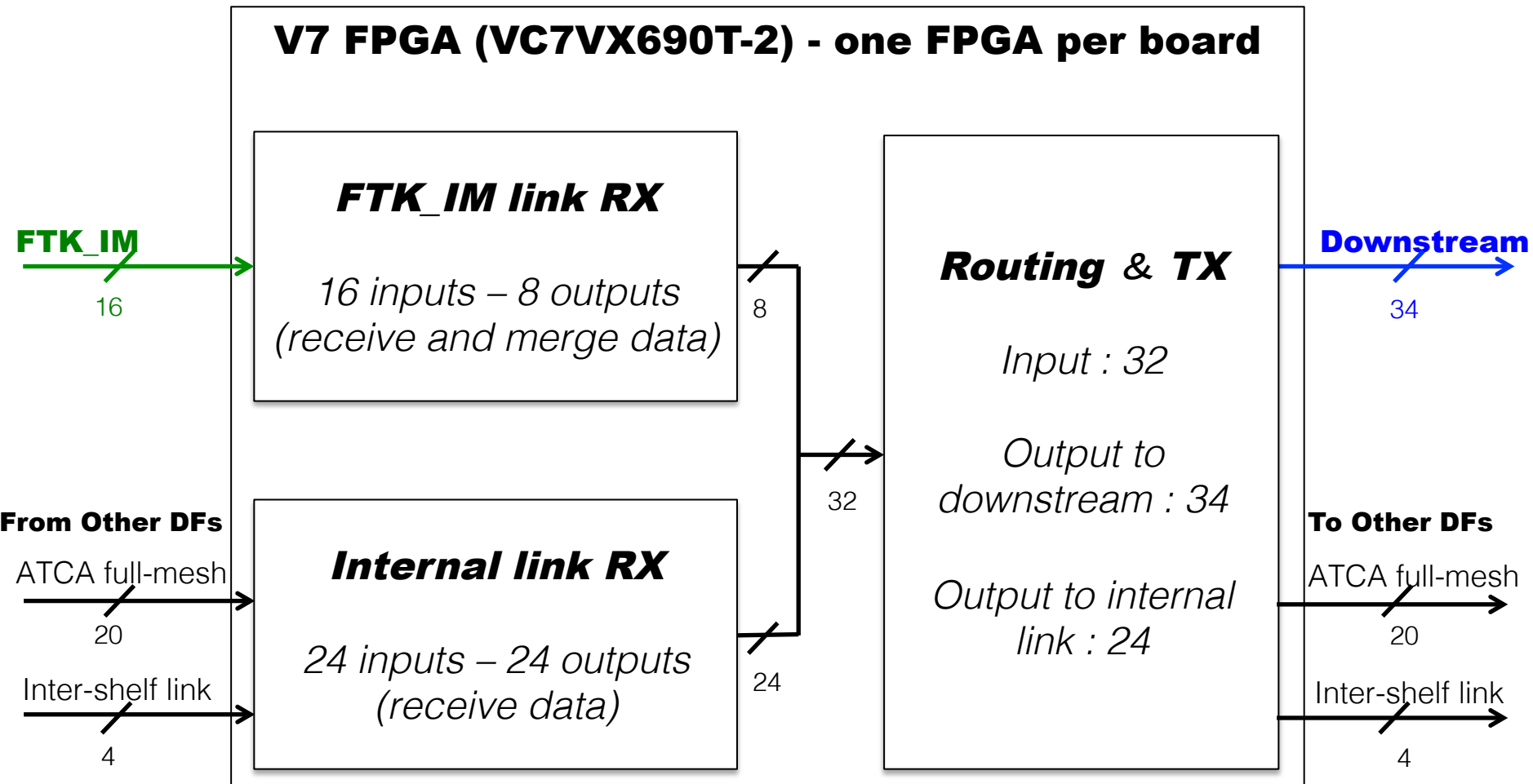 - Preparation for mass production

FTK_IM / DF team members

- Okumura, Y : University of Chicago
- Liu, T : Fermilab
- Olsen, J : Fermilab
- Iizawa, T : Waseda University
- Mitani, T : Waseda University
- Korikawa, T : Waseda University
- Yorita, K : Waseda University
- Annovi, A : INFN Frascati
- Beretta, M : INFN Frascati
- Gatta, M : INFN Frascati
- Sotiropoulou, C : Aristotle University of Thessaloniki
- Gkaitatzis, S : Aristotle University of Thessaloniki
- Kordas, K : Aristotle University of Thessaloniki
- Kimura, N : Aristotle University of Thessaloniki
- Cremonesi, M : University of Chicago
- Yin, H : Fermilab
- Xu, Z : Peking University

Backup materials

Data Formatter firmware diagram

V7 FPGA (VC7VX690T-2) - one FPGA per board

FTK_IM

16

FTK_IM link RX

16 inputs – 8 outputs (receive and merge data)

8

Routing & TX

Input : 32

Output to downstream : 34

Output to internal link : 24

Downstream

34

32

From Other DFs

ATCA full-mesh

20

Inter-shelf link

4

Internal link RX

24 inputs – 24 outputs (receive data)

24

To Other DFs

ATCA full-mesh

20

Inter-shelf link

4

Fast TracKer system diagram

Transmitter to FTK

Dual HOLA card

ATCA for preparation

VME for Tracking

ATCA to organize results
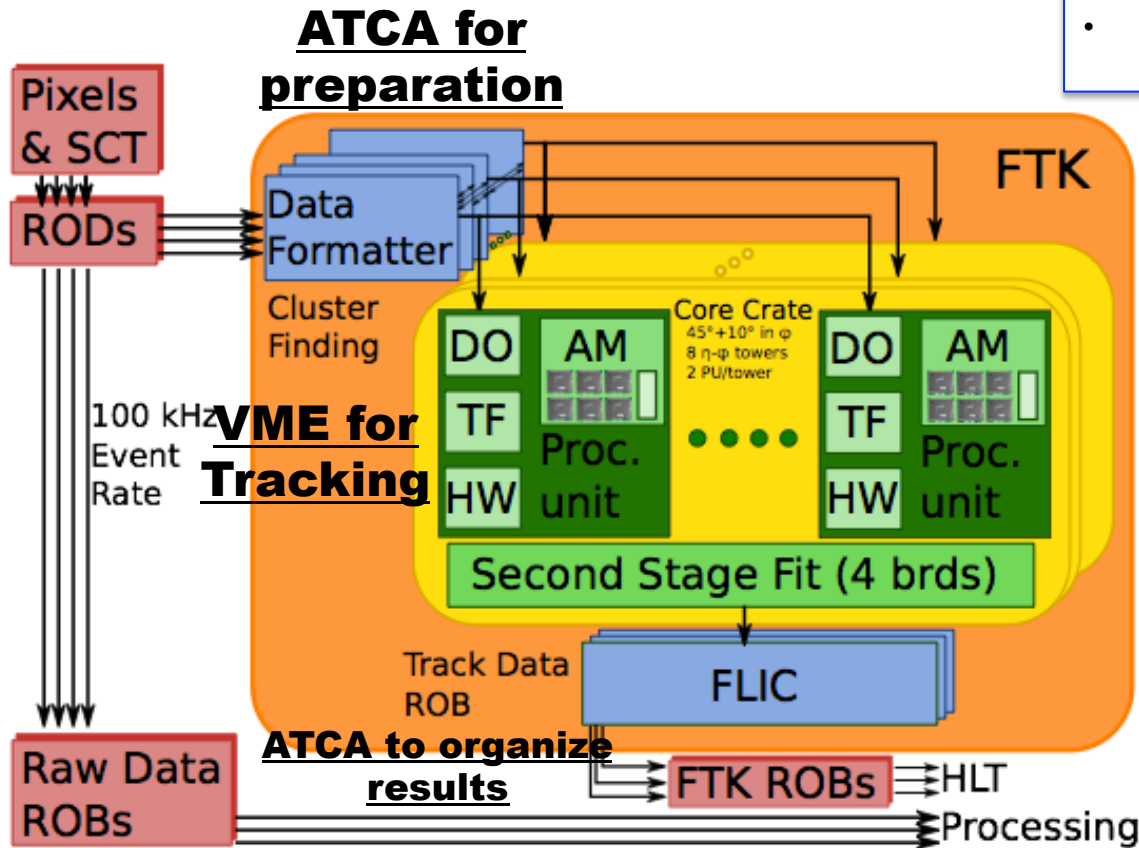
Preparation for FTK tracking

1. Input clustering mezzanine (IM)
2. Data Formatter (DF)
   - Organize SLINK input into 64 overlapping FTK eta-phi towers for parallel processing

Parallel processing Tracking Engine

3. AM Board + AM Chip
   - Track finding with 8 layers on Associative Memory (AM) chips
4. AUX card
   - 1st stage fitting with 8 layers
   - Interface to the DF / AM board
5. Second Stage Board (SSB)
   - 2nd stage fitting with 12 layers
   - Global duplication removal

Interface to the FTK ROBs

6. FLIC board