The LHCb Timing and Fast Control system

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Abstract

In this paper we describe the LHCb Timing and Fast Control (TFC) system. It is different from that of the other LHC experiments in that it has to support two levels of high-rate triggers. Furthermore, emphasis has been put on partitioning and on locating the TFC mastership in one type of module: the Readout Supervisor. The Readout Supervisor handles all timing, trigger, and control command distribution. It generates auto-triggers as well as controls the trigger rates.

Partitioning is handled by a programmable patch panel/switch introduced in the TTC distribution network between a pool of Readout Supervisors and the Front-End electronics.

I. Introduction

LHCb has devised a Timing and Fast Control (TFC) system[1] to distribute information that must arrive synchronously at various places in the experiment. Examples of this kind of information are:

- LHC clock
- Trigger decisions
- Reset and synchronization commands
- Bunch crossing number and event number

Although the backbone of the timing, trigger and control distribution network is based on the CERN RD12 system (TTC)[2], several components are specific to the LHCb experiment due to the fact that the readout system is different from that of the other experiments in several respects. Firstly, the LHCb TFC system has to handle two levels of high-rate triggers: a Level 0 (L0) trigger with an accept rate of maximum 1.1 MHz and a Level 1 (L1) trigger with an accept rate of maximum 40 - 100 kHz. This feature reflects itself in the architecture of the Front-End electronics, which consists of a L0 part and a L1 part (see Figure 1). The L0 Front-End (FE) electronics samples the signals from the detector at a rate of 40 MHz and stores them during the duration of the L0 trigger processing. The event data are subsequently de-randomized before being handed over to the L1 FE electronics. The L1 FE electronics buffers the data during the L1 trigger processing, de-randomizes the events before it zero-suppresses the data, and finally feds the data into the DAQ system for event building.

Secondly, the TFC architecture has been designed with emphasis on partitioning[3]. A partition is in LHCb a generic term, defined as a configurable ensemble of parts of a sub-detector, an entire sub-detector or a combination of sub-detectors that can be run in parallel, independently and with a different timing, trigger and control configuration than any other partition.

Furthermore, the aim has been to locate the entire TFC mastership of a partition in a single module. The trigger decision units are also considered as sub-detectors.

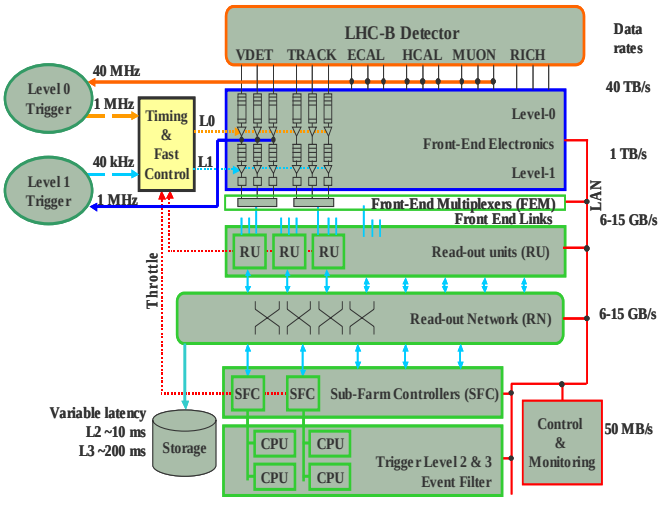

Figure 1: Overview of the LHCb readout system.

II. Use of the TTC system

The TTC system has been found to suite well the LHCb application. The LHC clock is transmitted to all destinations using the TTC system and Channel A is used as it was intended, i.e. to transmit the LHCb L0 trigger decisions to the FE electronics in the form of a accept/reject signal at 40 MHz.

Channel B supports several functions:

- Transmission of the Bunch Counter and the Event Counter Reset (BCR/ECR).
- Transmission of the L1 trigger decision (~1.1 MHz).
- Transmission of Front-End control commands, e.g. electronics resets, calibration pulse triggering etc.

Table 1: Encoding of the Channel B broadcasts. "R" stands for reserve bit.

	7	6	5	4	3	2	1	0
L1 Trigger	1	Trigger type			EventID		0	0
Reset	0	1	R	L1 EvID	L1 FE	L0 FE	ECR	BCR
Calibration	0	0	0	1	Pulse type		0	0
Command	0	0	R	R	R	R	R	R

The information is transmitted in the form of the short broadcast format[4], i.e. 16 bits out of which two bits are dedicated to the BCR/ECR and six bits are user defined.

From the TTC bandwidth it follows that a maximum of ~2.5 MHz of broadcasts can be transmitted. The eight bits are encoded according to Table 1. A priority scheme determines the order in which the different broadcasts are transmitted in case they clash.

III. TFC COMPONENTS SPECIFIC TO LHCB

The TFC architecture is shown in Figure 2. It incorporates a pool of TFC masters, Readout Supervisors[5], one of which is interfaced to the central trigger decision units and that is used for normal data taking. The other Readout Supervisors are reserves and can be invoked for tests, calibrations and debugging. The reserve Readout Supervisors also allow connecting local trigger units.

The TFC Switch[6] distributes the TTC information to the Front-End electronics and the Throttle Switches[6] feed back hardware throttle signals from the L1 trigger system, the L1 de-randomizers and components in the data-driven part of the DAQ system, to the appropriate Readout Supervisors.

The Throttle ORs[6] form a logical OR of the throttle signals from sets of Front-End electronics.

A GPS system allows time-stamping the local event information sampled in the Readout Supervisor.

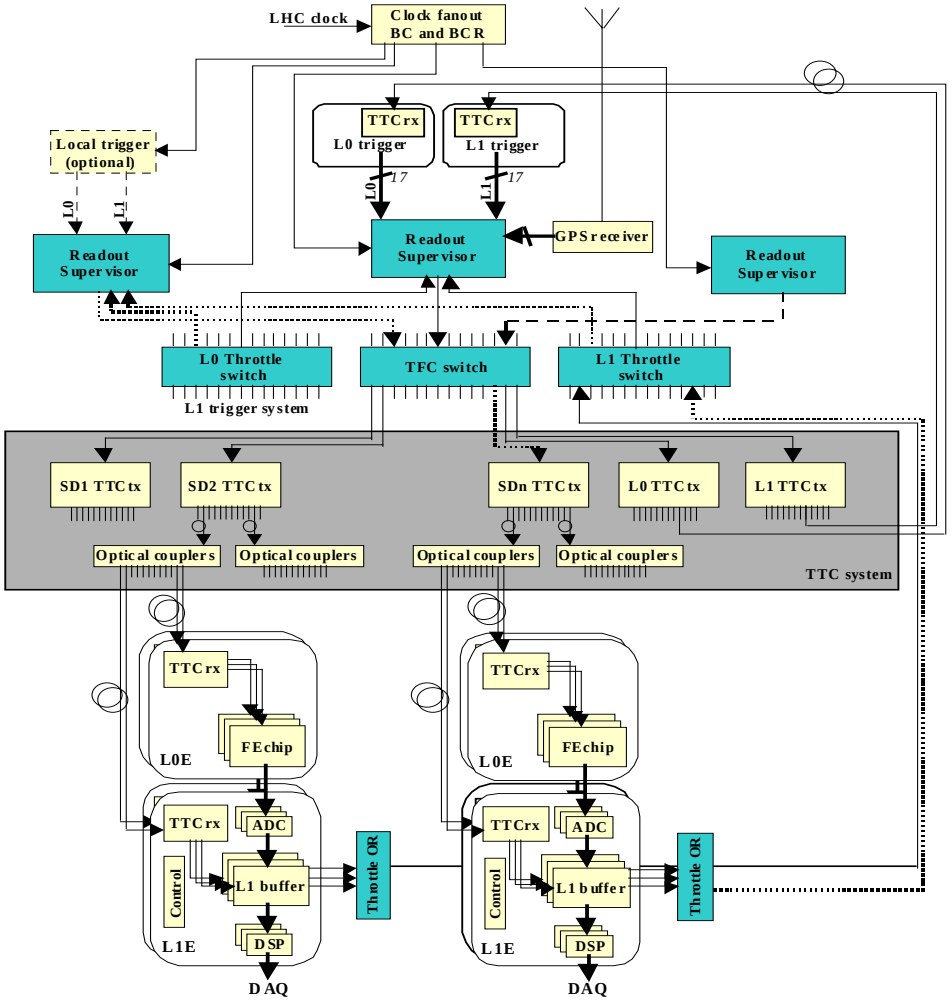

Figure 2: Overview of the TFC architecture.

IV. THE READOUT SUPERVISOR

The Readout Supervisor has been designed with emphasis on versatility in order to support many different types of running mode, and modifiability for functions to be added and changed easily. Below is a summary of the most important functions. A complete description can be found in Reference [5].

The TTC encoder circuit incorporated in each Readout Supervisor receives directly the LHC clock and the orbit signal from the TTC machine interface (TTCmi). The clock is distributed on the board in a star fashion and is transmitted to all synchronous destinations via the TTC system.

The Readout Supervisor receives the L0 trigger decision from the central L0 trigger Decision Unit (L0DU), or from an optional local trigger unit, together with the Bunch Crossing ID. In order to adjust the global latency of the entire L0 trigger path to a total of 160 cycles, the Readout Supervisor has a pipeline of programmable length at the input of the L0 trigger. Provided no other changes are made to the system, the depth of the pipeline is set once and for all during the commissioning with the first timing alignment. The Bunch Crossing ID received from the L0DU is compared to the expected value from an internal counter in order to verify that the L0DU is synchronized. For each L0 trigger accept, the source of the trigger (3-bit encoded) together with a 2-bit Bunch Crossing ID, a 12-bit L0 Event ID (number of L0 triggers accepted), and a "force bit" is stored in a FIFO. The force bit indicates that the trigger has been forced and that consequently the L1 trigger decision should be made positive, irrespective of the decision of the central L1 trigger Decision Unit (L1DU). The information in the FIFO is read out at the arrival of the corresponding L1 trigger decisions from the L1DU.

The RS receives the L1 trigger decision together with a 2-bit Bunch Crossing ID and a 12-bit L0 Event ID. The two incoming IDs are compared with the IDs stored in the FIFO in order to verify that the L1DU is synchronized. If the force bit is set the decision is converted to positive. The 3-bit trigger type and two bits of the L0 Event ID is subsequently transmitted as a short broadcast according to the format in Table 1. In order to space the L1 trigger decision broadcasts a L1 de-randomizer buffer has been introduced.

The Readout Supervisor controls the trigger rates according to the status of the buffers in the system in order to prevent overflows. As the distance and the high trigger rate, the L0 de-randomizer buffer occupancy cannot be controlled in a direct way. However, as the buffer activity is completely deterministic, the RS has a finite state machine to emulate the occupancy. This is also the case for the L1 buffer. In case an overflow is imminent the RS throttles the trigger, which in reality is achieved by converting trigger accepts into rejects. The slower buffers and the event-building components feed back throttle signals via hardware to the RS. Data congestion at the level of the L2/L3 farm is signalled via the Experiment Control System (ECS) to the onboard ECS interface, which can also throttle the triggers. "Stopping data taking" via the ECS is carried out in the same way. For monitoring and debugging, the RS has history buffers that log all changes on the throttle lines.

The RS also provides several means for auto-triggering. It incorporates two independent uniform pseudo-random generators to generate L0 and L1 triggers according to a Poisson distribution. The RS also has a unit running several finite state machines synchronized to the orbit signal for periodic triggering, periodic triggering of a given number of consecutive bunch crossings (timing alignment), triggering at a programmable time after sending a command to fire a calibration pulse, triggering at a given time on command via the ECS interface etc. The source of the trigger is encoded in the 3-bit L1 trigger qualifier.

The RS also has the task of transmitting various reset commands. For this purpose the RS has a unit running several finite state machine, also synchronized to the orbit signal, for transmitting Bunch Counter Resets, Event Counter Resets, L0 FE electronics reset, L1 + L0 electronics reset, L1 Event ID resets etc. The RS can be programmed to send the commands regularly or solely on command via the ECS interface. The Bunch Counter and the Event Counter Reset have highest priority. Any clashing broadcast is postponed until the first broadcast is ready (L1 trigger broadcast) or until the next LHC orbit (reset, calibration pulse, and all miscellanous commands).

The RS keeps a large set of counters that record its performance and the performance of the experiment (dead-time etc.). In order to get a consistent picture of the status of the system, all counters are samples simultaneously in temporary buffers waiting to be read out via the onboard ECS interface.

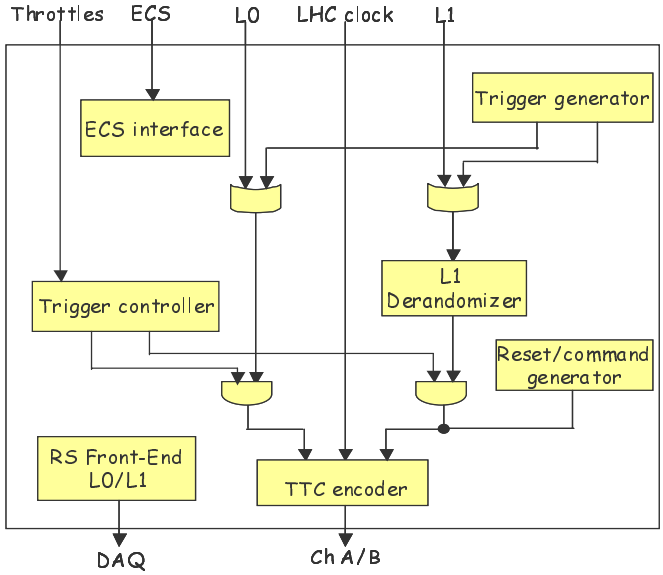

Figure 3: Simplified logical diagram of the Readout Supervisor showing the basic functions.

The RS also incorporates a series of buffers analogous to a normal Front-End chain to record local event information and provide the DAQ system with the data on an event-by-event basis. The "RS data block" contains the "true" bunch crossing ID and the Event Number, and is merged with the other event data fragments during the event building.

The ECS interface is a Credit Card PC through which the entire RS is programmed, configured, controlled, and monitored. Note that in order to change the trigger and control mode of the RS for testing, calibrating and debugging it is not necessary to reprogram any of the FPGAs. All functionality is set up and activated via parameters that can be written at any time.

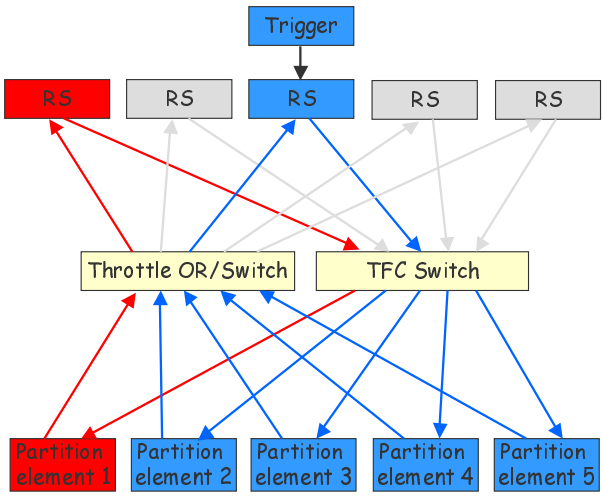

Figure 4: The TFC architecture simplified to show an example of partitioning.

A. *The TFC Switch and Partitioning*

A good partitioning scheme is essential in order to carry out efficient commissioning, testing, debugging, and calibrations. The LHCb TFC partitioning is shown by an example in figure 4, in which the TFC architecture in Figure 2 has been simplified. The TFC Switch allows setting up a partition by associating a number of partition elements (e.g. sub-detectors) to a specific Readout Supervisor (Figure 5). The Readout Supervisor can then be configured to control and trigger the partition in whatever specific mode that is required. In the example in figure 4, the partition elements 2 – 5 are running with the central RS, which is interfaced to the central triggers. Partition element 1 is simultaneously running a stand-alone run with a separate RS. The three other Readout Supervisors are idle and can be reserved at any time for other partitions. Note that the TFC Switch is located before the TTC optical transmitters (TTCtx) and that it is handling the encoded TTC signals electrically.

The configuring of the TFC Switch is done via the standard LHCb ECS interface incorporated onboard: the Credit Card PC.

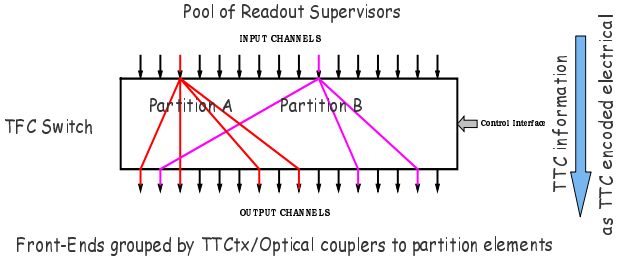

Figure 5: The principle of the TFC Switch.

From the architecture of the system it follows that the FE electronics that is fed by the same TTCtx is receiving the same timing, trigger, and control information. Hence the TTCtx define the partition elements. The TFC Switch has been designed as a 16x16 switch and thus allows the LHCb detector to be divided into 16 partition elements. To increase the partition granularity an option exists whereby four TFC Switches are deployed in order to divide the LHCb detector into 32 partitions (Figure 6).

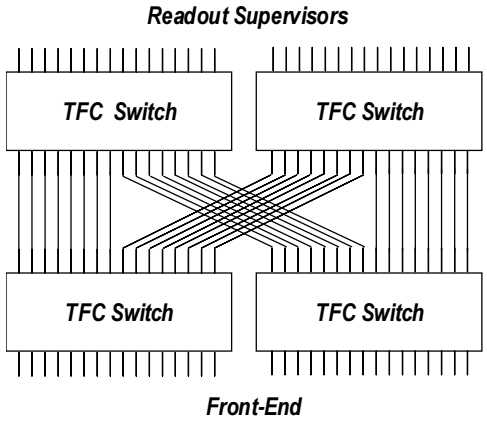

Figure 6: Four TFC Switches put together to increase the partition granularity to 32.

A crucial point concerning the TFC Switch is that all internal paths from input to output must have equal propagation delays. Otherwise, the partition elements will suffer from timing alignment problems using different Readout Supervisors. Measurements performed on the first prototype of the TFC Switch shows that it will be necessary to add adjustable delays at the outputs due to strongly varying propagation delays in the 16:1 multiplexers used.

B. *The Throttle Switches and the Throttle ORs*

The function of the Throttle Switches is to feed back the throttle information to the appropriate Readout Supervisor, such that only the Readout Supervisor in control of a partition is throttled by the components within that partition. Figure 4 shows an example of how they are associated. The logical operation of the Throttle Switch is to perform a logical OR of the inputs from the components belonging to the partition (Figure 7). The system incorporates two Throttle Switches, a L0 and a L1 Throttle Switch. The sources of L0 throttles are essentially the components that feed the L1 trigger system. The sources of L1 throttles are the L1 de-randomizers and the event building components.

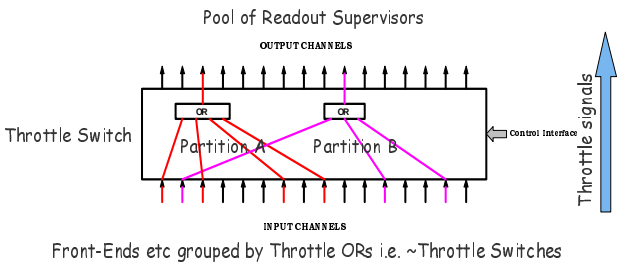

Figure 7: The principle of the Throttle Switches.

For monitoring and debugging, the Throttle Switches keep a log of the history of the throttles. A transition on any of the

throttle lines trigger the state of all throttle lines together with a time-stamp to be stored in a FIFO.

The configuring and the monitoring of the Throttle Switches are done via the standard LHCb ECS interface.

The Throttle ORs group throttle lines belonging to the same partition elements. They are identical to the Throttle Switches in all aspects except that they OR all inputs and have only one output.

VI. Conclusions

The LHCb Timing and Fast Control (TFC) system and the use of the TTC system are well established. The Readout Supervisor incorporates all mastership in a single module and it provides a lot of flexibility and versatility. Partitioning is well integrated through the TFC Switch and the Throttle Switches.

The architecture and the components have been put through two reviews and the system is now in the prototyping phase.

V. References

[1] R. Jacobsson and B. Jost, "The LHCb Timing and Fast Control system", LHCb 2001-016 DAQ.

[2] RD-12 Documentation on WWW (http://www/cern.ch/TTC/intro.html) and references therein.

[3] C. Gaspar, R. Jacobsson, B. Jost, "Partitioning in LHCb", LHCb 2001-116 DAQ.

[4] B. Jost, "The TTC Broadcast Format (proposal)", LHCb 2001-017 DAQ.

[5] R.Jacobsson, B. Jost, Z. Guzik, "Readout Supervisor Design Specifications", LHCb 2001-012 DAQ.

[6] Z. Guzik, Richard Jacobsson, and B. Jost, "The TFC Switch specifications", LHCb 2001-018 DAQ.