CARIOCA - 0.25μm CMOS Fast Binary Front-End for Sensor Interface using a Novel Current-Mode Feedback Technique

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ABSTRACT

We report on a very fast and low noise front-end, implemented in 0.25μm CMOS technology. The CARIOCA♣ amplifier discriminator chip has input impedance of 10Ω, in order to be compatible with sensors of large capacitance, and a peaking time of 14ns. The conversion gain of 8mV/fC remains almost unchanged up to a detector capacitance of 120pF. A noise figure of 450e^- at zero input capacitance with a noise slope of 37.4e^-/pF, at a 2.5V power supply, was measured.

1. INTRODUCTION

Investigation of the characteristics of state-of-the-art in deep submicron CMOS technologies shows that analog circuits with very good performance can be designed using these processes. Deep submicron technologies are, in particular, well suited for the design of binary front-end systems. In these applications, the limitation on the dynamic range imposed by the squeezed power supplies is not the primary issue [1-3].

Current-mode architectures are an attractive alternative to the more conventional voltage-mode ones for very fast circuits. In the current mode approach, the signal is processed in the current domain, thus avoiding charging and discharging of the parasitic capacitance to "high" voltage levels and keeping the internal nodes of the circuit at low impedance values. Therefore, combining current-mode techniques with the use of deep submicron technologies provides the opportunity of building analog circuits with high speed and low power consumption.

The front-end CARIOCA has been designed for 2 types of sensors to be used in the next generation of high energy particle detectors. One is optimized for the readout of the Multi Wire Proportional Chambers (MWPC) [4] of the LHCb* Muon system [5] and the other for silicon strip detectors. This paper presents only the requirements and results for the LHCb muon chambers, which is the more challenging in terms of detector capacitance. This work has been done in the framework of the CERN RD49 project [6].

The LHCb Muon System is composed of five muon stations which provide muon identification and trigger formation The stations are equipped with MWPCs, that are required to have a time resolution of 3.5ns (rms). High rates of up to 800KHz per channel in some detector regions require fast pulse shaping circuits. The MWPCs capacitances range from about 10pF to 200pF and the input time constant, $\tau_{in}=R_{in}C_{in}$, ultimately limits amplifier speed. Therefore, the preamplifier input impedance has to be as low as possible. In addition, an amplifier input resistance below 50Ω is required in order to limit the capacitive crosstalk between adjacent sensor elements.

2. CIRCUIT TOPOLOGY

Fast low noise pulse amplifiers are usually based on charge or transimpedance circuits, and have limited performance at large detector capacitance. This limitation is mainly due to the structure of the feedback network, which converts the output voltage of the amplifier stage into a feedback current. To achieve a low resistance it is necessary to keep the closed loop gain small enough to get a high-speed response. As a consequence, the charge-to-voltage gain is smaller and the sensitivity and noise performance are substantially reduced. The present front-end uses a novel low noise current mode feedback circuit that can amplify current signals of large detector capacitances at very high speed without this drawback.

CARIOCA is a eight-channel low noise amplifier discriminator binary front-end developed in a 0.25μm CMOS technology, operating at 2.5V. The present front-end has been optimized for detector capacitances up to 120pF. Each processing channel is formed by a current mode preamplifier, a three-stage discriminator and a LVDS driver. The overall chain is DC, allowing very high counting rate readout operation without baseline shift effects. Only one signal return path is used (ground) to be more robust against voltage supply variations. Each channel has an independent biasing and threshold circuit, which minimizes crosstalk between channels. The analog structure of a single channel is shown in Figure 1.

Figure 1: CARIOCA front-end block diagram. Each channel consists of a preamplifier, a three-stage discriminator with an external reference and a LVDS driver.

♣ **C**ERN **A**nd **RIO** **C**urrent **A**mplifier.

* LHCb is one of the 4 detectors of the world's largest proton collider (LHC) presently under development at CERN and schedule to start operation in the year 2005.

2.1 Preamplifier

The preamplifier, shown in Figure 2, consists of a transconductance amplifier formed by a direct cascode stage with a large n-channel input transistor (N1). The width over length ratio of N1 is 1600µm/0.7µm. The drain current of 2mA is controlled by a p-channel cascode current source. The novel current mode feedback loop comprises a current mirror followed by the current source placed at the output of the transconductance amplifier. A current gain is provided at the output by the transconductance ratio of transistors N3 and N4, as given by the Equation 1.

$$\frac{I_{OUT}}{I_{IN}} = -\frac{g_{m_{N4}}}{g_{m_{N3}}}$$

Equation 1: CARIOCA preamplifier current gain, as a function of the transistor transconductance.

Due to the feedback, the preamplifier input resistance is determined by Equation 2. In this equation Ai is the current gain (I_B/I_A) from the input branch to the transistor N2. For frequencies up to 10MHz the input resistance stays at about 10Ω.

$$R_{IN} = \frac{g_{m_{N2}}}{g_{m_{N1}} g_{m_{N3}} A_i}$$

Equation 2: CARIOCA preamplifier input resistance, with $A_I=I_B/I_A$.

The output current of the preamplifier (I_{OUT}) is sent to the current discriminator and is converted in parallel to voltage by an internal buffer. The buffer is used to drive the preamplifier output voltage (V_{OUT}) to the chip pad without increasing considerably the capacitance on the discriminator node.

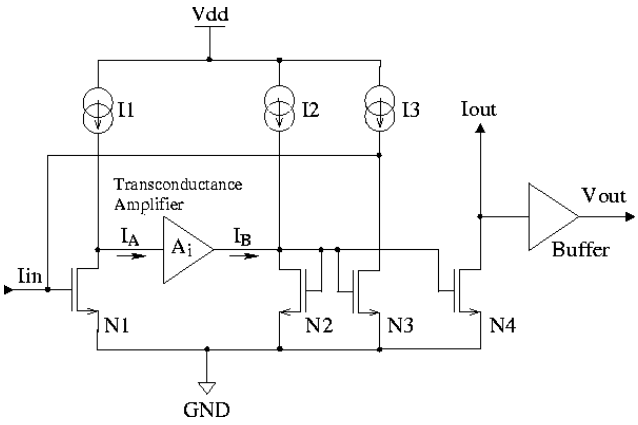

Figure 2: CARIOCA preamplifier schematic. The preamplifier consists of a transconductance amplifier of gain A_i, followed by a current mirror with a feedback loop. The output current (I_{OUT}) is sent to the discriminator and is converted to voltage by an internal buffer.

2.2 Discriminator

The discriminator consists of 3 stages: a current discriminator, a voltage sensing amplifier and a buffer followed by a LVDS driver, as shown in Figure 3. A baseline restoration based on a DC servo loop ensures both dynamic stability of the baseline and offset cancellation necessary with the fully DC coupled circuit.

The current discriminator is based on a current to voltage converter that feeds a voltage comparator. In order to achieve both high speed and high sensitivity the current to voltage converter is a p-channel transistor in common gate configuration. The threshold current is fixed by the width of the transistor P1 and P2 and by their bias current (I_{bias}), as shown in Equation 3:

$$I_{th} = \frac{W_{P2} - W_{P1}}{W_{P2}} \cdot I_{bias}$$

Equation 3: Discriminator current threshold.

In order to cancel the preamplifier offset, a compensation circuit which forces a positive offset, is added to the discriminator with an additional bias sources (I_4) and a low pass filtering capacitor (C_1).

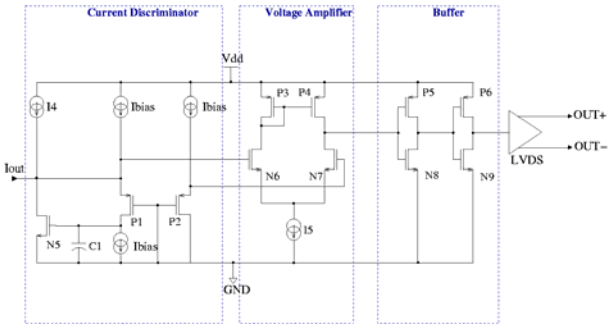

Figure 3: CARIOCA discriminator formed by a current discriminator, a voltage amplifier and a LVDS driver.

3. EXPERIMENTAL RESULTS

The CARIOCA low gain version was successfully operated with 2.5V power supply. The input signal and bias currents on the circuit were supplied by external resistors. An external operational amplifier is used to drive the output voltage from the preamplifier buffer. Examples of analog and digital signals are shown in Figure 4, at an input capacitance of 17pF. The analog signal is measured from the buffer connected to the preamplifier and the digital one from the LVDS driver. The positive overshoot is due to the baseline restoration circuit that produces a bipolar shape.

It is important to notice that all measurements were performed using an input signal with a rise time of 5ns, which shifts the peak position with respect to a delta pulse. This may reduce the preamplifier speed and sensitivity.

The sensitivity was measured for different detector capacitances and showed good uniformity up to 120pF within 5% error. The preamplifier gain is about 8mV/fC using an input signal of 5ns

rise time, as mentioned before. Good agreement between the simulation and the measurement was found [7].

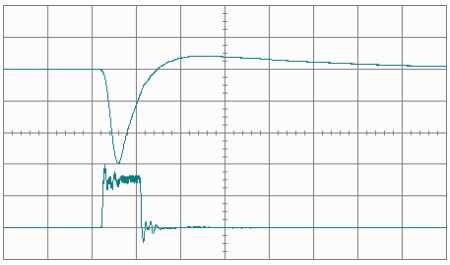

Figure 4: Example of the CARIOCA front-end analog and digital output signals for an input pulse of 72fC, at an input capacitance of about 17pF. The horizontal scale is divided in steps of 50ns and the vertical scale in steps of 200mV.

3.1 Peaking time

Figure 5 shows the peaking time versus the detector capacitance. The measurement shows a peaking time of 14ns at 0pF of input capacitance and a weak dependence with the input capacitance. The discrepancy between measurements and simulation is of about 15%. The discrepancy is probably due to additional parasitics and layout constrains, not considered on the simulation. If a delta input of 1ns rise time is considered, a 2ns reduction on the peaking time is observed.

The expected peaking time for the preamplifier alone is about 8ns. The deterioration of the preamplifier speed is due to the increase of capacitance in the coupling with the discriminator stage.

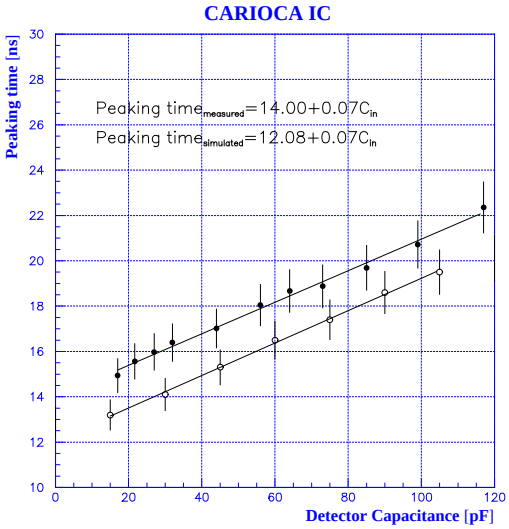

Figure 5: CARIOCA preamplifier peaking time versus the input capacitance for measurement (closed circle) and simulation (open circle). The discrepancy between simulation and measurements is probably due to additional parasitics and layout constrains, not considered on the simulation.

3.2 Linearity

The CARIOCA preamplifier showed good linearity up to 250fC for an input capacitance of 17pF, as shown in Figure 6.

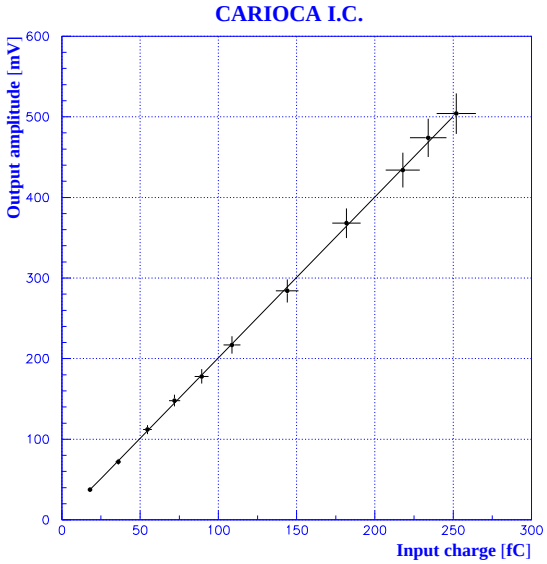

Figure 6: CARIOCA voltage output signal as a function of the input charge, after an amplifier attenuator used on the test board.

3.3 Noise

The noise behavior of current mirror circuits has been previously investigated [8]. In this paper a brief noise calculation is shown considering a weighting function with a bipolar shape, as described in [9]. The results for the parallel, serial and flicker noise are shown in Equation 4, where k is the Boltzman constant, T the absolute temperature, t_{peak} the signal peaking time and C_{in} the input capacitance.

$$ENC_p^2 = I_n^{\,2} \cdot t_{peak}, \quad I_n^{\,2} = \frac{4kT}{R_P}$$

$$\frac{ENC_s^2}{C_{in}^2} = \frac{V_n^{\,2}}{t_{peak}}, \quad V_n^{\,2} = \frac{4kTn\gamma}{g_m}$$

$$ENC_{1/f}^2 = A_f \cdot C_{in}^2$$

Equation 4: Parallel, serial and flicker noise calculation.

The equivalent input noise current is modelled as a noise resistance in parallel to the input is 50KΩ and the gate transconductance of the input transistor g_m is 30mS. The noise characteristics of 0.25µm CMOS technology, discussed in [10], were estimated to n = 1.4, γ = 0.6 and $A_f = 4.10^{-14} V^2/Hz$.

This calculation showed a parallel noise of 416e$^-$ with a noise slope of 35.9e$^-$/pF and an equivalent input noise voltage of 0.7nV/√Hz.

The noise measurements were performed with a drain current of 2mA at the input transistor and a peaking time of 14ns. The results are show in Figure 7 together with the calculations. A parallel noise of 450e^- was measured. The noise slope is about 37.4e^-/pF for input capacitance up to 50pF and 54.4e^-/pF for higher capacitances. The noise slope difference for low and high capacitance values is not fully understood.

For RC-CR filters of 25ns, normally used in several LHC front-end circuits, the noise slope obtained with CARIOCA can be translated to approximately 27e^-/pF for low input capacitances and 40.7e^-/pF for high capacitances.

The total power consumption was measured to be 12mW per channel, including bias circuits, discriminator and LVDS driver, for a supply voltage of 2.5V.

The layout of the circuit has been done with enclosed transistor structure and guard-rings, known to be tolerant to ionizing radiation effects [11]. Because of the additional parasitics and the layout constraints, the same circuit with standard layout would exhibit a better speed and noise performance.

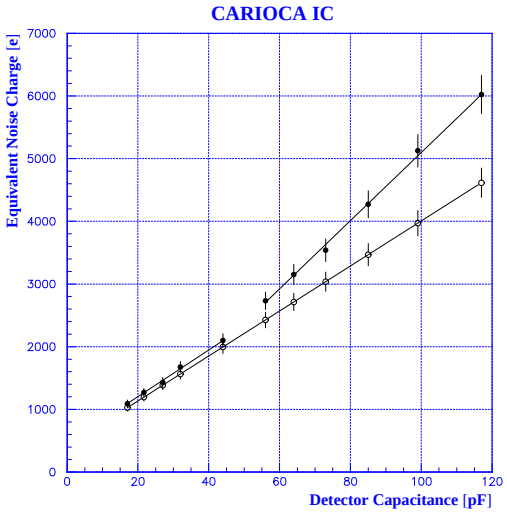

Figure 7: CARIOCA front-end equivalent noise charge measured (closed circle) and calculated (open circle) as a function of the detector capacitance for a peaking time of 14ns. The slope obtained for low capacitance is 37.4e^-/pF and for high capacitance 54.4e^-/pF. Calculations showed a noise slope of 35.9e^-/pF.

4. CONCLUSIONS

We have presented a novel current-mode feedback circuit implemented in a eight-channel binary front end for a fast readout of sensors. The CARIOCA chip has been manufactured in 0.25µm CMOS technology. The tests of the four low gain channels, optimised for 120pF of input capacitance, have shown excellent agreement with the expected results from SPICE simulations.

Noise measurements indicate an excellent performance of the current mode feedback and agree with noise calculations based on the models for 0.25µm CMOS technology.

5. ACKNOWLEDGEMENT

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