The LHCb Trigger

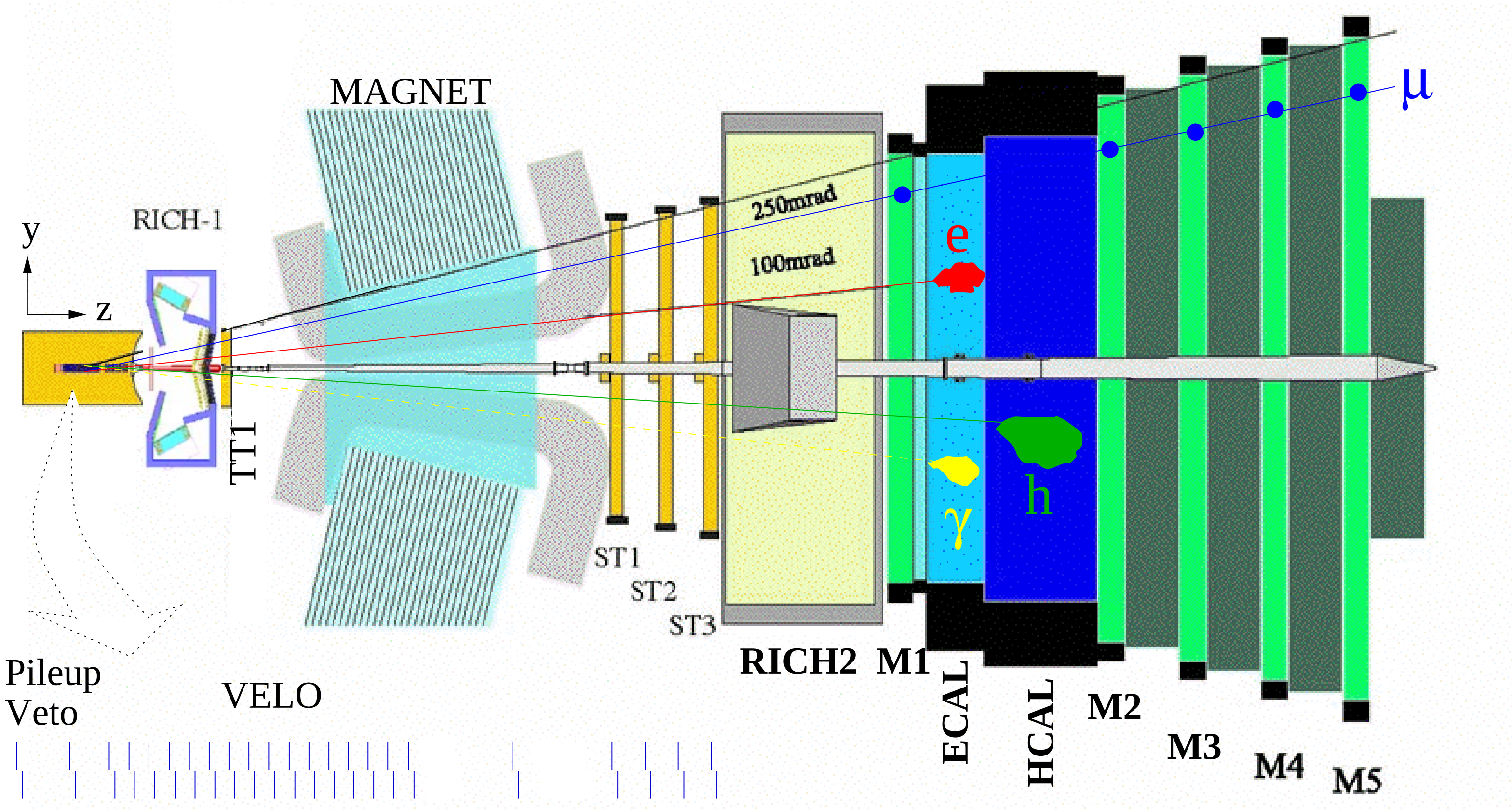
Trigger[1] (tri·gəɹ). Forms: *α*. 7–8 (9 *dial.*) tricker, (7 trycker); *β*. 8 triger, 7– trigger. [In form *tricker*, ad. Du. *trekker* a trigger, f. *trekken* to pull: see TREK. The form *trigger* occurs in 1660, but *tricker* remained the usual form down to *c* 1750, and is still in dialect use from Scotland to the English Midlands.]

1. A movable catch or lever the pulling or pressing of which releases a detent or spring, and sets some force or mechanism in action, *e.g.* springs a trap.

The Compact Edition of the Oxford English Dictionary
Oxford University Press, Twenty-Third edition, January 1984

- LHCb&Trigger Overview
- First Level Trigger (L0)
  - Single interaction/x-ing selection by Pile-up Veto
  - Highest p$_T$ μ's reconstruction by Muon Trigger
  - Highest E$_T$ e,γ,π^0 or h reconstruction by Calorimeter Trigger
- Second Level Trigger (L1)
  - Full track reconstruction in Si Vertex Locator
  - Matching of tracks with L0 leptons and hadrons
  - Rough momentum measurement of selected tracks
- Higher Trigger Levels (L2,L3)
  - Confirmation of L1 with better dp/p
  - Full reconstruction

LHCb Trigger Detectors Overview



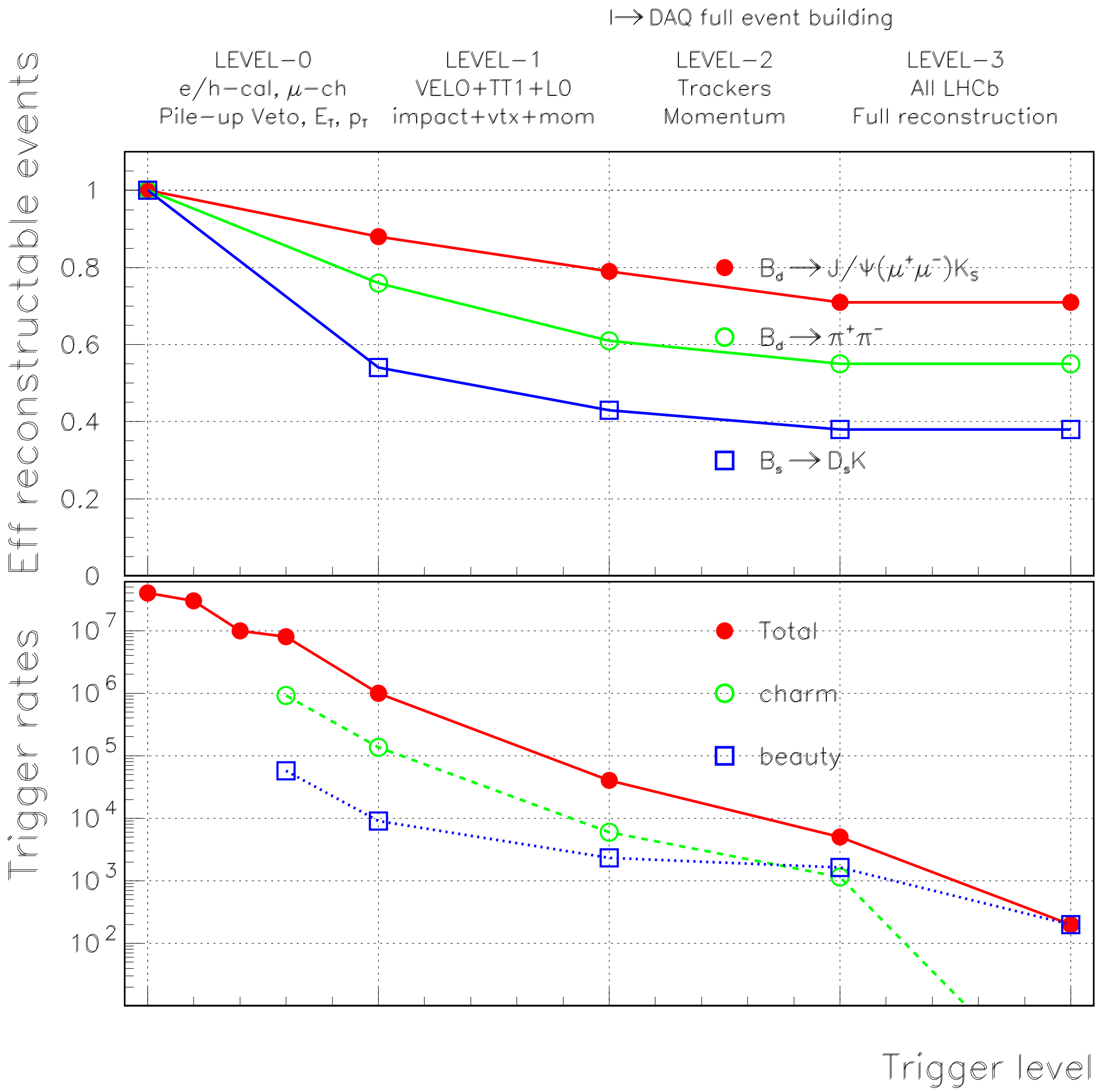
L0 Input rate 40 MHz

- Pile-up Veto: 2 Si-discs, 2048 binary channels.
- Scintillating Pad Detector: 5952 cells, 1-bit/cell.
- Preshower: scintillator, 5952 cells, 1-bit/cell.
- Electromagnetic Cal.: shashlik, 5952 cells, 8-bit E_T.
- Hadron Cal.: iron/scintillating tiles, 1468 cells, 8-bit E_T.
- Muon Chambers: MWPC&RPC, 120k physical channels $\rightarrow$ 26k "trigger" channels.

L1 Input rate 1 MHz

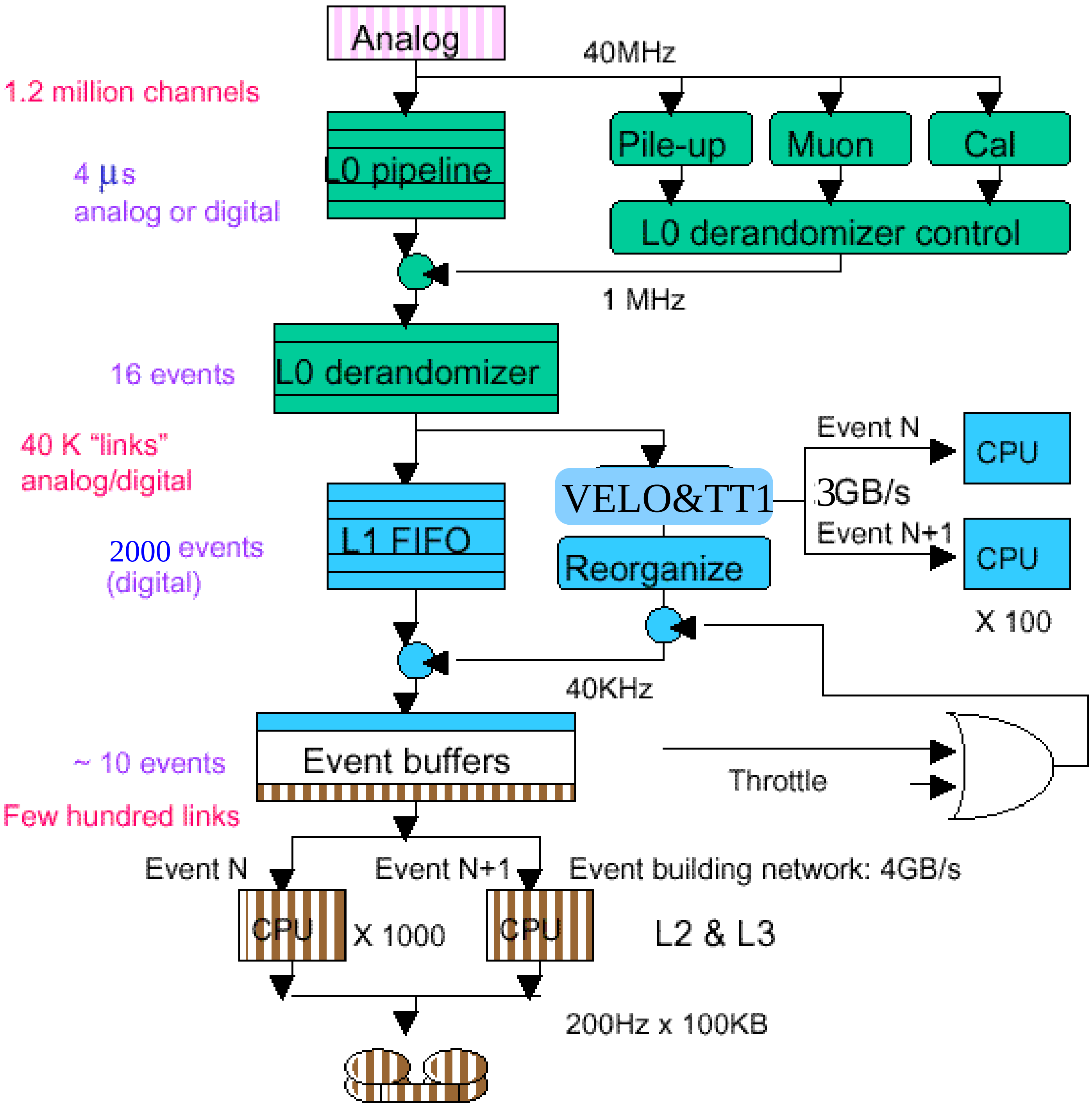
- L0 summary info.
- VELO: 220μm thick Si, 170k binary channels.
- TT1 : 400-500 μm thick Si, $\sim$150k binary channels.

LHCb Trigger Rates Overview



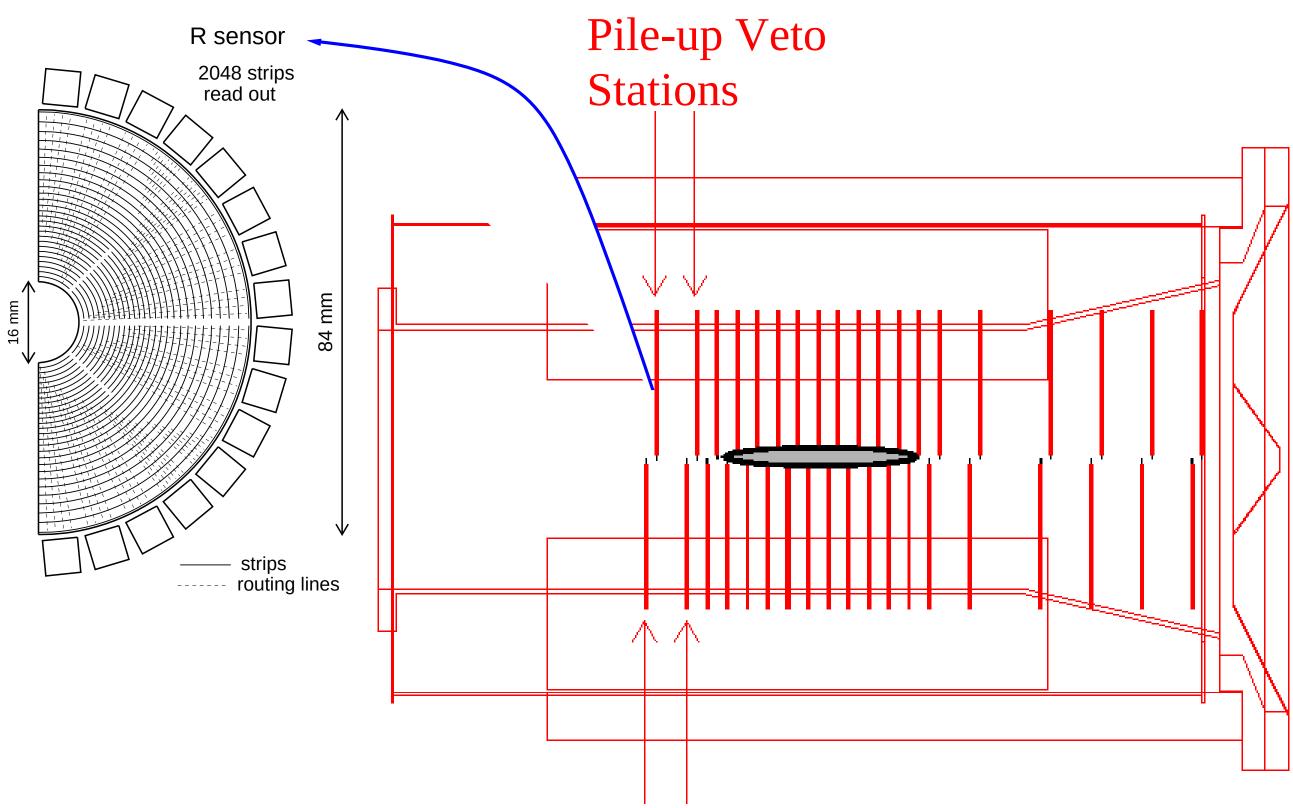
- 30 MHz of x-ings have both bunches filled
- Wanted: single interactions: run at $L{=}2{\times}10^{32}$ cm^{-1}s^{-1}.
- Of 80 mb non-elastic cross-section, $\sim$60 mb is "visible"$\rightarrow\sim$10 MHz of x-ings with "visible" interactions.
- 8 (1.6) MHz of single (double) interactions/x-ing
- Pile-up Veto reduces rate to $\sim$ 8 MHz
- L0 highest E$_T$ μ,e,γ,π^0 and h triggers reduce rate to 1 MHz
- L1 Trigger reduces rate to 40 kHz
- L2(3) Trigger reduces rate to 5 (0.2) kHz

Front End Electronics Overview



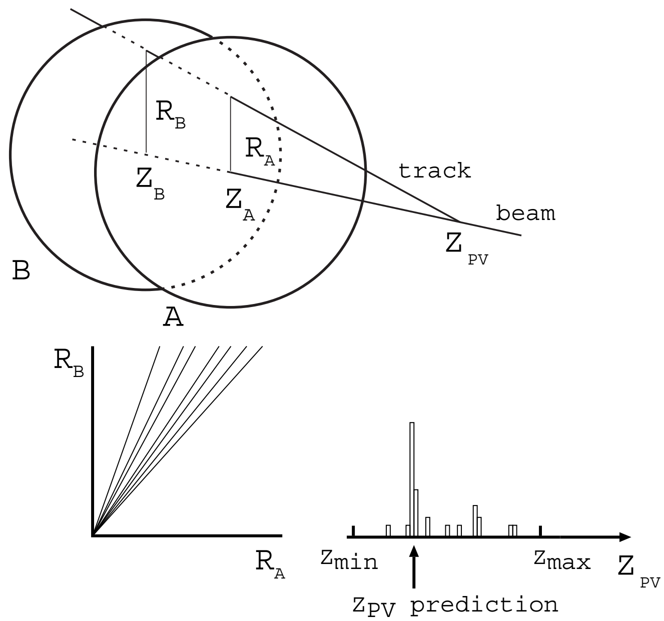
L0 Pile-up Veto Detector

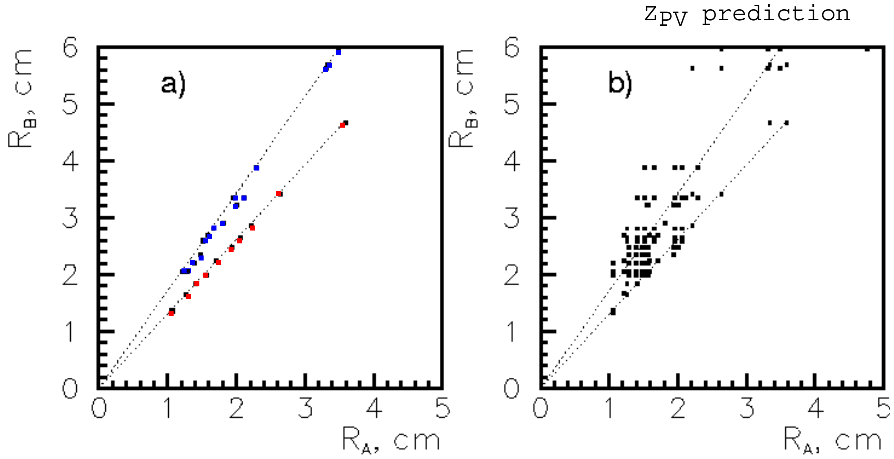
- two Si discs upstream of interaction cigar
- coverage -4.2$< \eta <$-2.9
- same sensors as used for VELO (see talk Ulrich Parzefall)
- .OR. of 4 neighbouring strips (performed in Beetle chip)
- Re-group data in 90° sectors reduces total number of 8192 strips to 1280 channels.

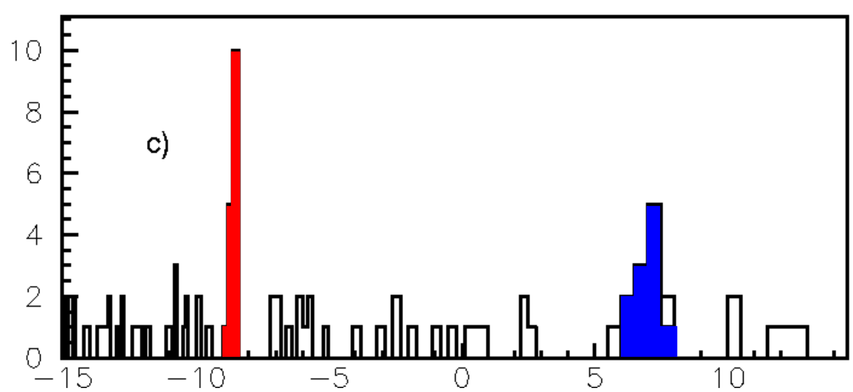


L0 Pile-up Veto Algorithm

$$\frac{R_B}{R_A} = \frac{z_B - z_{PV}}{z_A - z_{PV}} \quad (1)$$





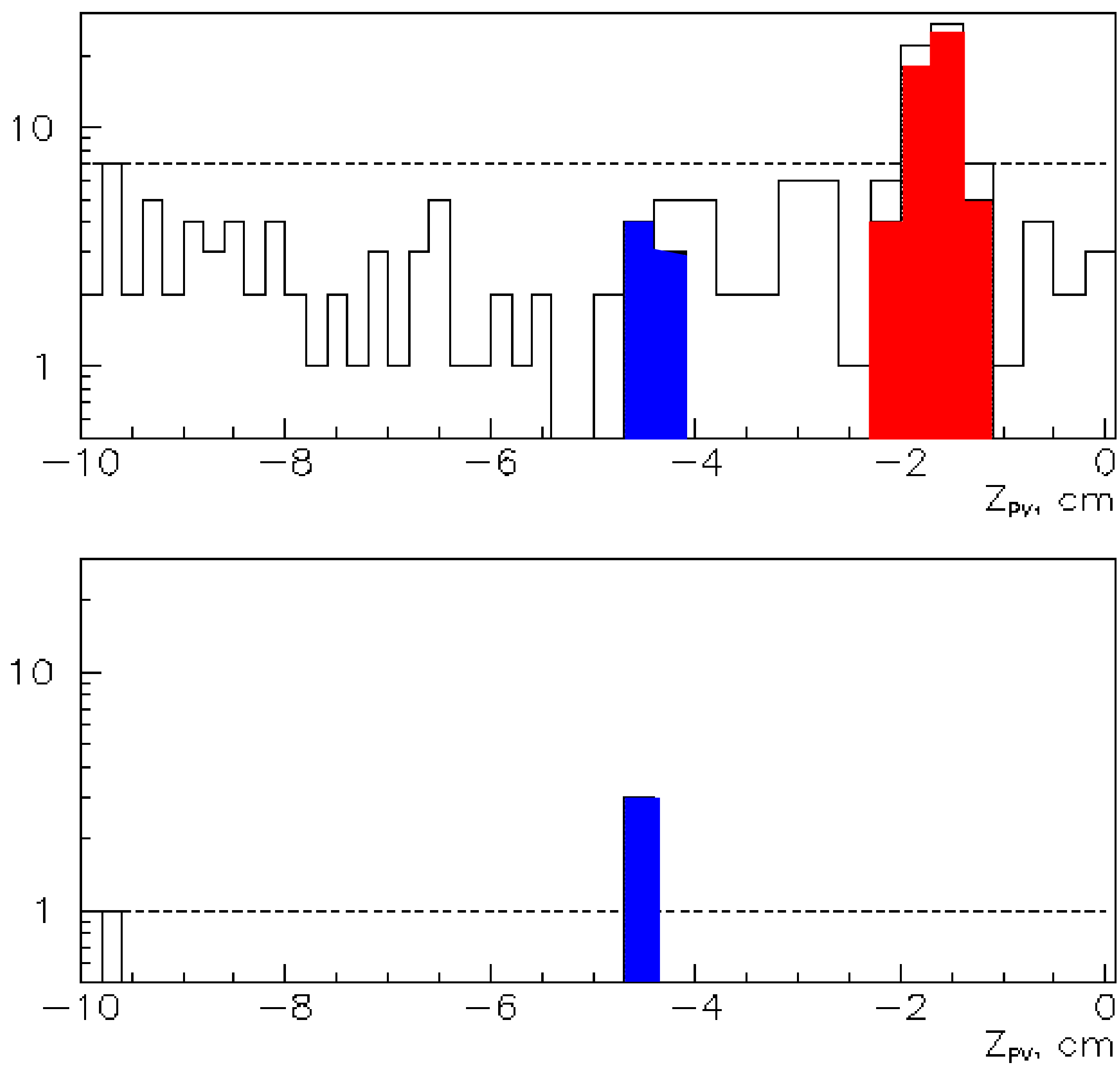


The whole algorithm fits into 4 large FPGAs.

L0 Pile-up Veto Algorithm

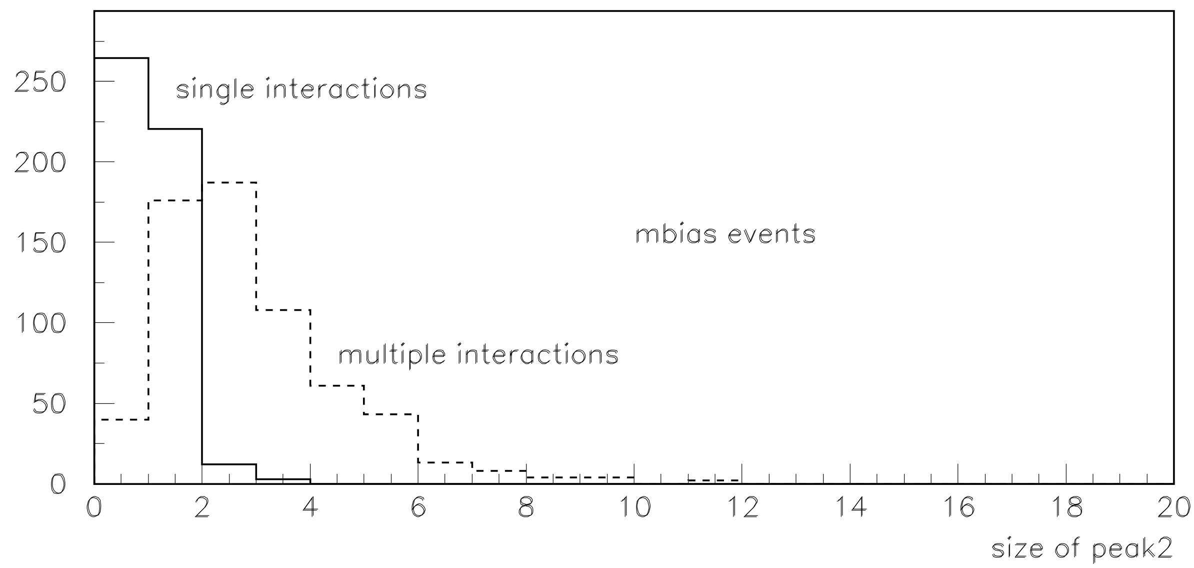
If multiplicty of two interactions is comparible “easy”.
To be able to indentify small multiplicity vertex in “noise” of large multiplicity vertex: apply masking scheme.

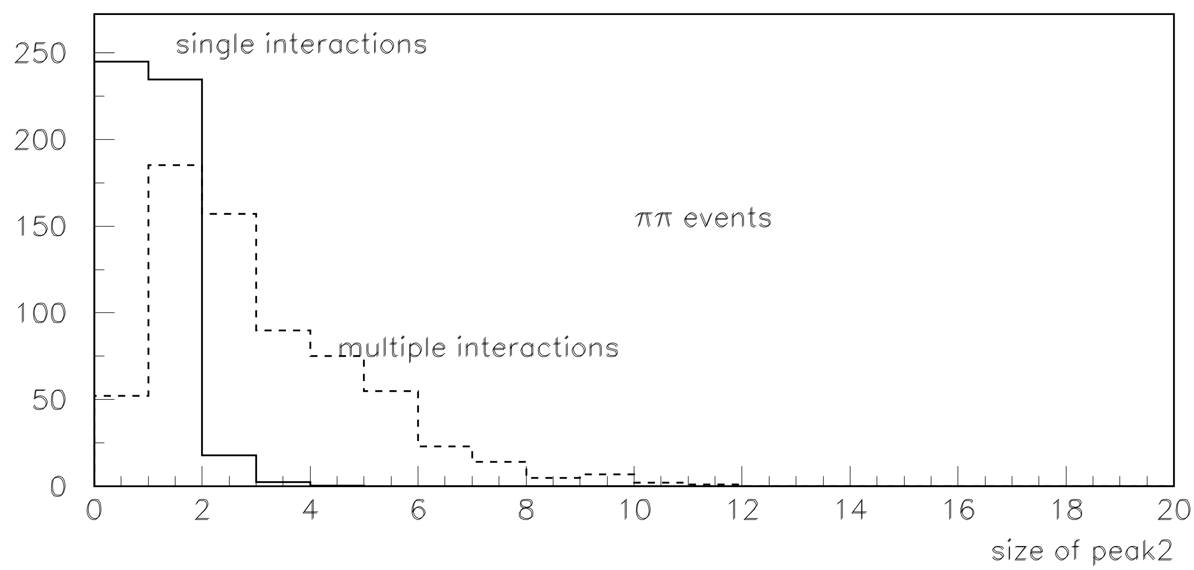
- Project diagonals
- Identify largest peak above threshold
- Remove all hits contributing to this peak
- Project diagonals of remaining hits
- Look for peak over threshold



Pile-up Veto Performance

Height of peak after masking:



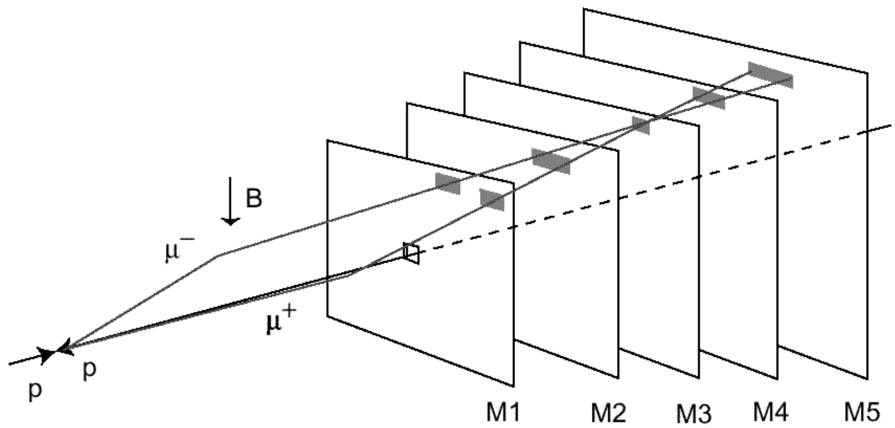


Some typical numbers on performance:

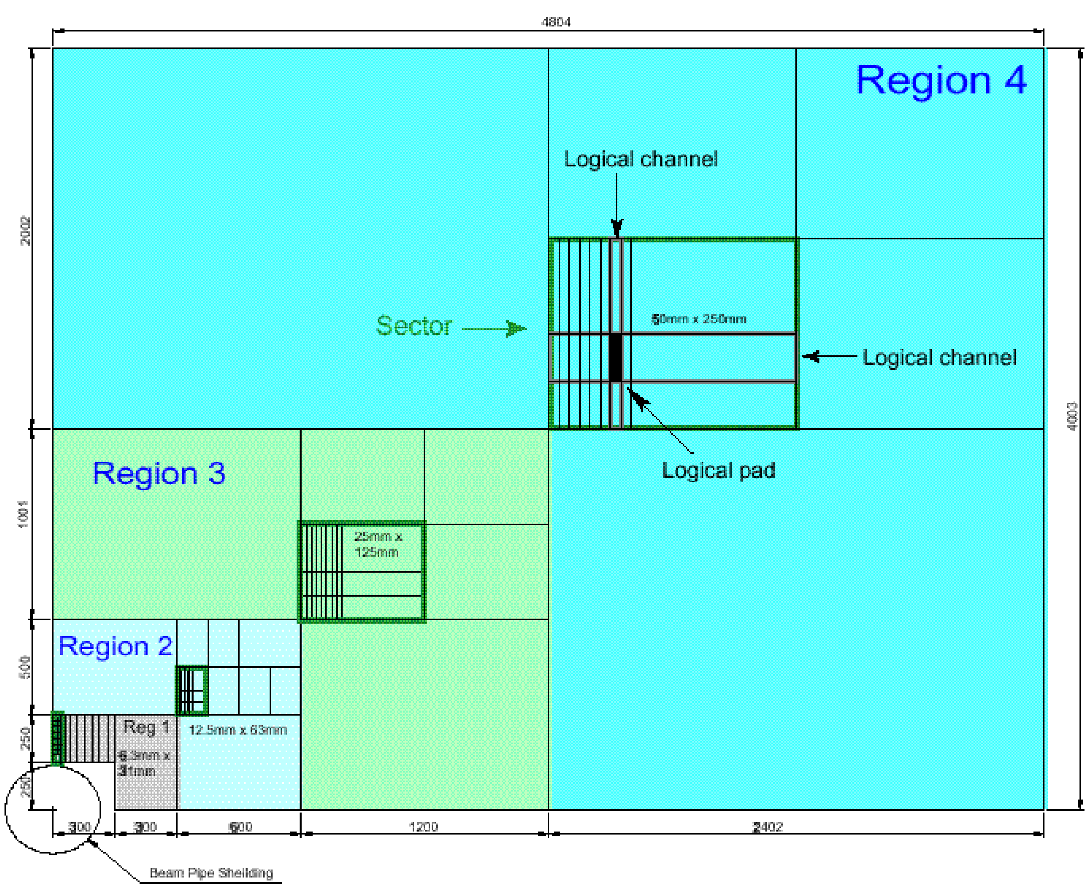
- Does not veto 95% of single interactions in signal events.
- Vetoes 60% of double interactions with the highest multiplicity.

L0: μ Trigger

Look for straight lines in pads in the μ-chambers

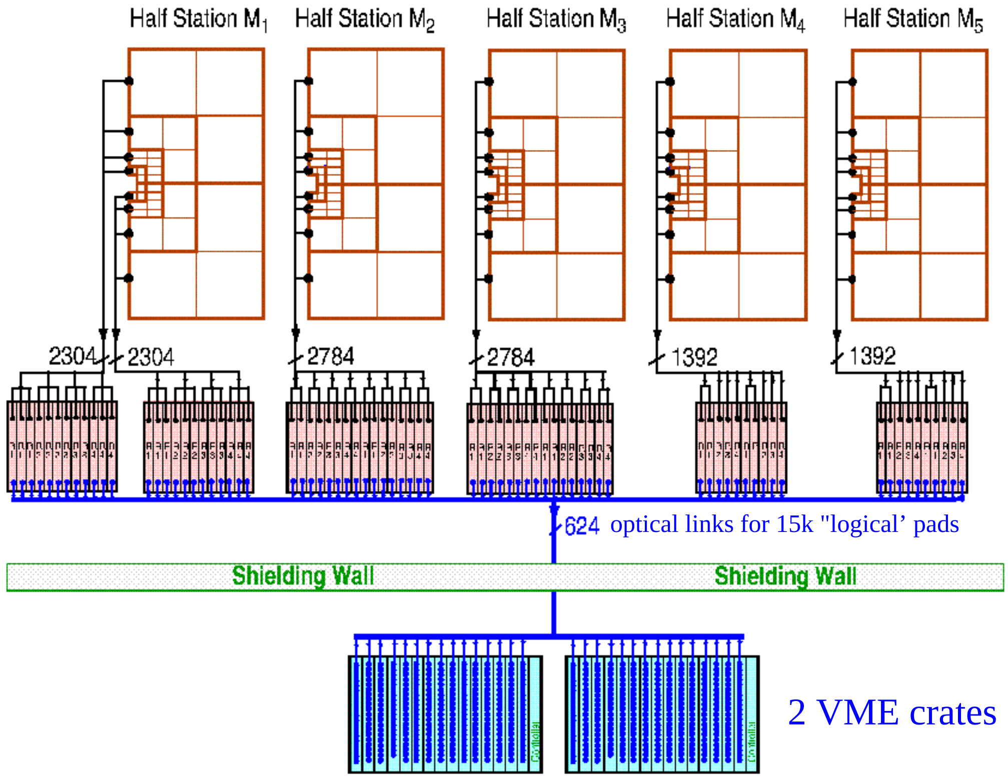


- MWPC (54%) and RPC (if rate<1 kHz/cm^2).
- 120k pads and strips. Eff$>$ 99% by .OR. 2 layers per station.
- Combined strips→ 26k pads. Size: 1×2.5 cm^2 (M1-inner) to 16×20 cm^2 (M5-outer)
- All pads are projective in Y



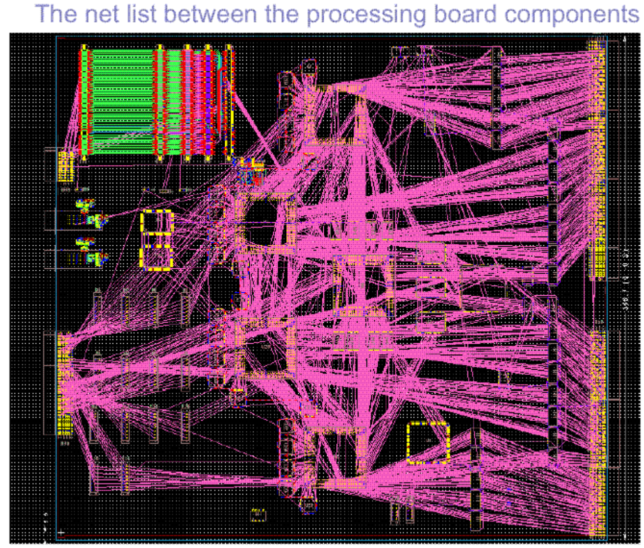
L0: μ Trigger schematic

Half the μ-Trigger system

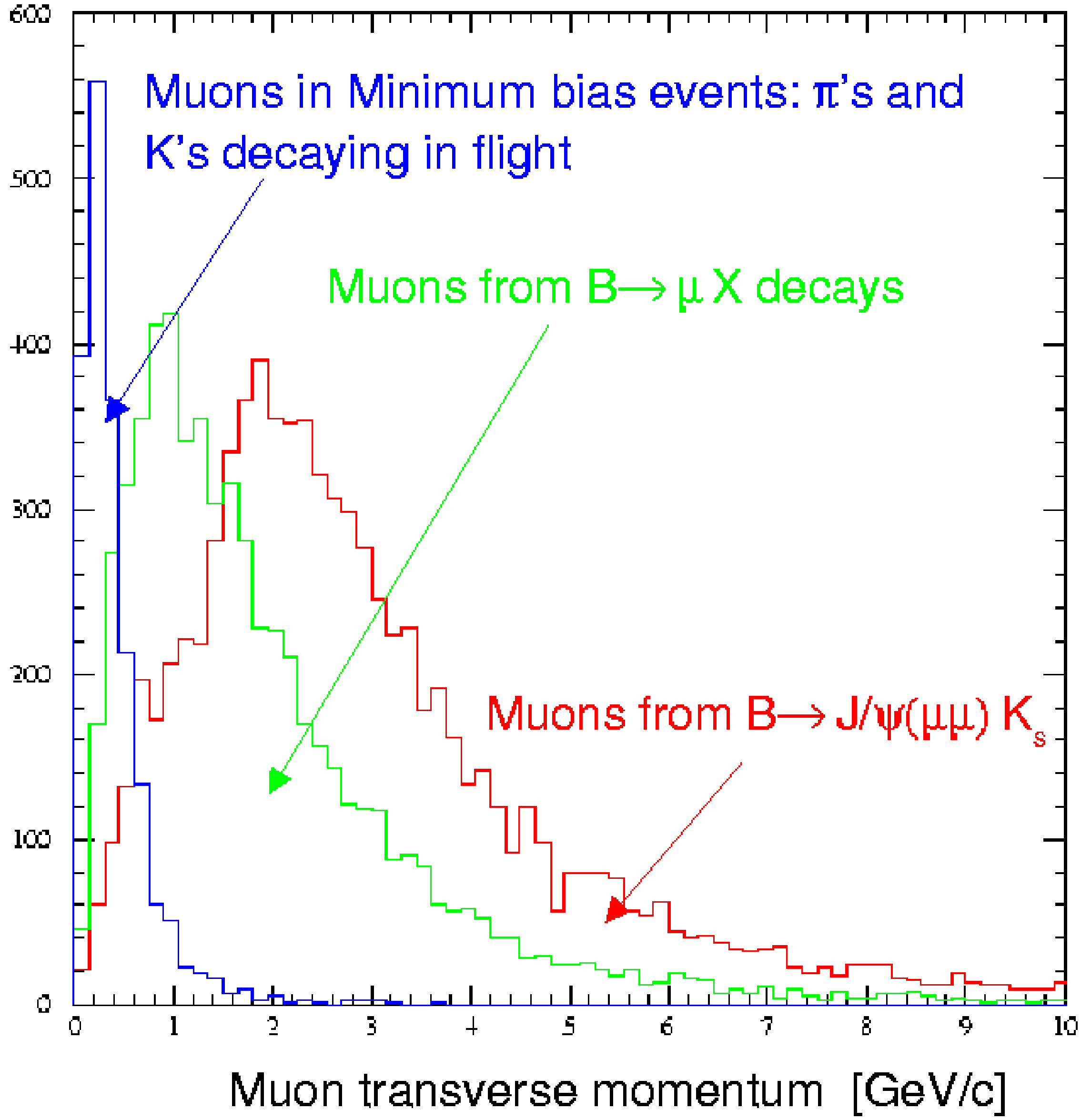


- Optical patch-panel to collect matching pads together.
- Routing nightmare: 14500 pins/VME board.
- One VME crate per quarter.
- Two largest p_T μ's per quarter.
- Fully synchronous.
- Latency $\sim$1 μs.

The net list between the processing board components



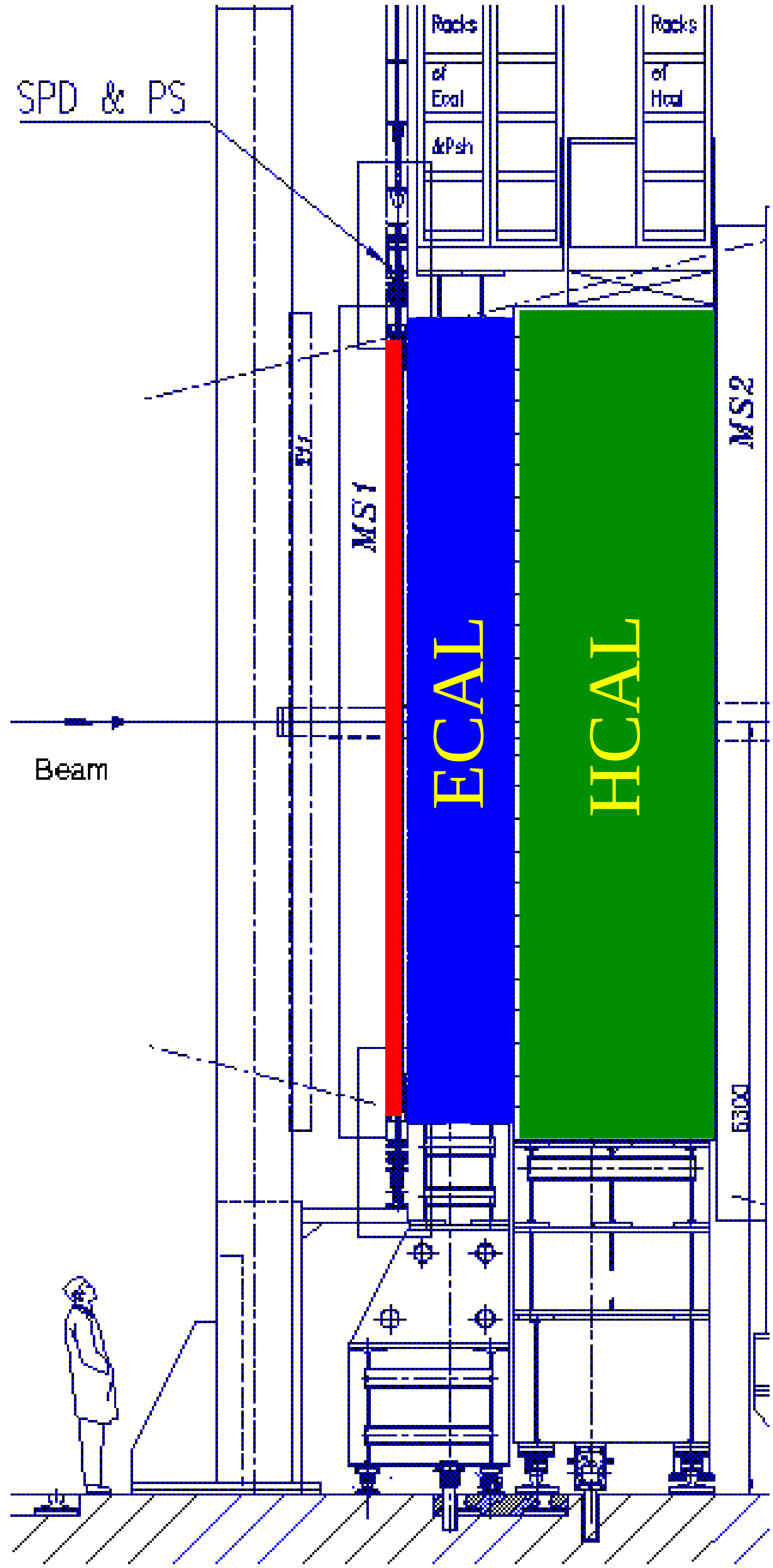
L0: μ Trigger Performance



- Efficiency B$_d \rightarrow \psi K_S \sim 85\%$.
- Efficiency B$\rightarrow \mu X \sim 55\%$
- Algorithm very robust against increased background or chamber inefficiency.
- LHC μ-halo: negligible loss under normal condition.

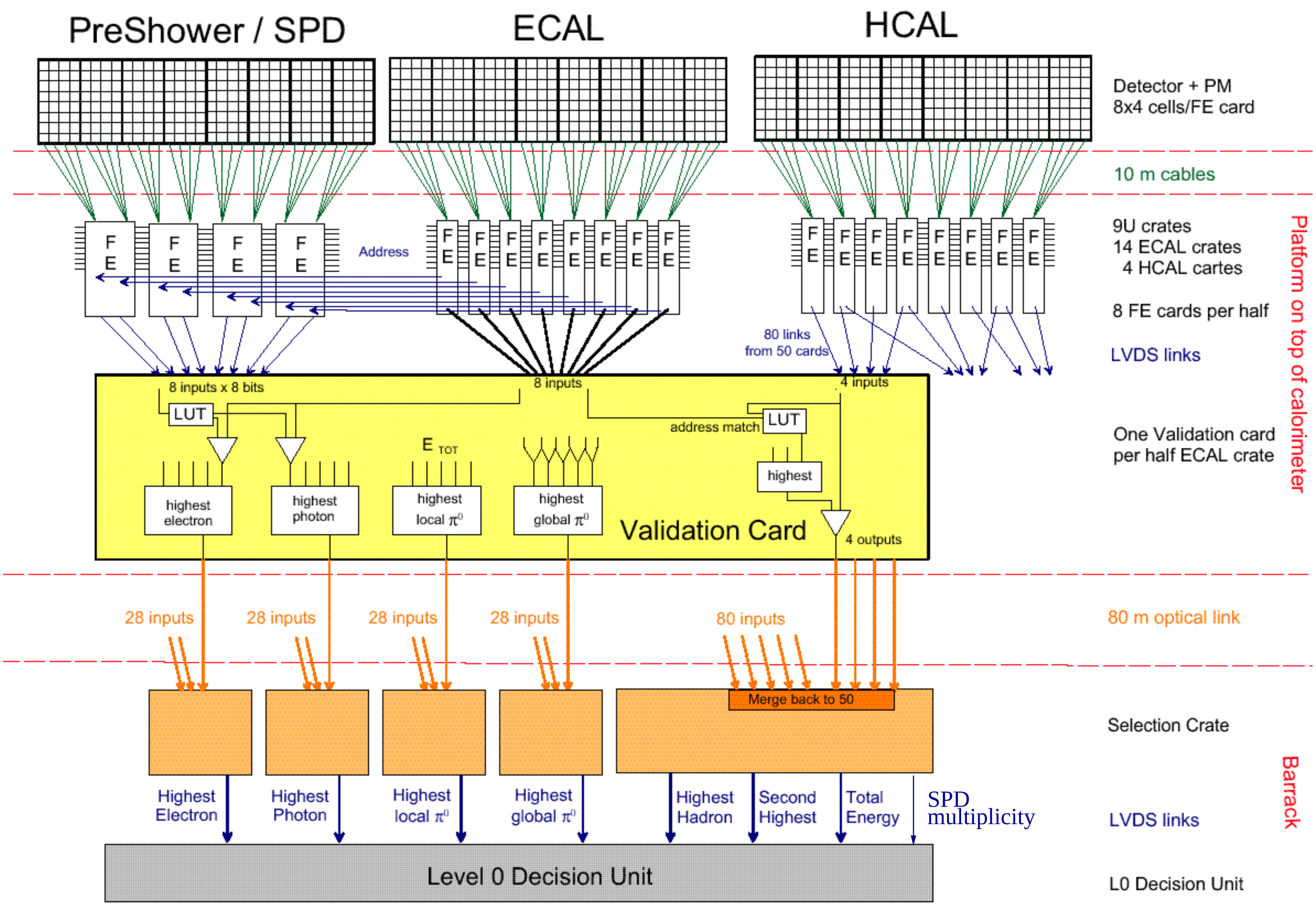
L0: Calorimeter Trigger Detectors

- Scintillating Pad Detector: 5952 cells, 1-bit/cell.
- Preshower: scintillator, 5952 cells, 1-bit/cell, $2X_0$
- Electromagnetic-Cal.: shashlik, 5952 cells, 8-bit E_T, $25X_0$
- Hadron-Cal.: iron/scintillating tiles, 1468 cells, 8-bit E_T, $5.6\lambda_I$



L0: Calorimeter Trigger

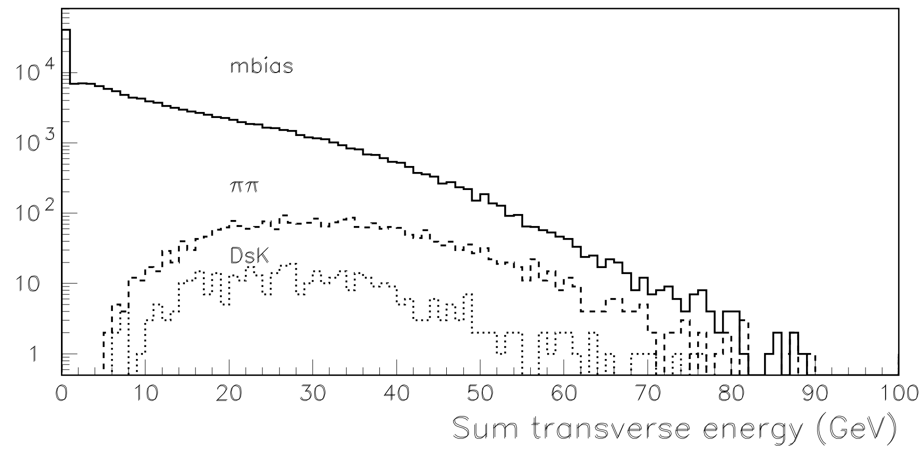
- Add E_T of 2×2 clusters
- Collect largest (&second largest for h) clusters
- Distinguish between γ and e with SPD
- Distinguish between MIP and e with PreShower
- Add ECAL E_T to largest HCAL clusters behind it
- Add up all E_T of all clusters
- Count number of SPD cells with a hit

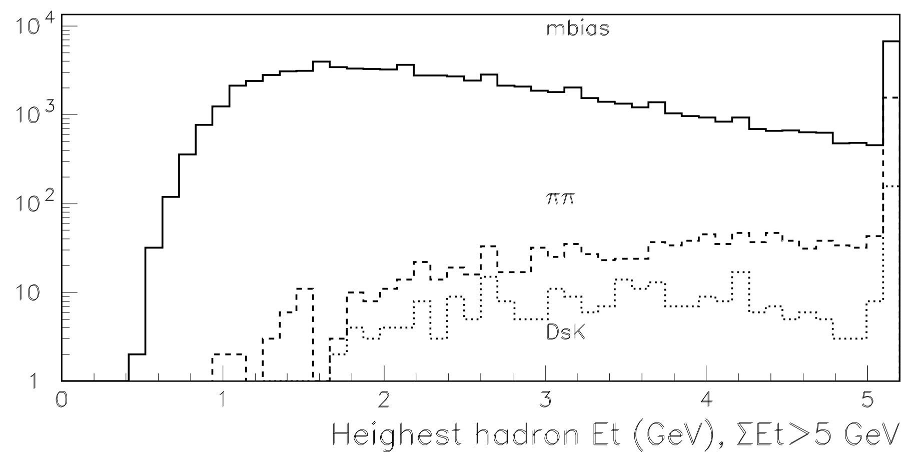


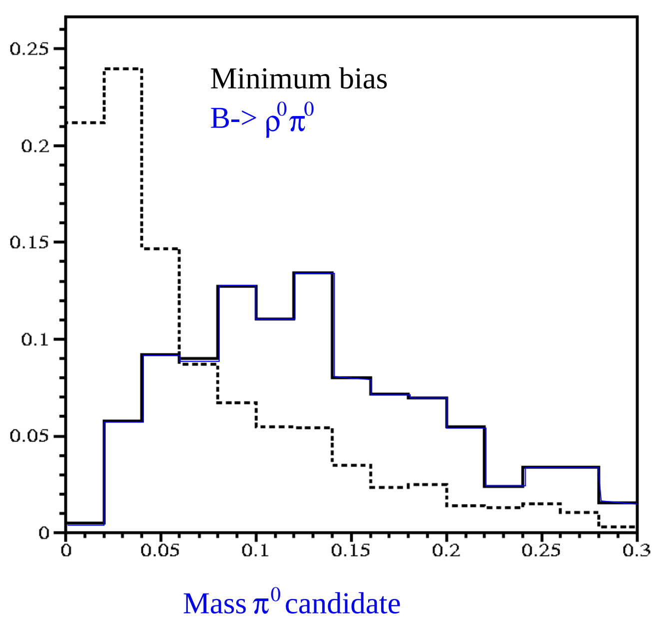
Fully synchronous architecture.

L0: Calorimeter Trigger Performance

- Use ΣE_T to reject diffractive/elastic (μ-halo) events, typical threshold 5 GeV.
- Highest E_T hadron for hadronic channels, typical threshold 3-4 GeV

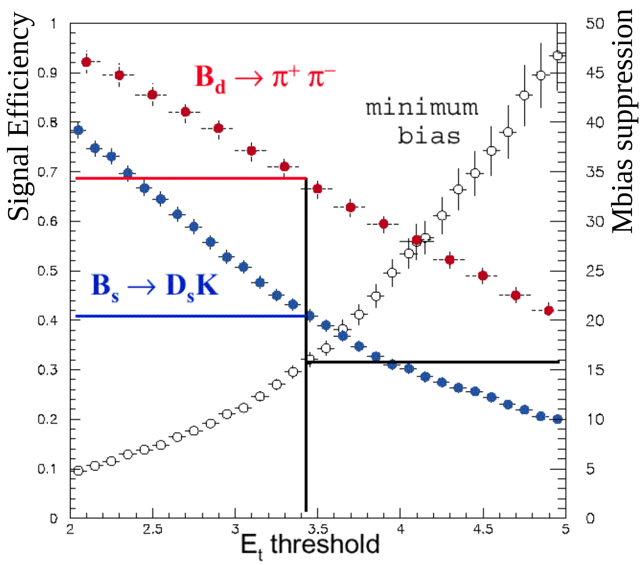


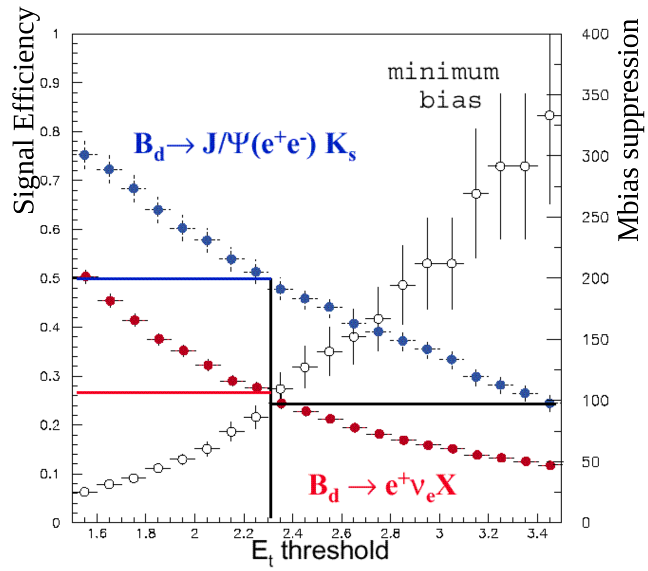




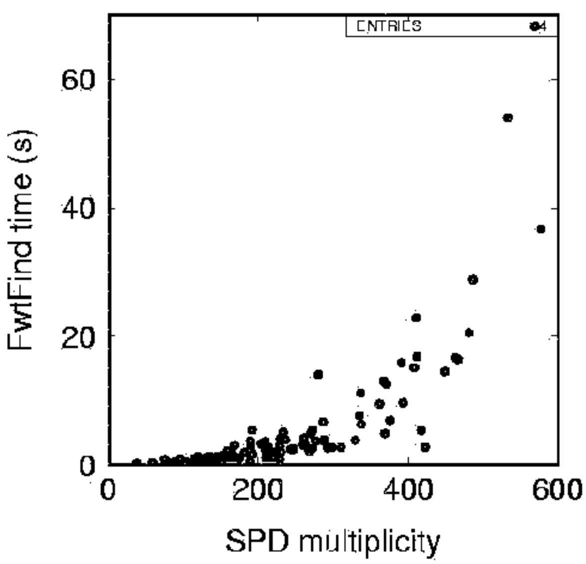
- π^0 trigger

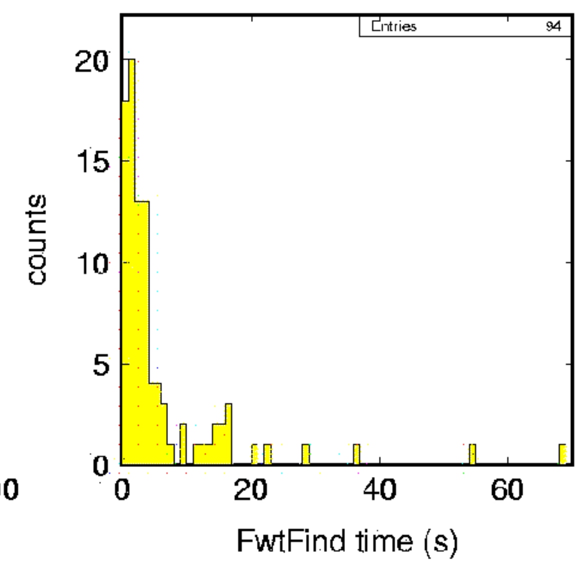
L0: Calorimeter Trigger Performance





- Eff hadron channels 40-70% for 60% of L0-BW.
- Eff B$_d \to \psi(ee)K^0_S$ around 50% for 10% of L0-BW.



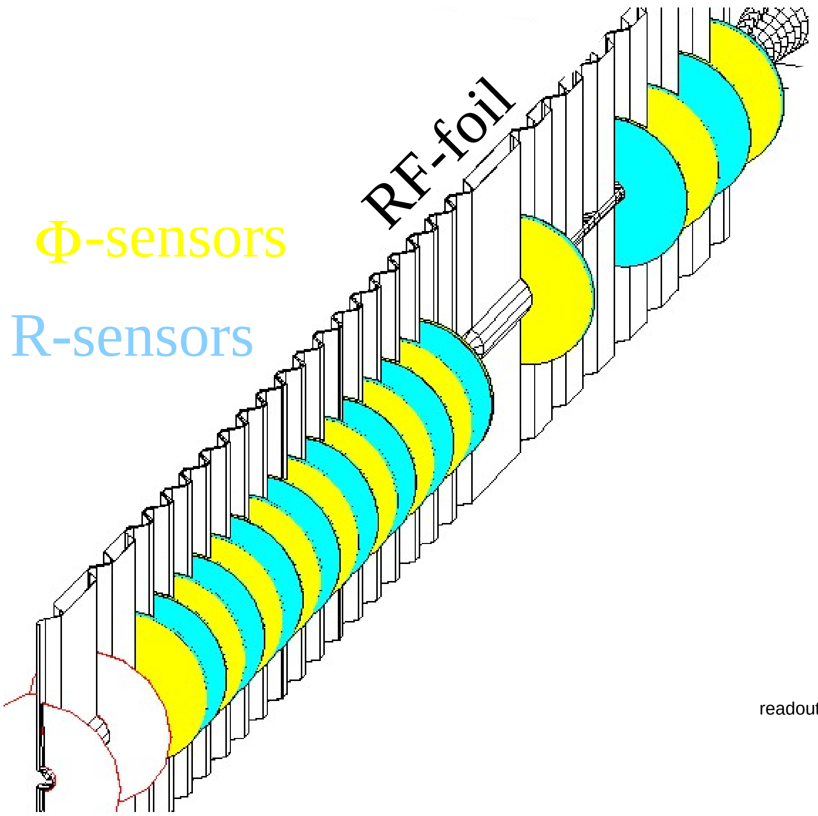


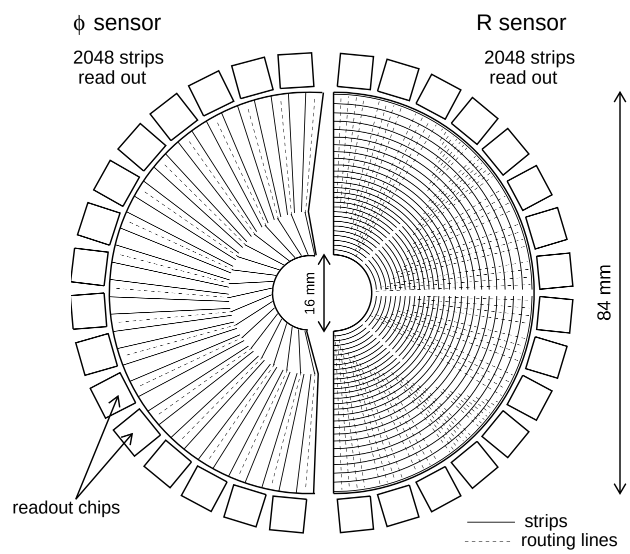
- Optionally reject "large" events at the earliest (L0) trigger using SPD information.

L1-Trigger: L0 summary data & VELO data

L0 summary information:

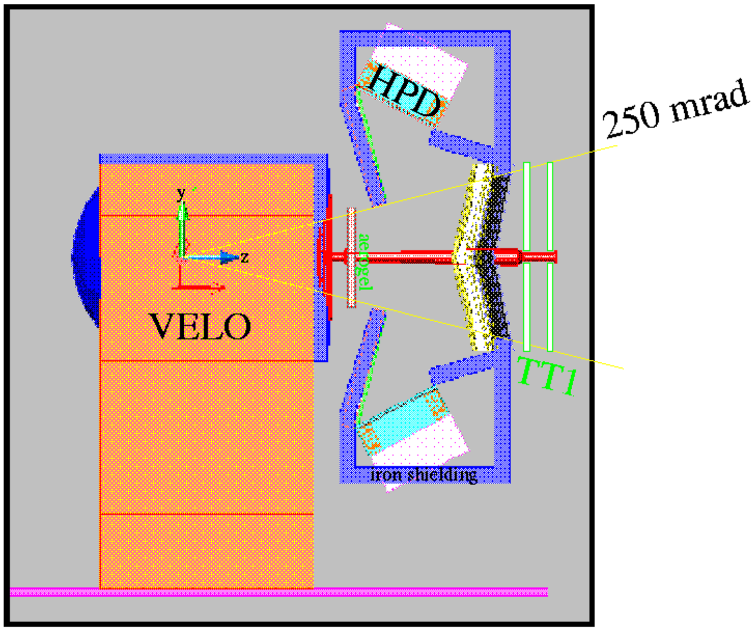
- From cal: e,$\gamma, \pi_G^0, \pi_L^0, h_1, h_2$ and ΣE_T
- ΣE_T of previous and next two crossings.
- Three largest p$_T$ μ's from μ-trigger
- From Pile-up Veto: height of second peak, z-primary vertex.



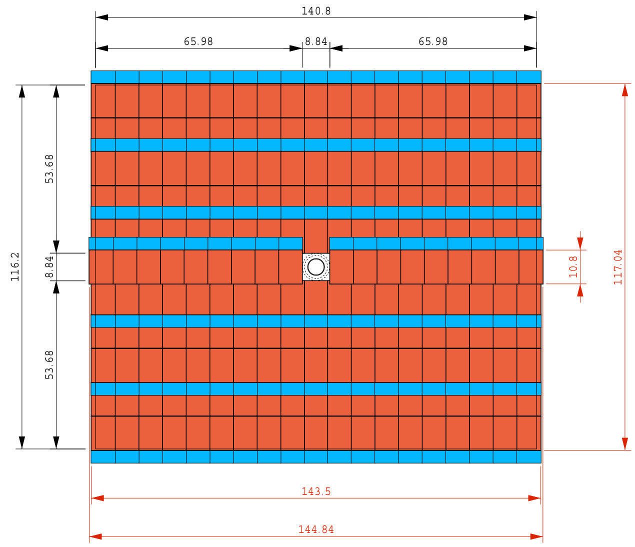


- VELO: 220μm thick Si, 170k binary channels for Trigger.
- Each station is a sandwidch of a R and Φ-sensor.
- Φ-sensors have a 10-20° stereo angle.
- Sensitive Si-area starts 8 mm from the centre of the beam
- Whole detector mounted on XY-table to centre whole VELO on beam-line.
- Roughly 1200 clusters per event.

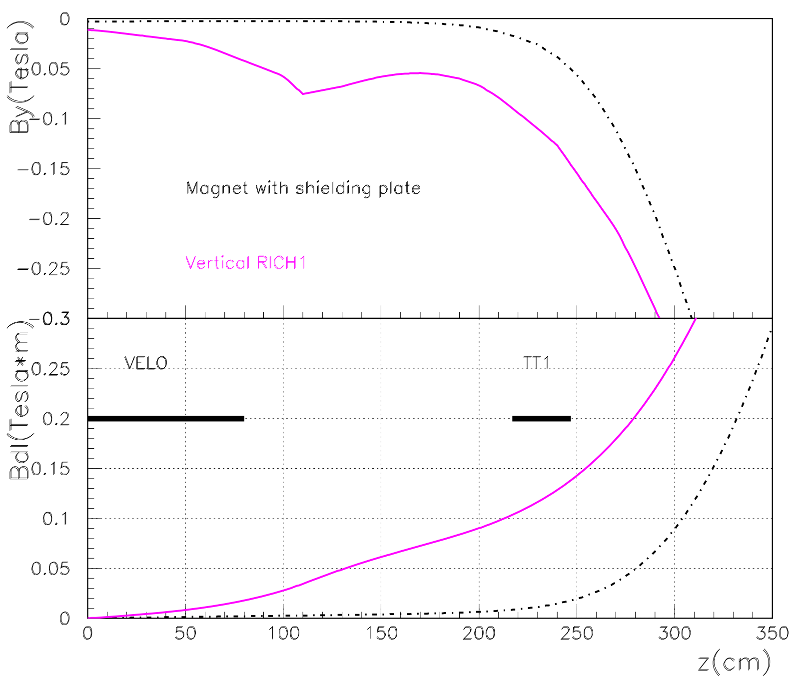
L1: TT1 data and dp/p



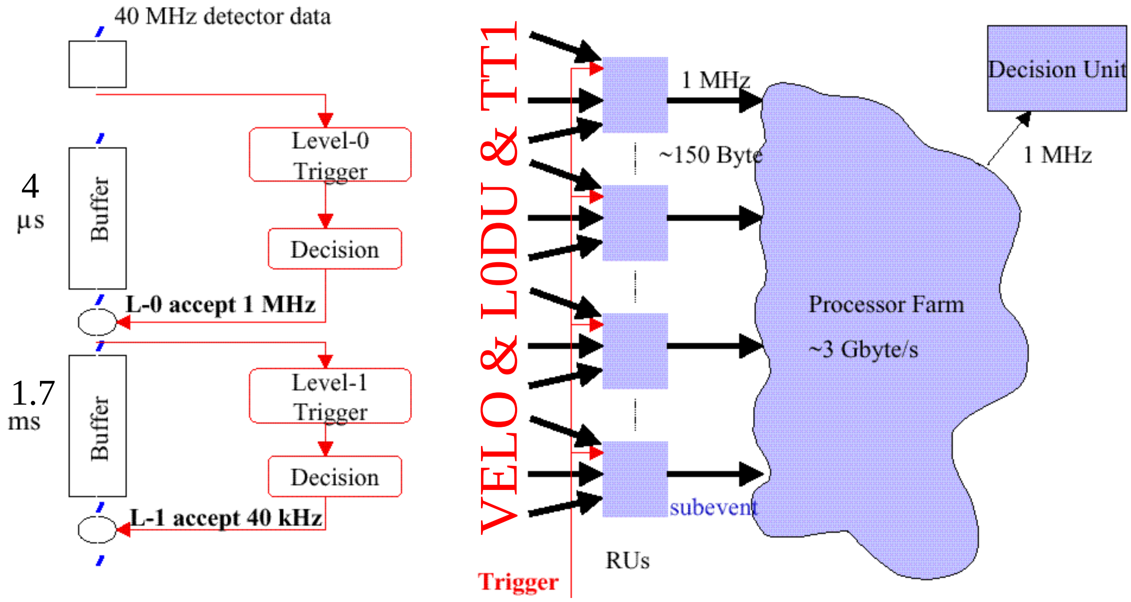
New: RICH1 arrangement



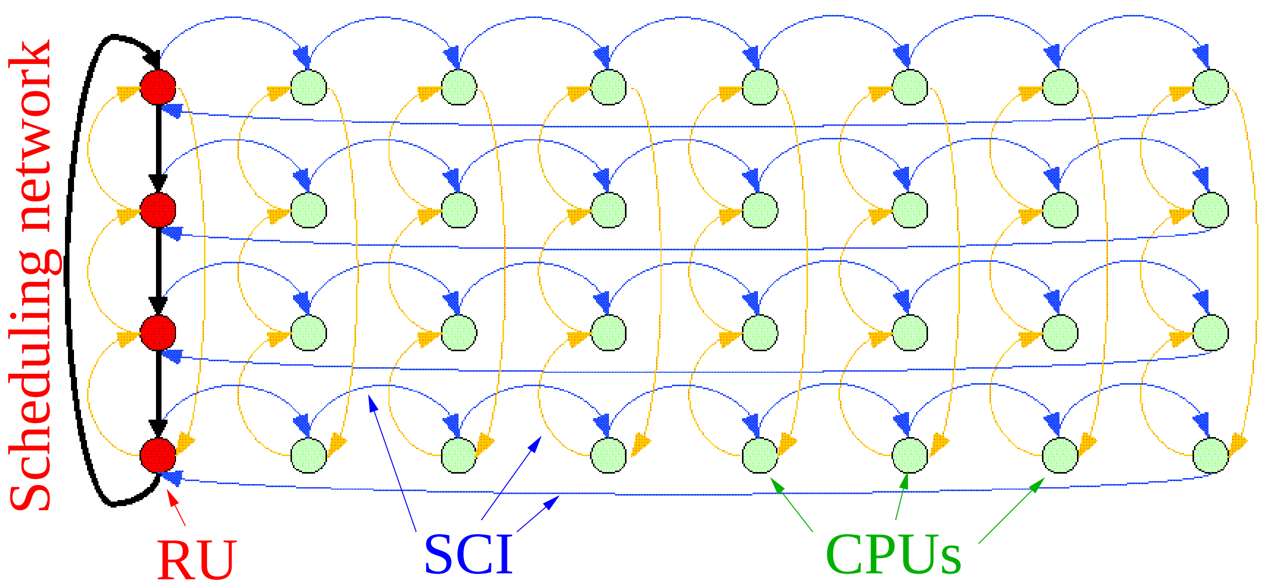
New: 4-layer Silicon station (TT1) 400-500 μm thick Si, ~150k binary channels. 350 cluster per event



L1: implementation

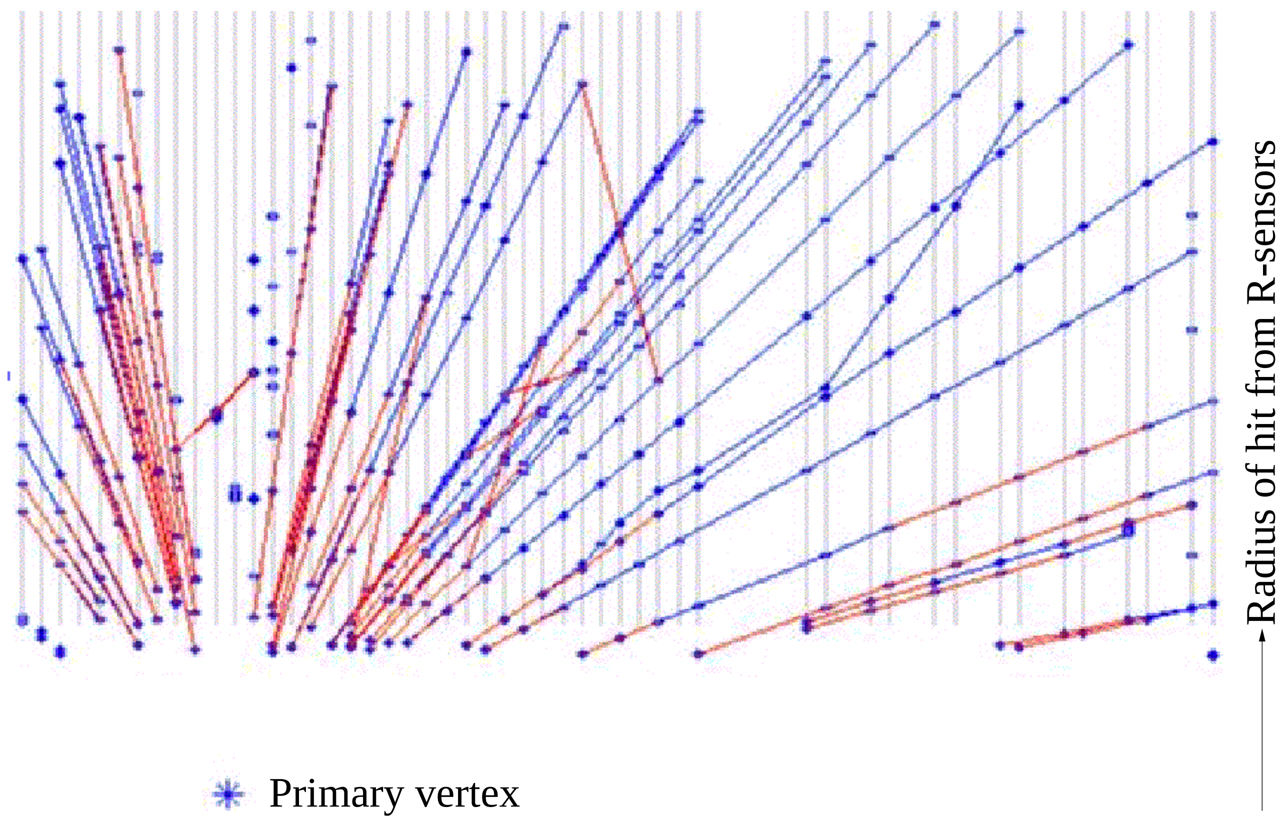


- Data size ~3-4 kbyte/event
- L0-rate: 1 MHz
- Use scheduler for event building traffic
- 2D-torus of CPUs with Scalable Coherent Interface
- Reached >1.2 MHz in prototype set-up.

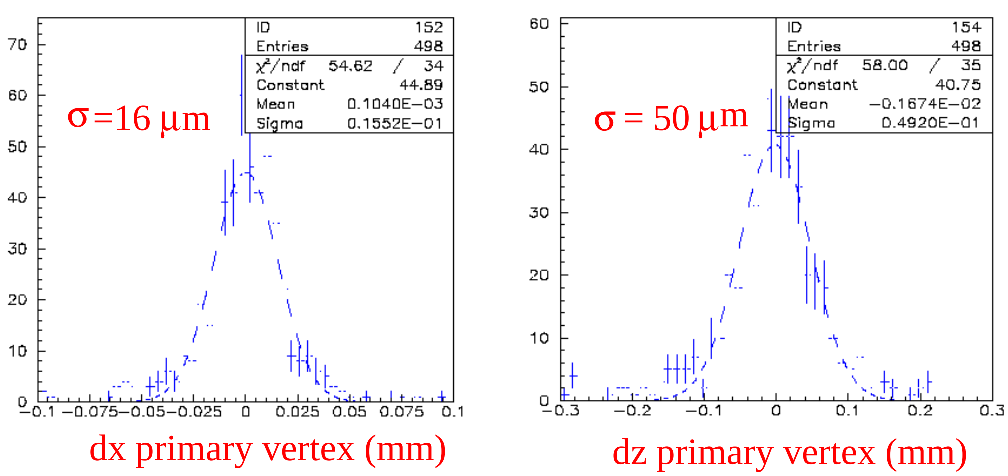


L1-algorithm: track reconstruction

- 2D tracking in VELO: $\sim 95\%$ eff for B-tracks
- 1.7 ms on 2001 CPU $\rightarrow$ need $\sim$300 CPUs in 2007.

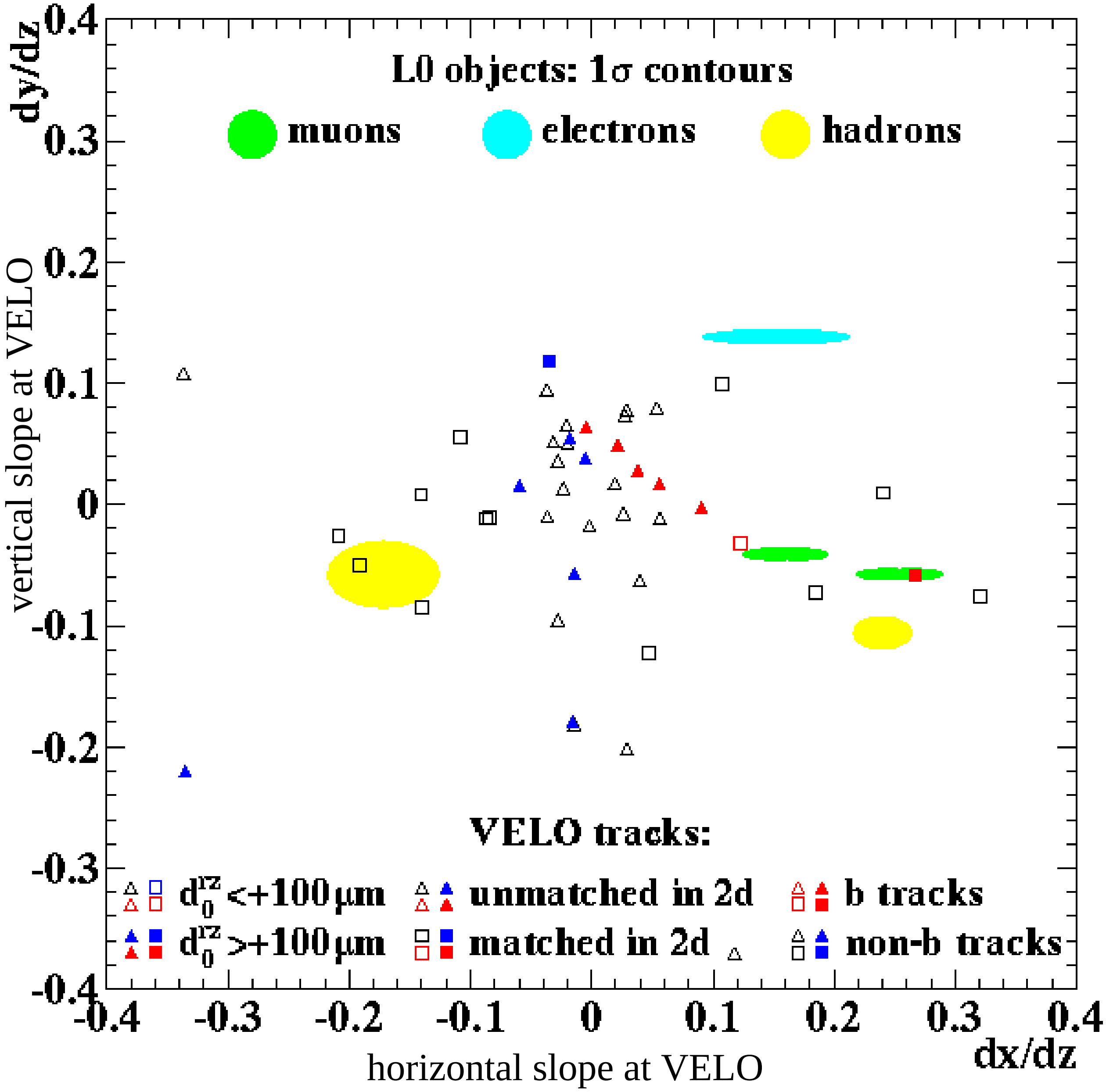


- Find primary vertex.
- Note: most of impact parameter info in rz-projection.



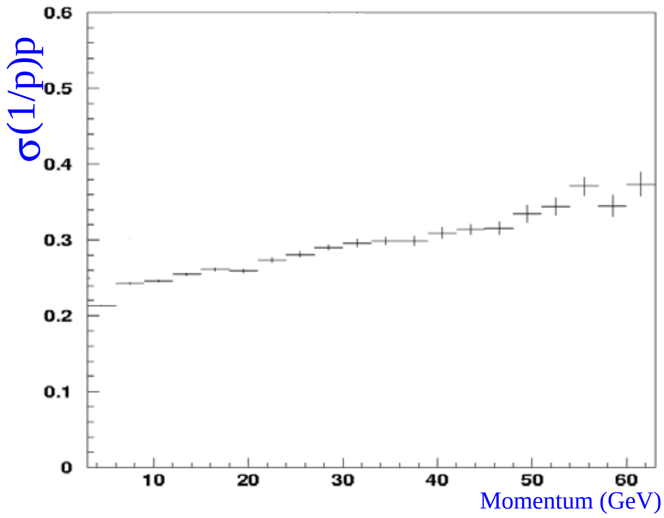
L1-algorithm: VELO→L0

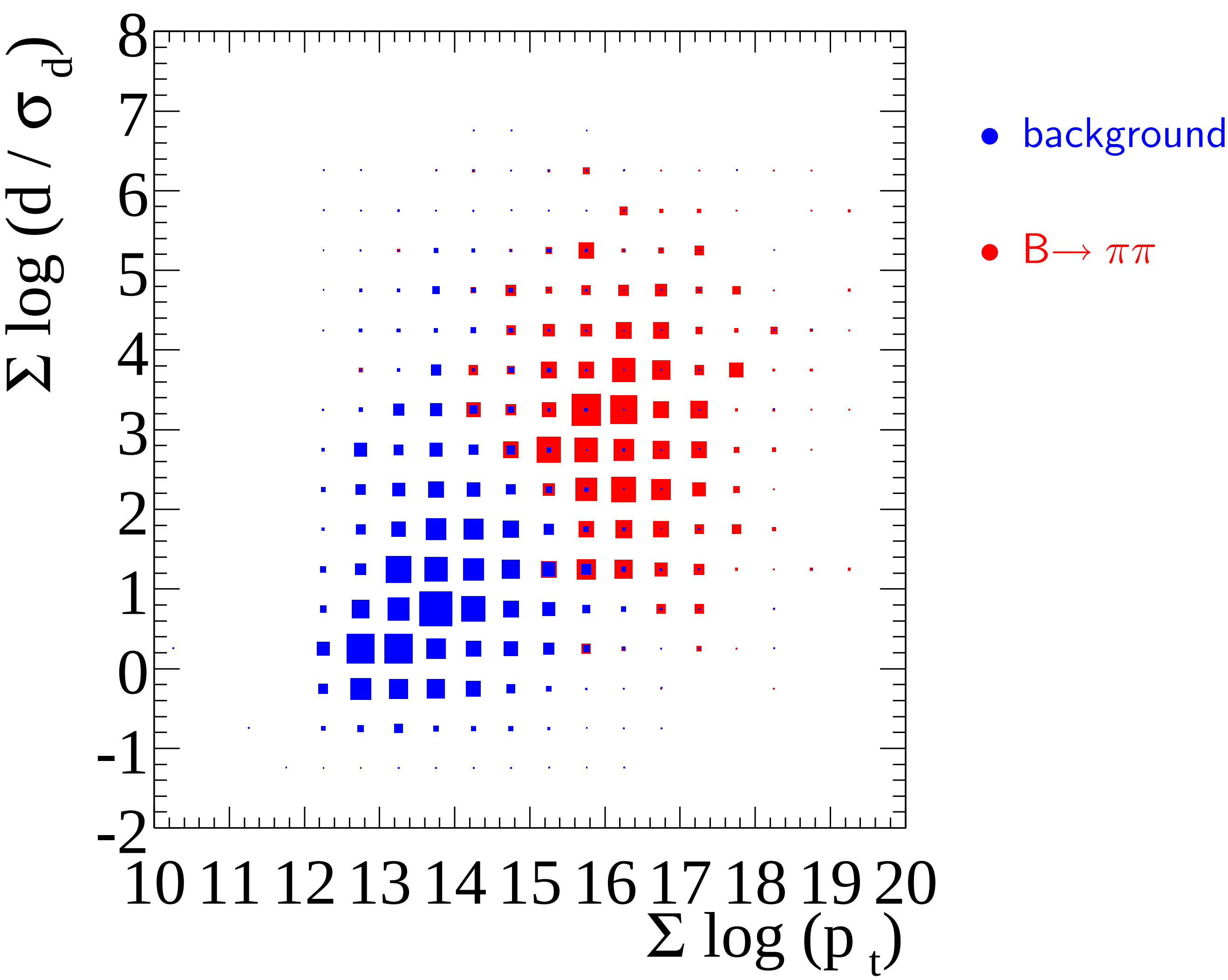
- VELO-tracks→L0 e,h,μ
- $\sim$90% eff for $p_T > 1$ GeV.



L0: L1-algorithm: VELO→TT1

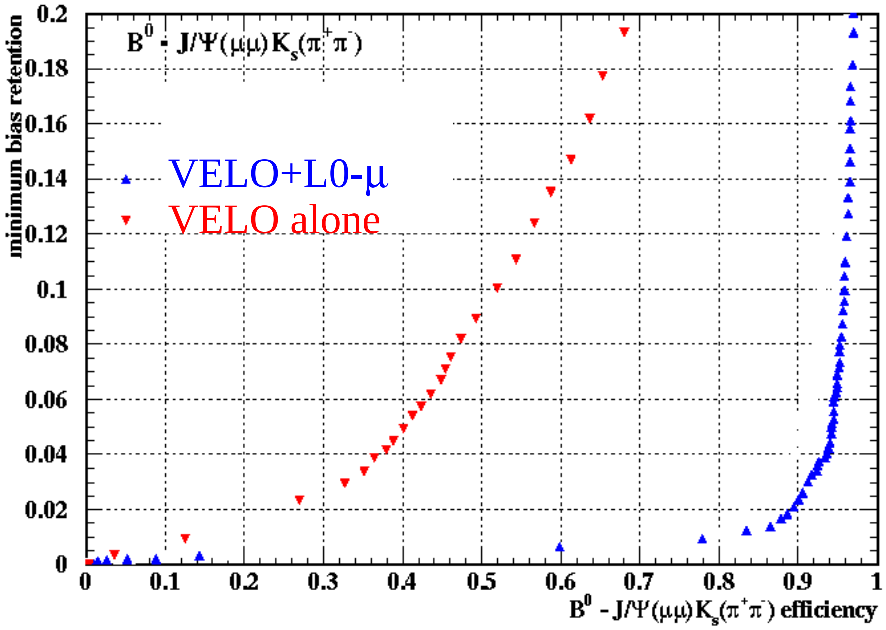
- Momentum of VELO tracks with significant impact parameter using TT1.



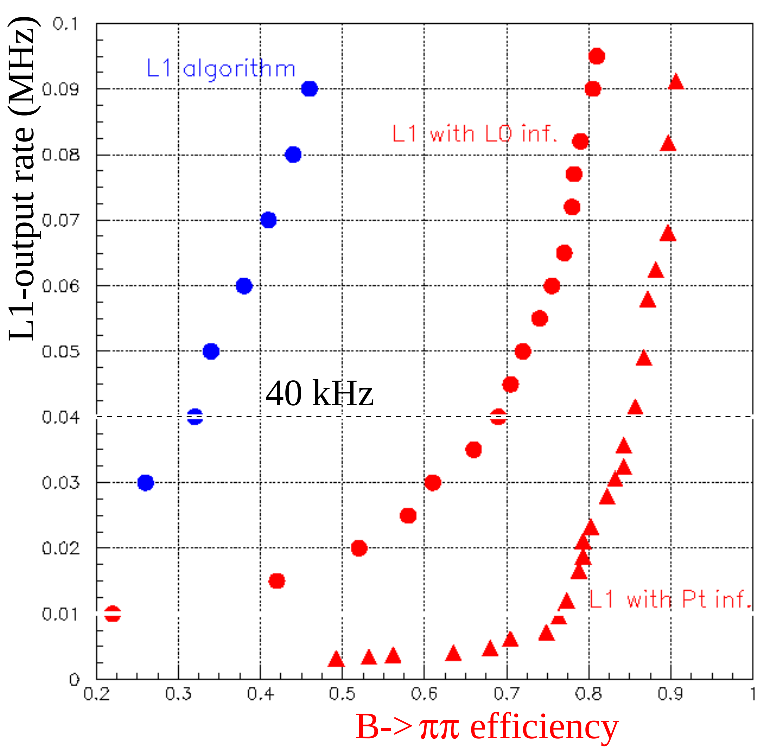


L1 Preliminary Performance

- L0-μ linked to VELO track with significant impact parameter provides excellent signature.



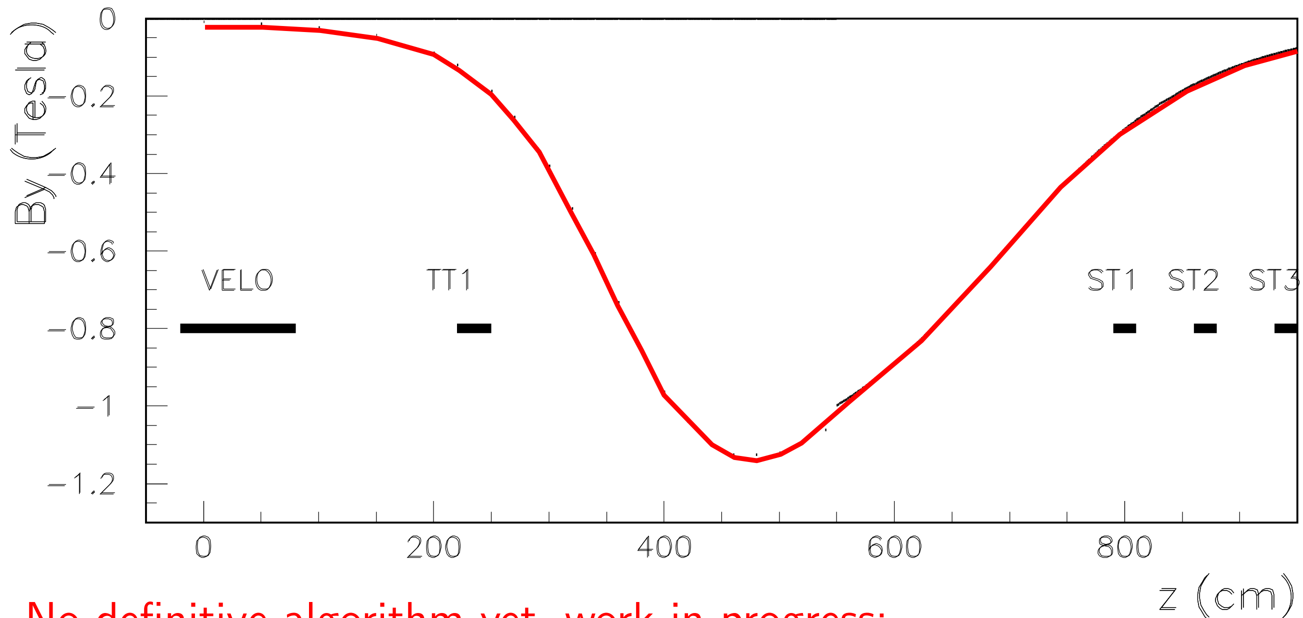
- Momentum information (from L0&TT1) for hadronic channels



Higher Level Triggers

Boundary conditions:

- Read all event data into CPU farm with 40kHz
- About 900 CPUs, hence: about ∼20 ms/event.
- Aim: roughly 200 Hz output rate.



No definitive algorithm yet, work in progress:

- Confirm L1, but with dp/p=1% using ST1-3.
- Investigating fast tracking algorithm(s) to connect VELO tracks to ST1-3, example: Hough transform.
  - Use only wire position (not TDC) of straw chambers
  - Reached $\sim 95\%$ efficiency for tracks > 5 GeV
  - Time/track $\sim$ 1 ms on 2001 CPU
- Use parametrized momentum determination, not Kalman filter

Summary

L0 Based on largest E_T leptons and hadron. Additional information on number of primary vertices, event multiplicity and total energy in calorimeter.
Implementation fully synchronous, protoype work in progress.

L1 Partial event building at 1 MHz, uses information of L0, and does tracking in VELO and TT1 on small CPU farm.
A 10% prototype in operation.

L2/3 Full reconstruction on farm. Fast algorithms under development.

LHCb Trigger TDR forseen for January 2003.

Trigger² (tri·gəɹ). [f. TRIG *v.*¹ + -ER ¹.]
1. A device or appliance to retard or stop the motion of a vehicle descending a slope.

The Compact Edition of the Oxford English Dictionary
Oxford University Press, Twenty-Third edition, January 1984