LHCb Vertex Detector Electronics Timing and Synchronization

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Abstract

Synchronization of the electronics is the key issue at LHC with the short bunch crossing period, the very high trigger rate and the large number of detector channels. The Vertex Detector signals from 200K channels have to be sampled optimally. The consistency of the event data fragments from all detector channels must be guaranteed during data flow in the front-end and off-detector electronics and the data acquisition system. The ongoing activity in the LHCb Vertex Detector is described. The necessary synchronization hardware and procedure to detect synchronization errors and to recover with a minimum data losses are presented.

1 Introduction

LHCb is a dedicated experiment to study CP violation and other rare phenomena in B-meson decays at LHC [1]. Spectrometer consists of a vertex detector at the intersection point (placed in "Roman pots"), tracking system, RICH counters with aerogel and gas radiators, a large-gap dipole magnet, a calorimeter system and a muon system. The LHCb detector provides a good acceptance for both b-hadrons in a $b\bar{b}$ event, a particle identification capability, a good invariant mass resolution and efficient lepton, hadron and displaced vertex triggers. It is planning to reach its physics goal using only events with single interactions. The detector will therefore be operated at a modest luminosity of 2×10^{32} cm^{-2}s^{-1} for its entire lifetime.

The overall architecture of the LHCb front-end electronics, trigger and data acquisition system [2] is shown in Figure 1. Detector signals are sampled at 40 MHz and are buffered

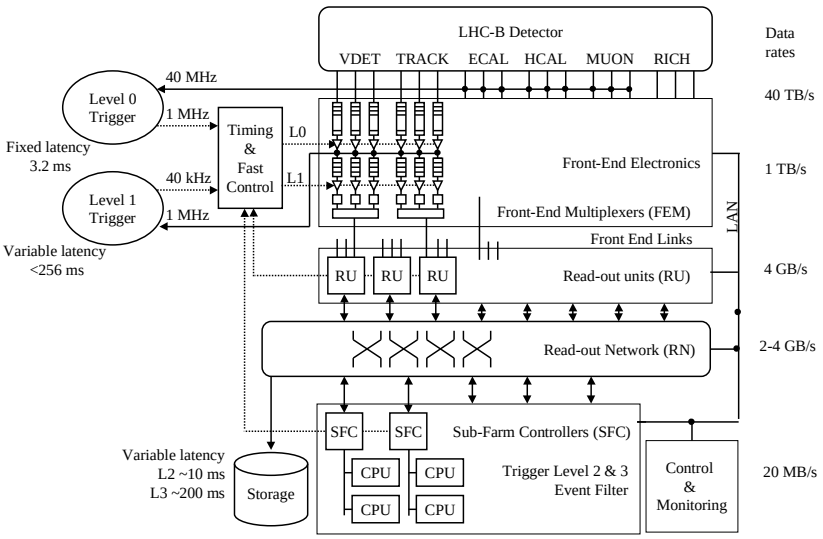

Figure 1: LHCb Trigger/DAQ architecture

during the latencies of the Level-0 (accept rate of 1 MHz) and Level-1 (accept rate of 40 kHz) triggers. Triggers use data from specific detectors, namely muon, calorimeter and pile-up for the

Level-0 trigger and vertex detector for the Level-1 trigger. The LHCb timing and fast control system distributes a common clock, a Level-0 and a Level-1 trigger decisions and synchronous commands to all components. It uses the CERN TTC system [3] as a backbone but requires a LHCb specific Readout Supervisor and a Switch. Data for accepted events are processed and transferred to the DAQ system. Table 1 summarize the main LHCb front-end electronics, trigger and data acquisition system parameters.

Table 1: Main LHCb Trigger/DAQ parameters

Number of channels	950000
Bunch crossing rate	40 MHz
Fixed Level-0 latency	4 μs
Level-0 accept rate	1 MHz
Variable Level-1 latency	max 1 ms
Level-1 accept rate	40 kHz
Readout rate	40 MHz
Average event size	100 kB

Event data from roughly one million channels shall flow through the front-end electronics, trigger and DAQ systems maintaining synchronization across event fragments from different parts of the experiment. The LHCb front-end electronics will be located in a harsh radiation environment and, therefore, errors are unavoidable. However, they must be detected and reported and an error recovery procedure shall be defined.

2 Vertex Detector Electronics

A total of 19 layers of silicon microstrip detectors are placed perpendicular to the beam, of which 17 layers are used as a vertex detector system. Each layer consists of two planes with r and phi strips respectively. These strip configurations are chosen to make an efficient trigger algorithm for the fast track reconstruction. The total number of the detector channels is around 220K. The vertex detector electronics follows the general LHCb architecture described above. The functional diagram is shown in Figure 2

and consists of front-end, off-detector and processing electronics.

The radiation hard front-end electronics are mounted near the detector inside the vacuum tank. Analog, rather than binary, readout has been chosen since it allows for a better monitoring and control of the radiation damage in the detector. 128-channel front-end chips perform data storage in 160 stages analog pipeline with integrated derandomizing buffer of 16 stages during the Level-0 trigger latency. Upon receiving the Level-0 trigger accept signal, data from the derandomizer are multiplexed (32 to 1) and transmitted to the off-detector electronics via analogue data links (4 links per front-end chip). The read-out speed is 40 MHz and the total readout time is 900 ns. This allows four extra time slots for the data framing (header, status) in addition to the detector channel data. The TTC receiver chip provides the clock, Level-0 accept and reset signals. The I2C serial bus is used to control and monitor both the front-end and the TTC receiver chips.

The off-detector electronics is located at a distance of maximum cable length of 10 m from the detector, connected by 7000 twisted-pair cables to the front-end electronics. It performs analog data digitizing (8-bit 40 MHz FADC), synchronization tasks (as discussed in [4]), data preprocessing for the Level-1 vertex topology trigger, digital data storage during Level-1 trigger latency and transmission to the processing electronics after Level-1 decision. It is implemented

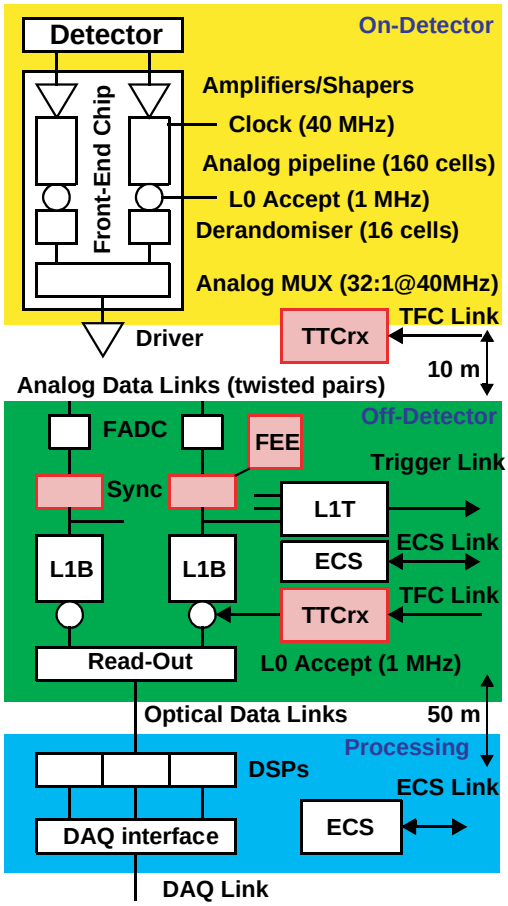

Figure 2: LHCb Vertex Detector Electronics

as 64 channels custom modules. Similar to the front-end electronics, the TTC receiver chip provides the clock, Level-0 accept and reset signals. The interface to the experiment control system on the board performs loading of the necessary parameters (registers, lookup tables), FPGA in-system reprogramming and monitoring of correct functioning of the electronics (error and performance statistics) while the experiment is running.

After Level-1 decision the event data are transmitted via optical links to the processing electronics, located in the counting room and based on commercial components and boards (e.g. DSPs). One DSP processes the data from a number of detector channels. It continuously updates the pedestal and noise for every channel and every event, makes common baseline shift corrections, excludes noisy channels, keeps track of hot and dead channels and monitors the errors. The zero-suppressed data are transferred to the DAQ system. Table 2 summarize the main vertex detector electronics parameters.

3 Synchronization Tasks and Hardware

All parts of the vertex detector electronics (front-end, off-detector and processing) receive clock, Level-0 accept, Level-1 decision and reset centrally from the LHCb timing and fast control system via TTC receiver chip with deterministic delivery time. However, data from different detector channels follow different data paths and hence different path delays have to be compensated in order to provide synchronous data arrival to the defined points along the data flow. A number

Table 2: Main vertex detector electronics parameters

Number of detector channels	220000
Number of analog data links	7000
Number of readout modules	110
Number of optical data links	110
Number of DSPs	880

of such points in the vertex detector electronics is specified below.

3.1 Sampling synchronization

In the front-end electronics the sampling from the front-end amplifier into the analog pipeline in has to be synchronized to the peak of the signal. The FADCs in the read-out modules may need an adjustment of their clock phases for correct sampling of incoming analog data from the input links.

For the front-end electronics the clock phase adjustment is performed using built-in features in TTC receiver chip (0.1 ns clock phase adjustment). One TTC receiver chip serves the group of front-end chips and, therefore, the clock phase adjustment can be performed only for a whole group of chips. The correct value of the clock phase is initially set on signal model and later adjusted using test pulses.

In the off-detector electronics one TTC receiver chip is included in the read-out module. It can be used for a global clock phase adjustment which affects all the FADCs in the module. For individual clock phase adjustment for the group of 4 FADCs (digitizing input analog data from one front-end chip) the programmable delay line with 1 ns step is used.

3.2 Level-0 accept synchronization and event tagging

Upon receiving the Level-0 trigger accept signal, data from the analogue pipeline are transferred to the derandomizer. The Level-0 trigger latency is fixed and for LHCb is equal to 160 clock cycles. In order to compensate for different data paths in the front-end electronics, the TTC receiver chip has programmable delay (up to 16 clock cycles) for the Level-0 accept signal.

At that point the event data are tagged with the event identification. For the vertex detector the event identification chosen is an 8-bit Level-0 pipeline address. It is transmitted to the off-detector electronics from the front-end chip as a pseudo-digital header using two empty time slots between the analog samples on four analog links.

3.3 Front-end data synchronization and error detection

In the off-detector electronics analogue data from the input links are continuously digitized. The detection of the event data is done by the synchronization logic. It uses time arrival prediction and generated pipeline address from the emulator of the front-end chip control logic. The synchronization logic compares the pipeline address received from the front-end electronics with one provided by the emulator in order to check the integrity of the data from different front-end chips.

Upon detecting an error the synchronization logic masks (set to zeroes) event data for the Level-1 trigger. The error flag is also written in the Level-1 buffer together with the event data.

The emulator and the TTC receiver chip provide full event identification information (bunch-crossing and event number) to be stored together with the event data in the Level-1 buffer. The

event number is also attached to the data to be sent to the Level-1 vertex topology trigger.

3.4 Level-1 decision synchronization

Event data in the Level-1 buffer are kept in the order of arrival (first-in, first-out). At the output of the Level-1 buffer event data are synchronized to the Level-1 decision. This decision is delivered by the TTC receiver chip in the same order as the event order in the Level-1 buffer.

It contains the accept/reject bit and two less significant bits of the event number, attached to the data by the off-detector electronics synchronization logic. There two bits are used for synchronization. I a case of error, the error flag is attached to the data. The use of only two bits reduces the required TTC bandwidth but still allows for the synchronisation check.

After the Level-1 accept, the events are re-numbered. An additional, monotonous DAQ number is added to the event data. This number is used in the downstream DAQ for the event building.

3.5 Error detection and recovery

Synchronization errors are detected at several locations in the vertex detector electronics (front-end chip, off-detector electronics) and corrupted data are flagged. The error statistics is monitored by the processing electronics collected by the experiment control system and reported to the DAQ system (Figure 3).

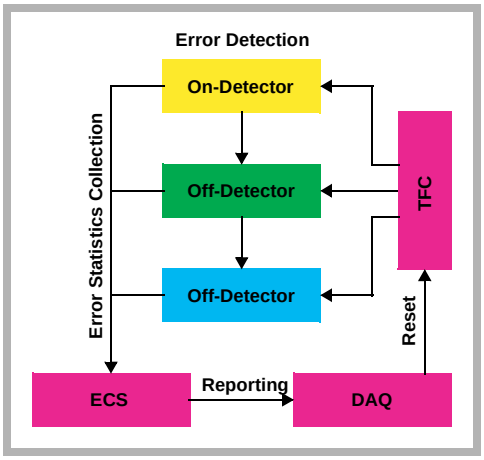

Figure 3: Error detection and recovery

In order to recover from errors, the global periodical resetting of the electronics has been chosen rather than local re-synchronization since it guarantees the uniform behavior of the whole experiment. Possible scenarios [5] include resetting of only the front-end electronics, off-detector electronics or both.

The resetting frequency is calculated using error detection rate in the electronics. The Reset signal is send to all LHCb electronics from the central place via the TTC system and may be synchronized to the gap in the LHC orbit to reduce event losses.

4 Summary

The vertex detector is a vital part of the LHCb experiment and its electronics must be robust against possible errors, unavoidable in the experiment environment. Synchronization check and

error detection is performed along the data flow and the error recovery procedure is defined. It involves periodical resets, based on the observed error rate.

The vertex electronics prototypes are under development for both the front-end and the off-detector electronics. The 4-channel off-detector module prototype is shown in Figure 4. The

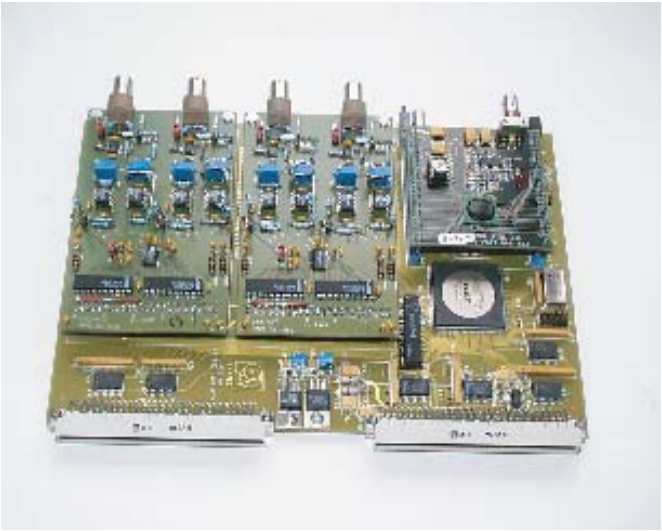

Figure 4: Off-detector electronics prototype

prototype performs input analog data digitizing and synchronization tasks. A local data storage on the module allows its usage in a stand-alone mode. The first possible application is a read-out of the front-end chip prototype.

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