ASSOCIATIVE MEMORY COMPUTING POWER AND ITS SIMULATION

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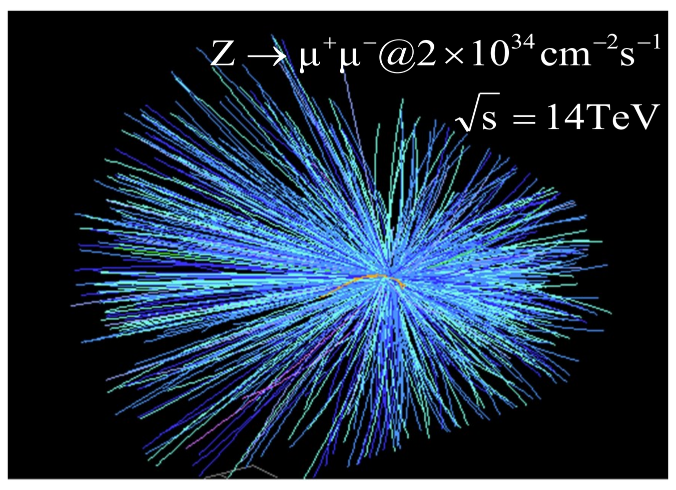
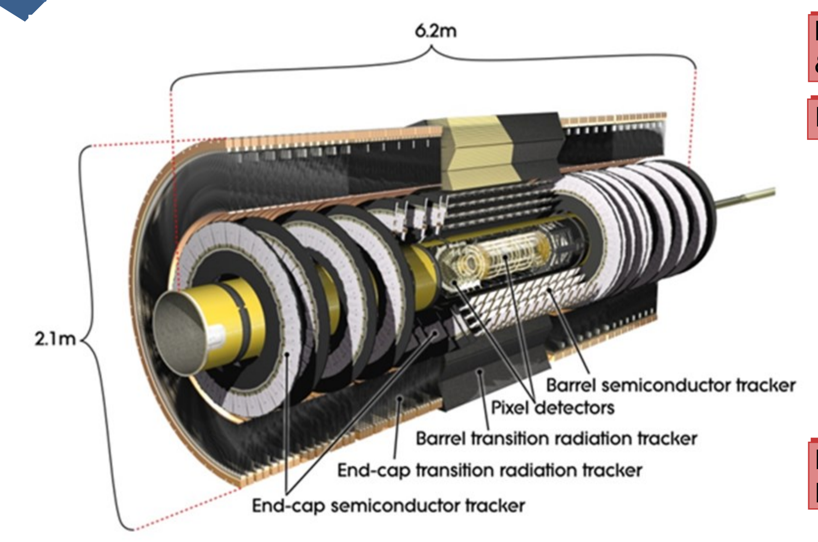
The Challenge

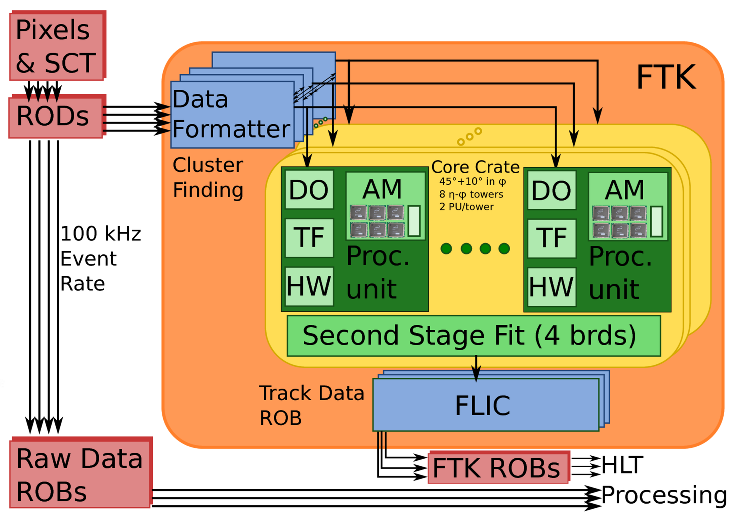


During LHC high luminosity running, the high rates, multiplicities and energies of particles produced in the p-p collisions pose a unique challenge to the ATLAS Trigger.

Online track reconstruction is proved to be an effective solution in separating the most interesting events from the extremely large pile-up background.

The ATLAS FTK Processor



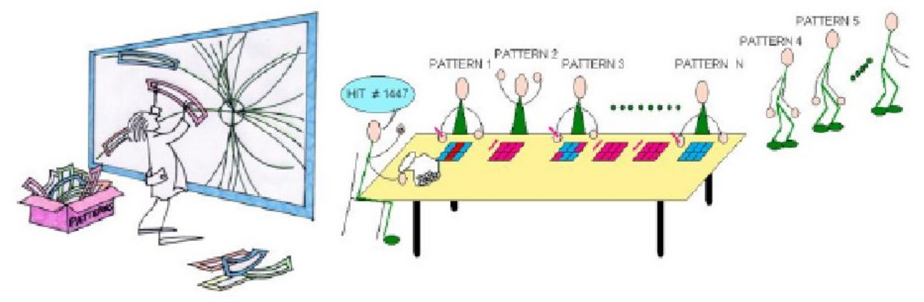


FTK will operate at full level 1 trigger output event rate (100kHz) and will provide high quality global track reconstruction at the beginning of level 2 trigger processing [1].

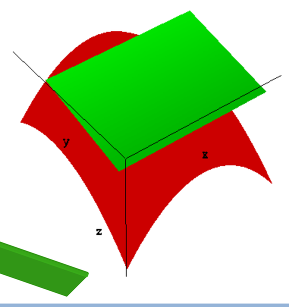
FTK uses a set of independent engines, each working on a different region of the Inner Detector (ID):

- 64 independent η-φ towers
- 512 parallel processing units

The Idea



Pattern recognition: carried out by a dedicated device called **Associative Memory (AM)**. Find coarse-resolution track candidates named roads. The AM compares in parallel the event hits with all the stored pre-calculated low resolution track patterns and returns the addresses of the matching patterns.



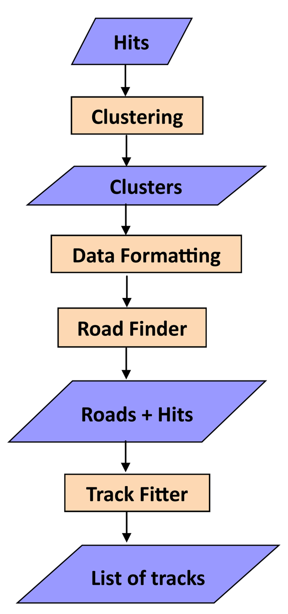
Track fitting: fit the full resolution hits inside the road to determine the track parameters. Exploit linearized constraints between the hit positions and helix parameters.

$$p_i = \sum_j C_{ij} \cdot x_j + q_i$$

FTK SIMULATION

FTK simulation describes the logic of the main parts inside the processor and verifies how different setups can influence the performance of the system.

The different HW steps are replicated in a detailed simulation. The main blocks are: **Road Finding (RF)** and **Track Fitting(TF)**.



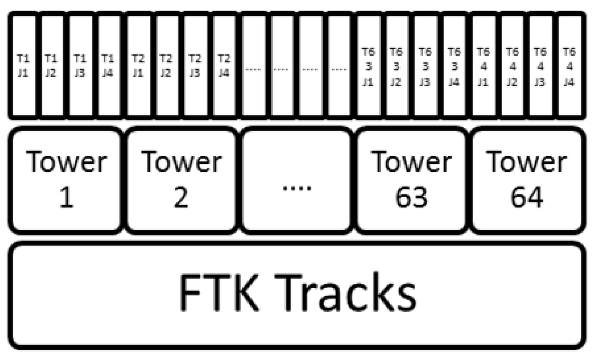
The RF controls the input: some clustering functionalities and distribution of the hits to the towers.

The RF output is a list of output roads with the associated hits, stored in different containers to save space.

Most memory consuming elements in the FTK simulation

Element type	Unit size	Number of Units	Memory requirements
Pattern bank	36 B/patt	10^9	36 GB
Fit Constants (1st stage)	616 B	$\sim10^6$	500 MB
Fit Constants (2nd stage)	1 KB	1.6×10^6	1.6 GB

The memory requirement is extremely high. The simulation tasks are divided in independent jobs. Each job controls only a fraction of the system, smaller than a single tower, in order to fit the task in standard machine.



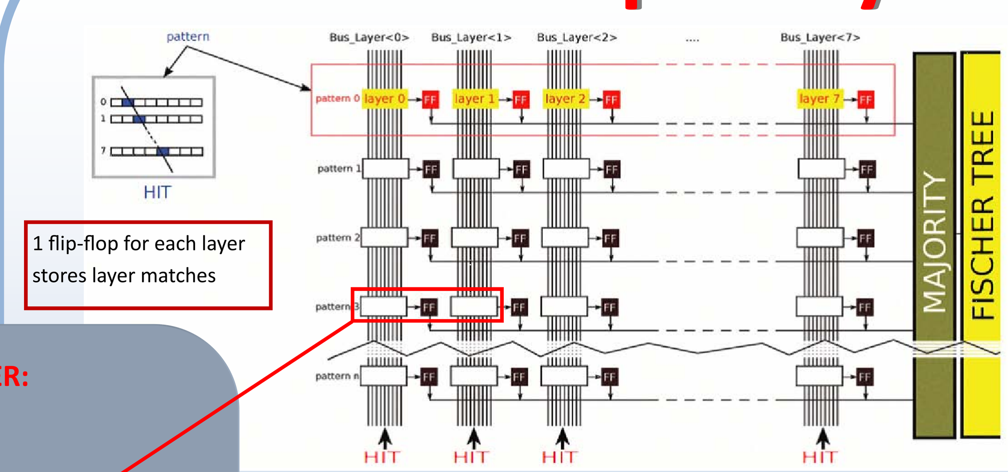
Segmentation:

- 64 hardware towers
- 4 jobs for each tower

→ 256 jobs.

The jobs of each tower are executed in sequence, with a partial merge at the end of the last job.

The AMchip array



AM CONSUMPTION [2]:

~2.5 W for 128 kpatterns

AM COMPUTING POWER:

Each pattern:

4 x 32 bit comparators

Each 10 ns

128 kpatt x 4 = 500 K instructions

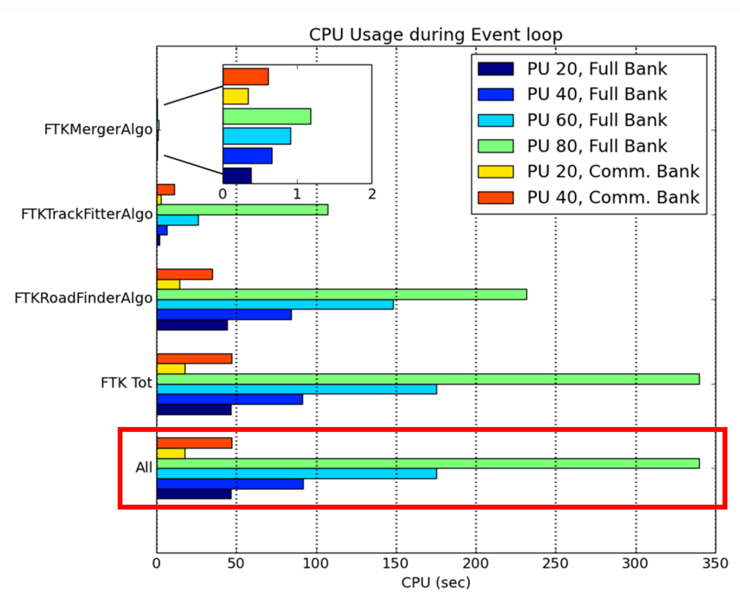
→ $500K \times 100M = 50\times10^6\,MIPS/chip$

$3.2\times10^9\,MIPS/AMB$ (64 chips)

$4\times10^{11}\,MIPS$ in the whole AM system

- Each row contains a pattern, one word/layer, each word stores one bin
- Input hits are presented on the Hit Buses. Each word compares its content to the hit.
- If a pattern match is found, the pattern address is transmitted on the output Address Bus.

CPU Time per Event

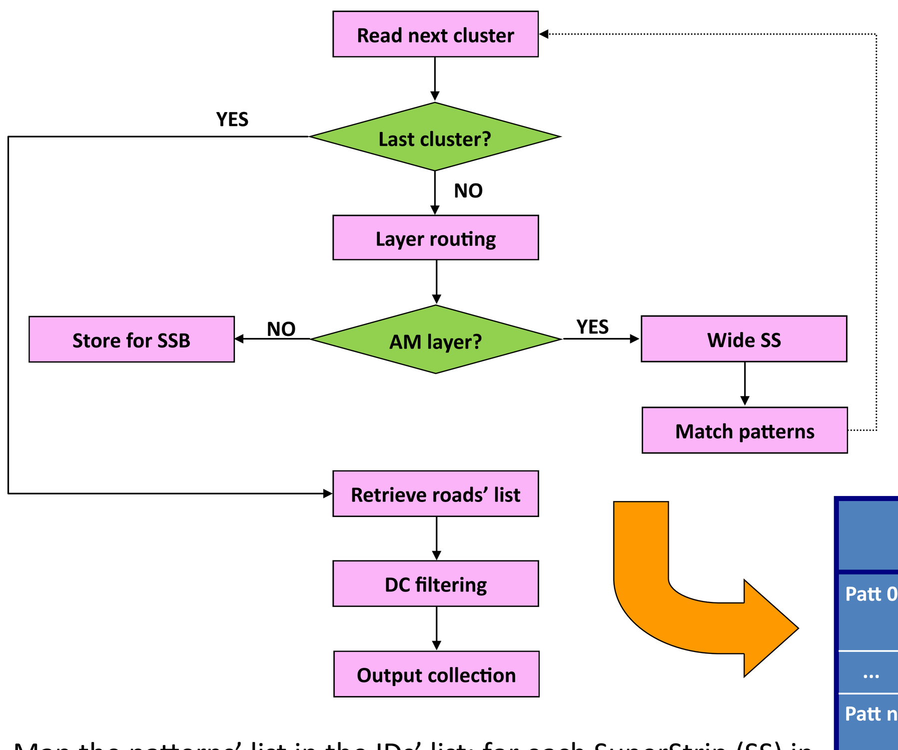


- **FTKRoadFinderAlgo**: pattern matching
- **FTKTrackFitterAlgo**: track fitting
- **FTKMergerAlgo**: merge of the tracks from the parallel jobs

- The measurements were taken with VM with 1.8 kSpecInt
- ***The emulation of the RF dominates the overall execution time***
- TF becomes important at high pile-up
- The FTKMergerAlgo is negligible

ROAD FINDING EMULATION

Road Finding Diagram

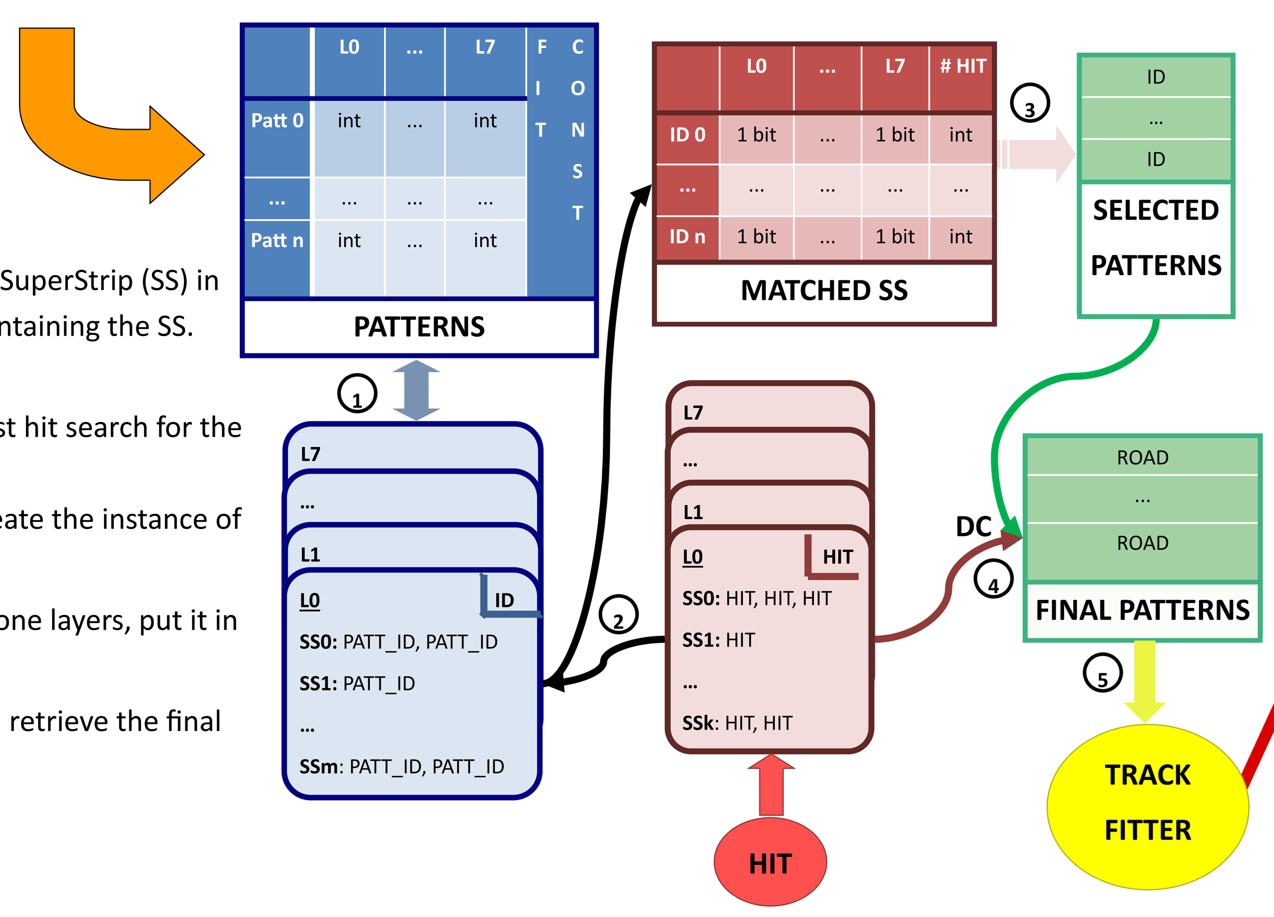


The road finding step reproduces the match between incoming clusters and the pattern bank, as the AM does.

The AM emulation module is the most important and consuming part of the whole simulation.

The code needs some internal structures to store the data in the chip, the status of the match during an event and the data to be sent to the next step.

Internal Data Structures



1. Map the patterns' list in the IDs' list: for each SuperStrip (SS) in each layer insert the list of the patterns' id containing the SS.
2. For each input hit:
   - Calculate the correspondent SS, if it's the first hit search for the related patterns in the "Matched SS" table.
   - Append the hit to list of hits for the SS or create the instance of the container.
3. When a pattern ID has hits on at least all but one layers, put it in the "Selected Patterns" table.
4. Check the "Don't Care" (DC) bit content and retrieve the final list of roads.
5. Send the output collection to the Track Fitter.

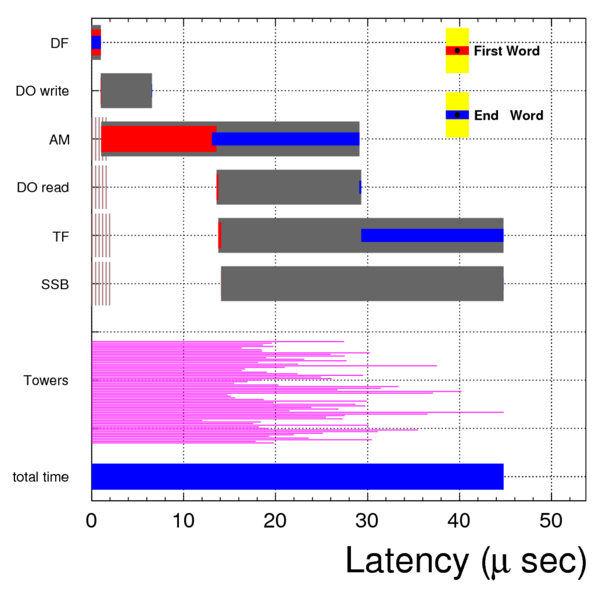
FTK SIMULATION RESULTS

The emulation software is an important test of the hardware because it can evaluate the performance of different types of AM implementations, changing most working points that are relevant for the AM performance[1].

Reaching good time performance for this emulation is important for two main reasons:

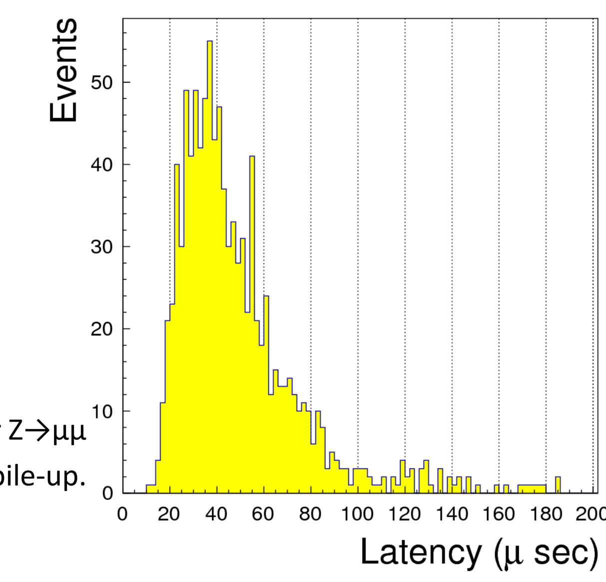
1. The emulation will be used to monitor the FTK hardware components in order to check for errors and malfunctions of the system.
2. ATLAS needs to emulate the system at the best to parameterize the effect of FTK on quantities that are interesting in physics analysis.

LATENCY



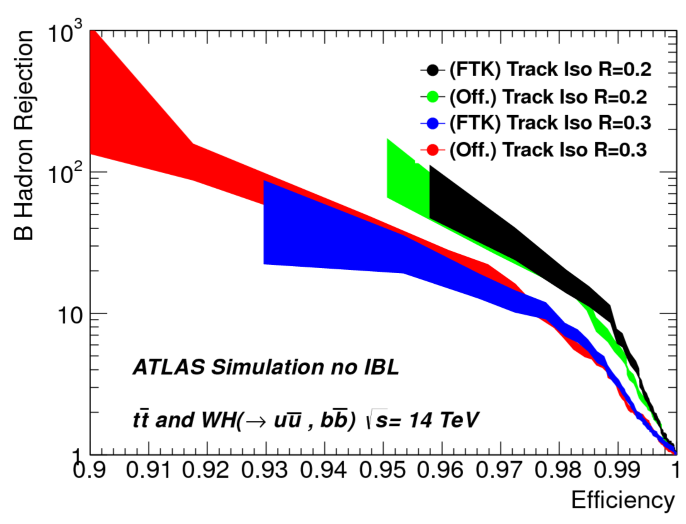
FTK latency for one event at 69 pile-up.

The timing of the functional blocks is given for the region that takes the most time.



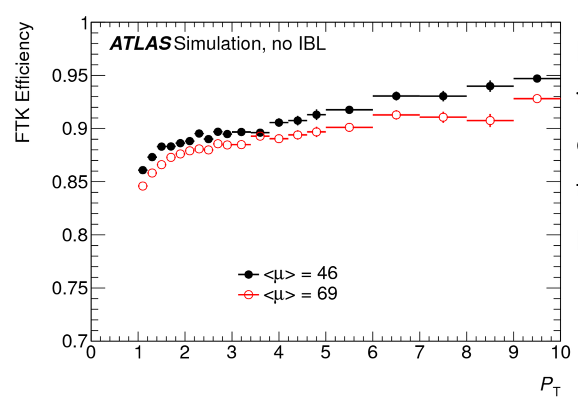
FTK latency for Z→μμ events with 69 pile-up.

EFFICIENCY

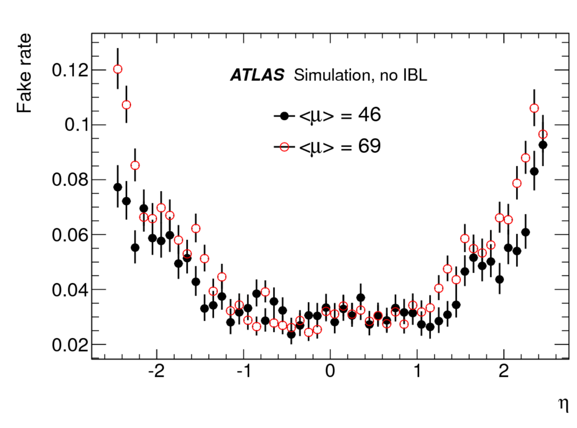


Efficiency versus rejection curves found in R=0.2 and R=0.3 cones around a central muon candidate originated from a W boson or B hadron. FTK curves are in agreement with those observed in offline.

The band represents the statistical uncertainty.



Efficiency of the FTK tracks with respect to offline tracks as a function of p_T with 46 and 69 pile-up events.



Fraction of FTK tracks not matched to truth as a function of η with 46 and 69 pile-up events.

References:

[1] ATLAS Collaboration, ATLAS Fast Tracker Technical Design Report

[2] G. Volpi et al., Performance of the AMBFTK board for the FastTracker processor for the ATLAS detector upgrade

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