The Associative Memory Serial Link Processor for the Fast TracKer (FTK) at ATLAS

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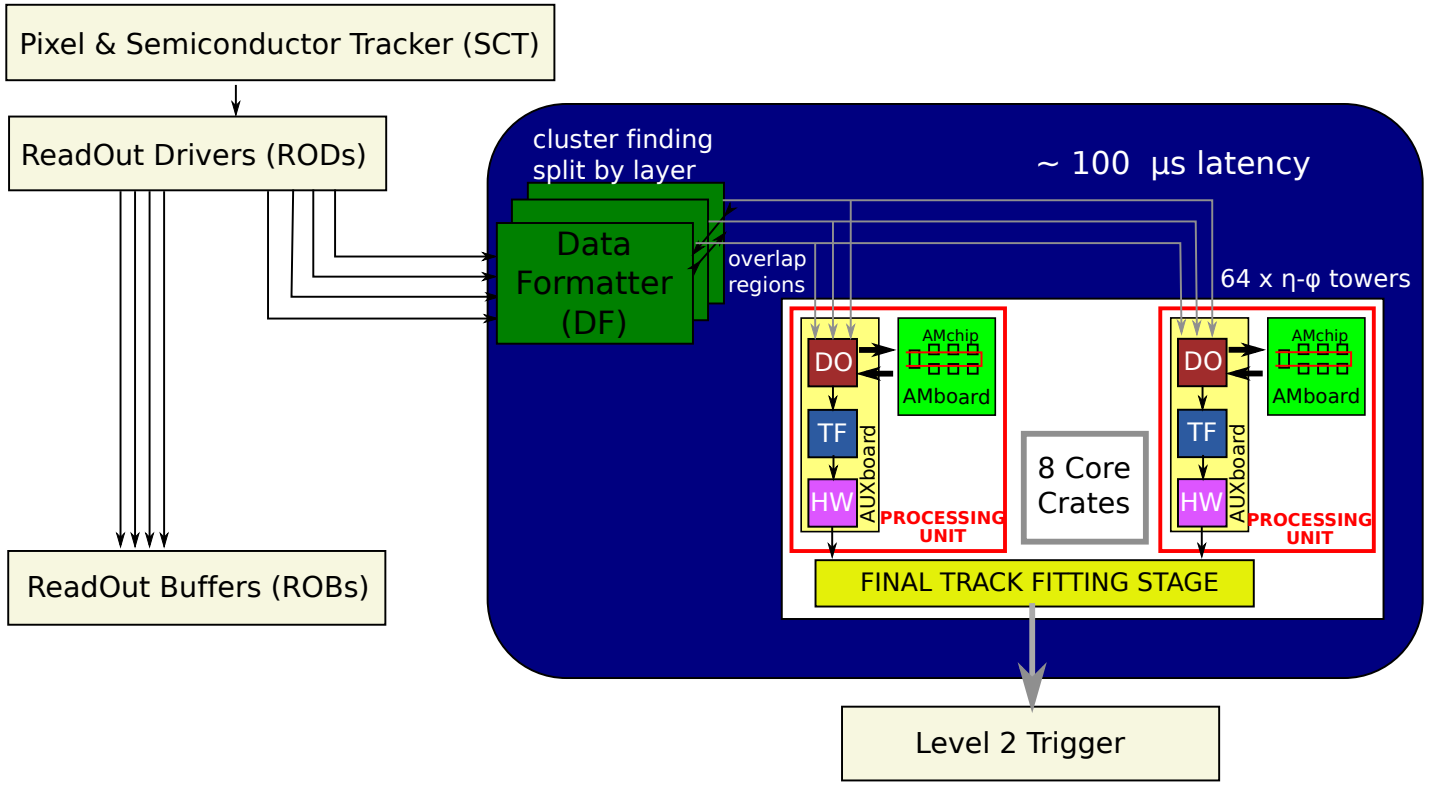
Overview

FTK Architecture



The FTK system is made of:

- 48 Data Formatters (DF)
- 128 Processing Units
- 32 Final Boards
- Interface towards Level 2 Trigger

Each processing unit is composed of:

- an AM Board with 8 M patterns
- a rear card (AUX Board) with
  - Data Organizer (DO)
  - Track Fitter (TF)
  - Hit Warrior (HW)

The AM System

The **Associative Memory (AM)** [1] system is the core of the FTK:

- It stores 1 billion (10^9) AM patterns for pattern recognition (in the whole FTK system)
- It performs pattern matching using the hit information of the ATLAS silicon tracker
- It finds track candidates at low resolution that are seeds for a full resolution track fitting

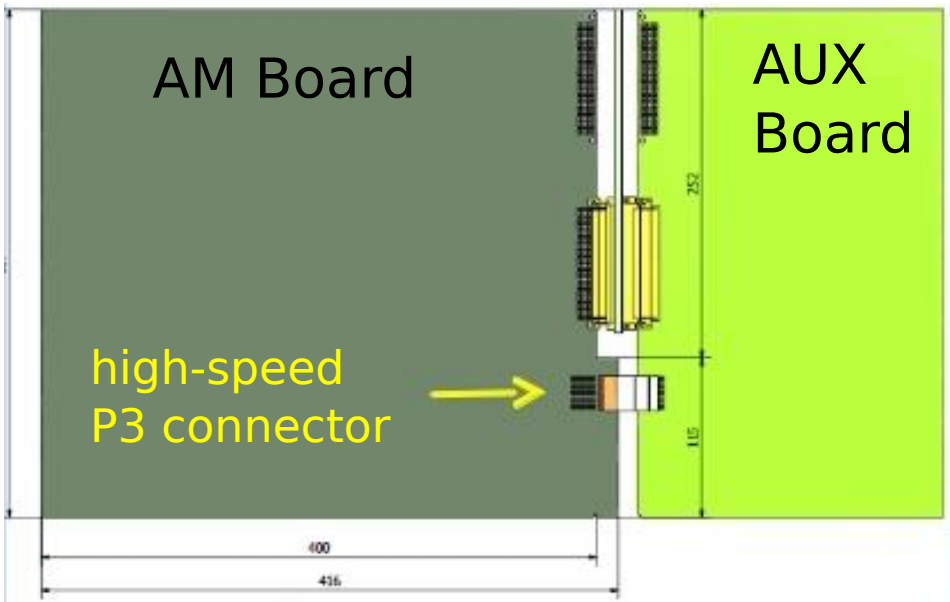
Pattern density:
1 G patterns in the whole FTK system
$\longrightarrow$ 8 M patterns per board (128 boards)
$\longrightarrow$ 128 k patterns per chip (64 AM chips / board)

[1] A. Andreani et al., "The AMchip04 and the processing unit prototype for the FastTracker," *IOP J. Instr.* **7** (2012) C08007

AM Chip and Board Requirements

Major concerns:

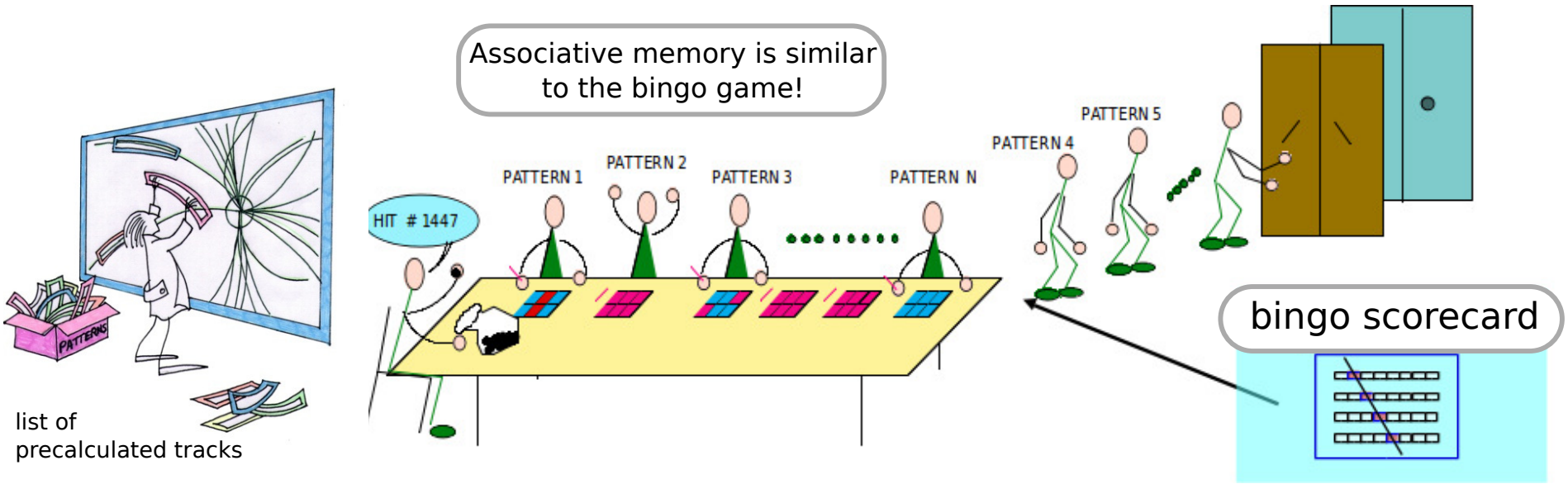
- high pattern density (**8 Mpattern/board**) $\longrightarrow$ large silicon area
- I/O signal congestion at board level (solution: **2 Gbit/s** serial links)
- Maximum power limited by cooling (because we are fitting 8 k AM chips in 8 VME crates and 8 racks): **250 W** per AM board



- AM Board: 9U VME board
- AUX Board: rear card (placed in the same slot of the VME Core Crate)

Serial links must work at 2 Gbit/s $\longrightarrow$ **ERNI 973028 ERmet ZD High-Speed Connector** (P3) between cards

The Associative Memory working principle



- Dedicated device $\longrightarrow$ maximum parallelism
- Each pattern with dedicated comparator
- Track search during detector readout

The Associative Memory integrated circuit (AMChip)

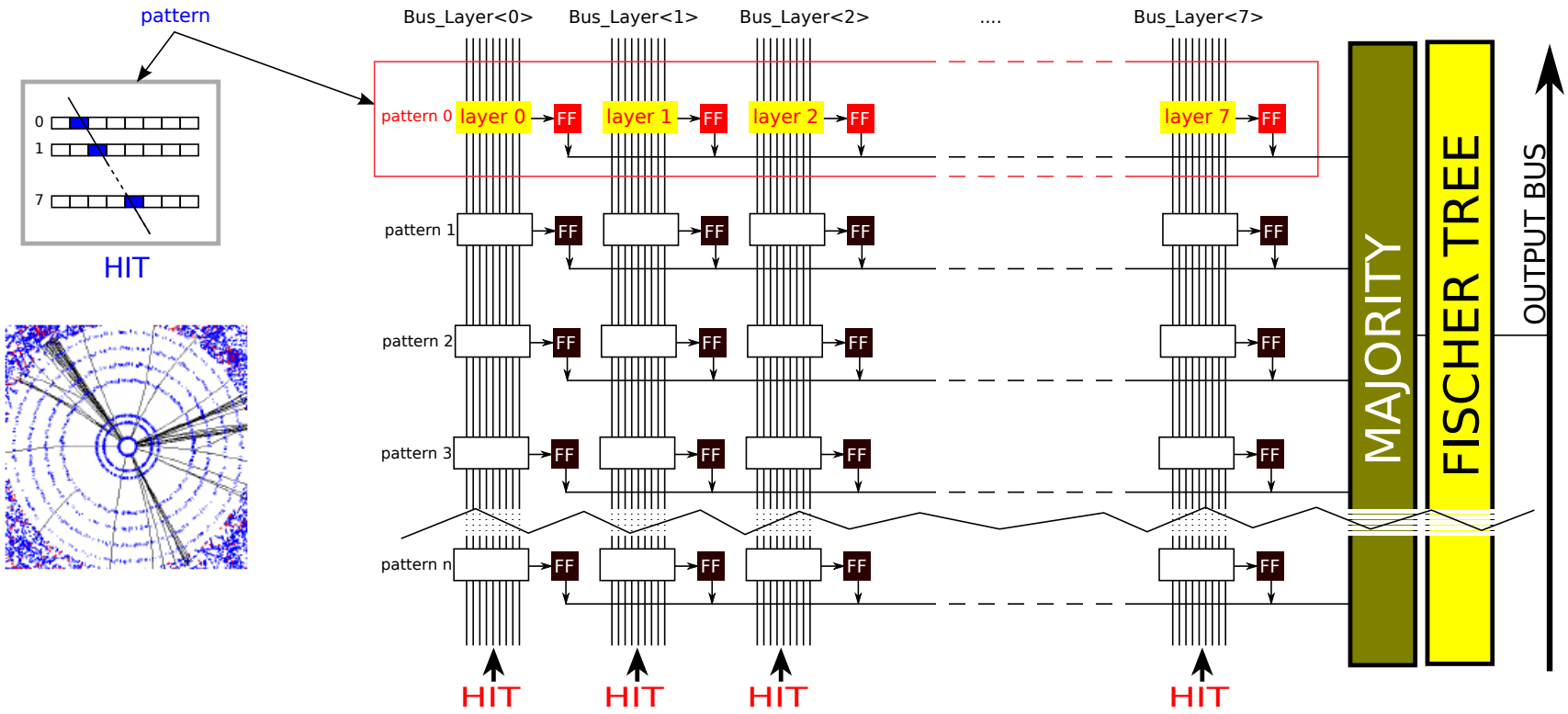
Several versions of the AMChip:

Vers.	*Design*	*Tech.*	*Area*	*Patterns*	*Package*
1	Full custom	700 nm		128	QFP
2	FPGA	350 nm		128	QFP
3	Std cells	180 nm	100 mm^2	5 k	QFP
4	Std cells + Full custom	65 nm	14 mm^2	8 k	QFP
mini-5	**Std cells + Full custom + SERDES IP blocks**	**65 nm**	**4 mm^2**	**0,5 k**	**QFP**
5			**12 mm^2**	**3 k**	**BGA**
6	**Std cells + Full custom + SERDES IP blocks**	**65 nm**	**150 mm^2**	**128 k**	**BGA**

red = under fabrication

blue = under design (figures are estimated)

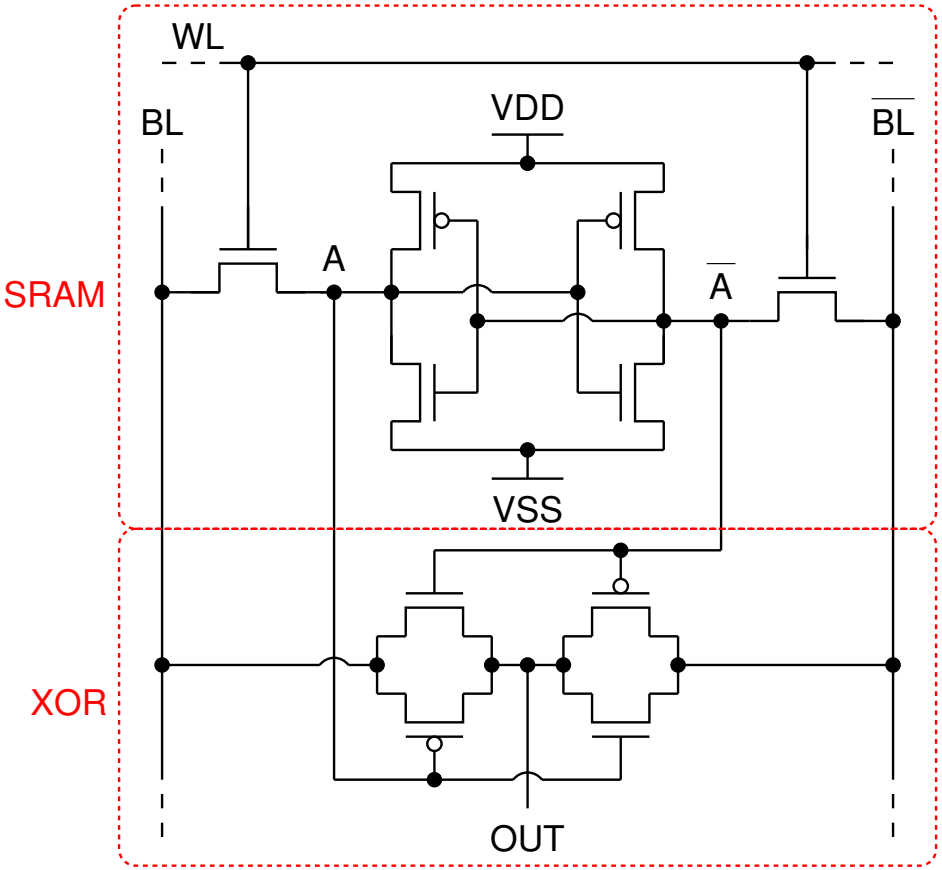
AM working principle

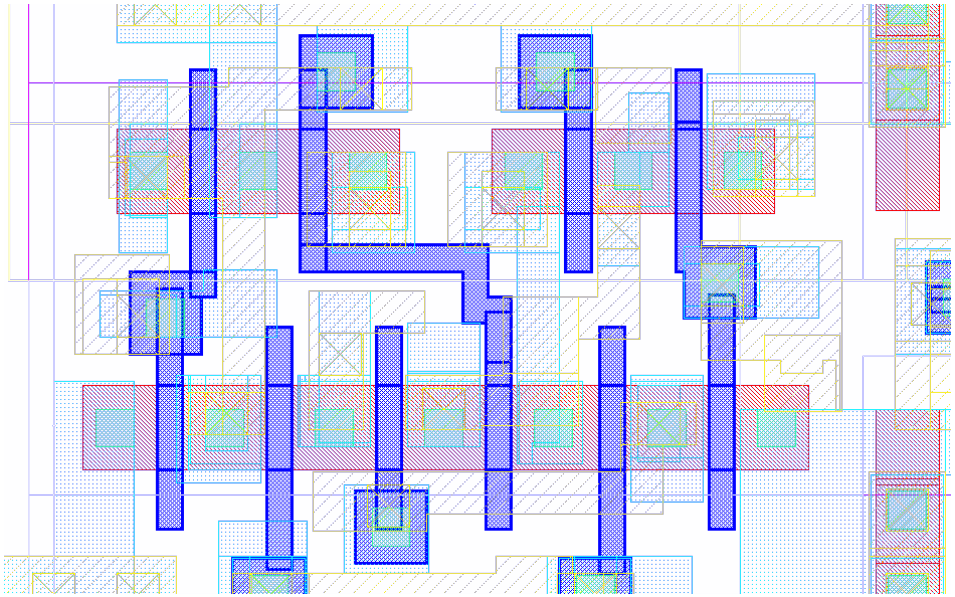


- Small (18 bit) CAM cell for each bus and for each pattern
- The CAM cell compares its own content with the hits received
- Matching result (1 or 0) is stored into a Flip-flop (FF)
- Partial matches are analyzed by the majority logic and compared to the desired threshold
- A priority encoder reads the matched patterns in order

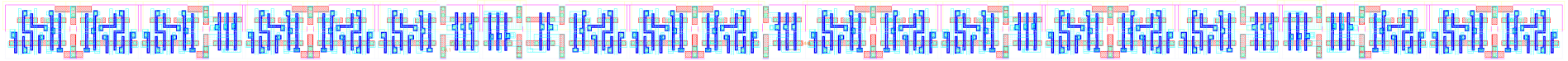
AMChip Memory Layer: (1) XORAM

New CAM cell, called XORAM, based on the XOR function and made of a 6T SRAM cell merged with a 6T-XOR gate.





Schematic and layout of the XORAM cell.

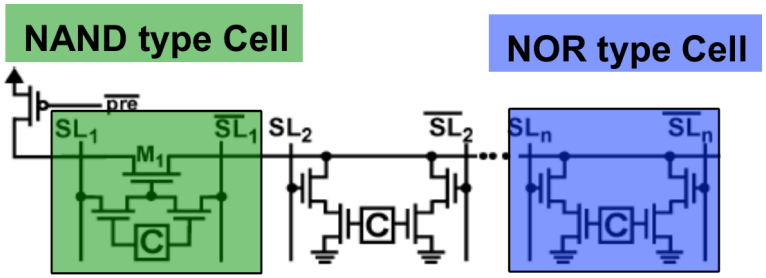


Layout of the 18-bit CAM cell, made of 18 XORAM cells and a 18-bit NOR gate

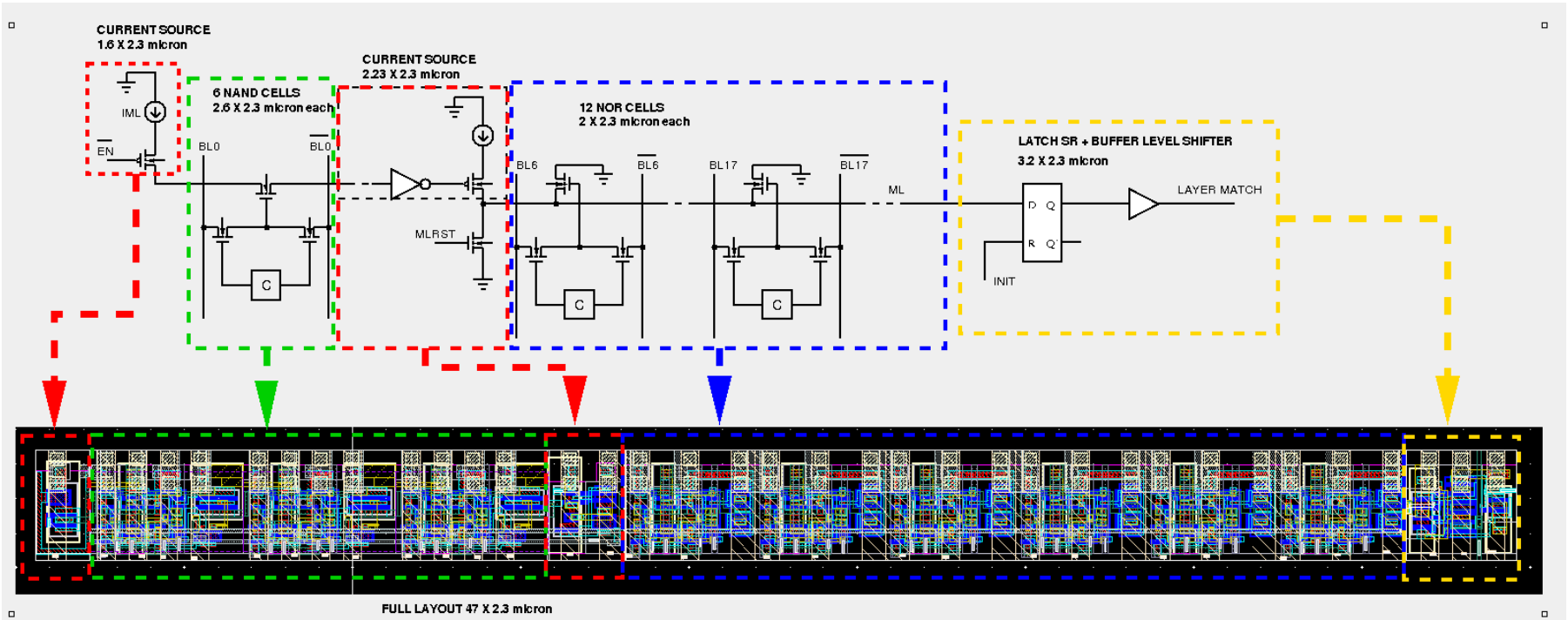
AMChip Memory Layer: (2) TOP2_LV

New low voltage (LV) current race CAM cell:

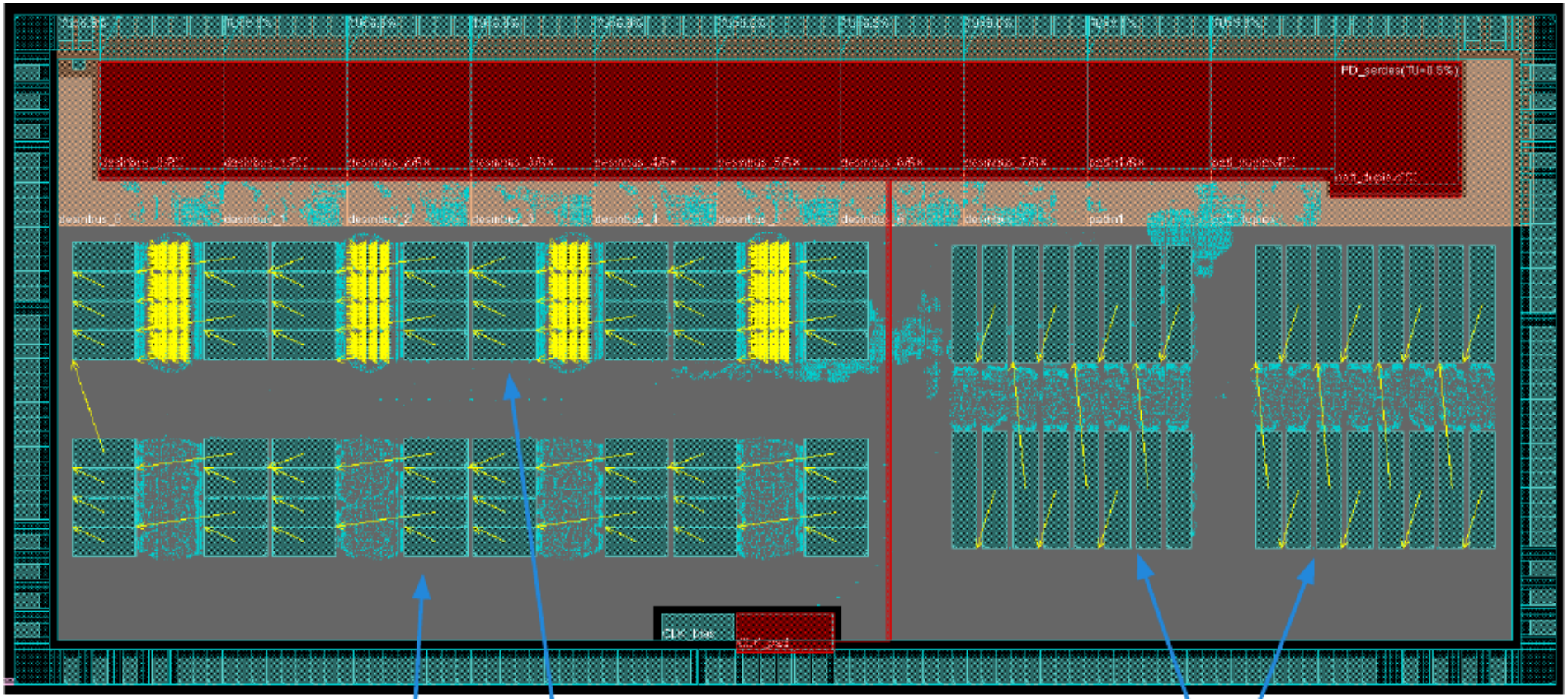
- 6 NAND type cells (9 transistors each)
- 12 NOR type cells (9 transistors each)
- 0.8 V supply
  (lower than 1.2 V used for std cells)
- Current race scheme
- Selective precharge scheme: $\longrightarrow$



K. Pagiamtzis and A. Sheikholeslami, "Content-addressable memory (CAM) circuits and architectures: A tutorial and survey," *IEEE J. Solid-State Circ.* **41** (2006) 712–727



AMChip05 layout



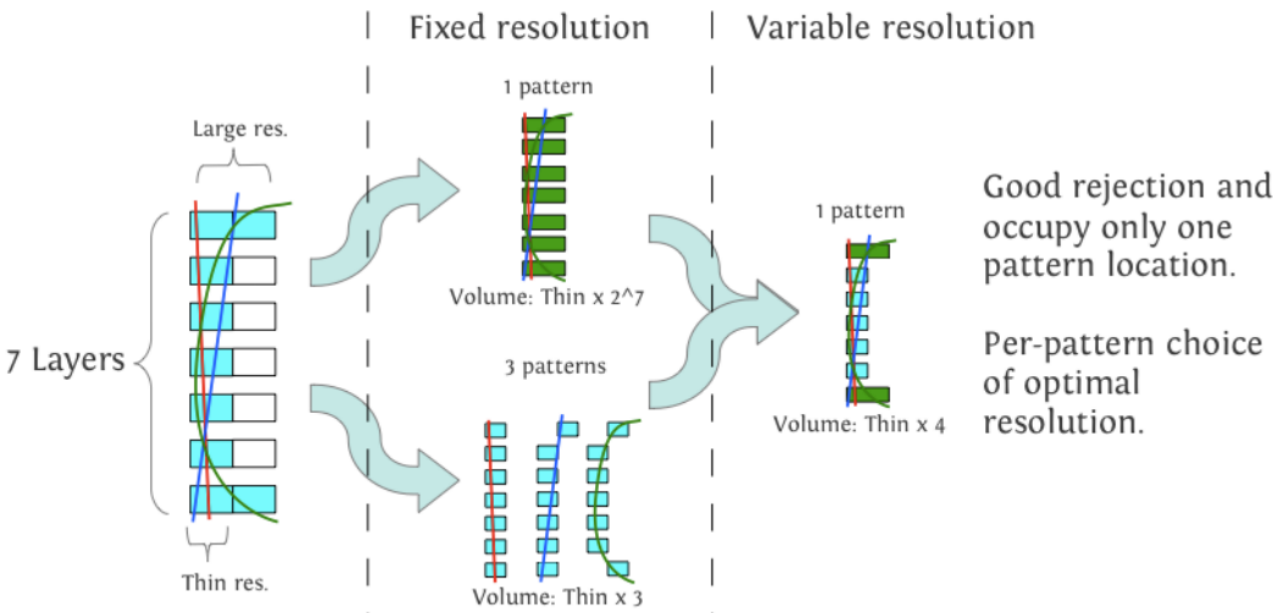
Evaluating 3 options:

- XORAM
- XORAM with full-custom majority
- LV NAND-NOR cells

Variable resolution AM

Ternary logic (1, 0 and "don't care") to improve performance:

- Wider patterns in high occupancy regions, smaller patterns in low coverage regions (where the number of trajectories is low, to reduce fakes)
- Pattern bank reduction factor: ≈5
- AM with "don't care" reduces the fakes by ≈7
- Good performance with almost same HW

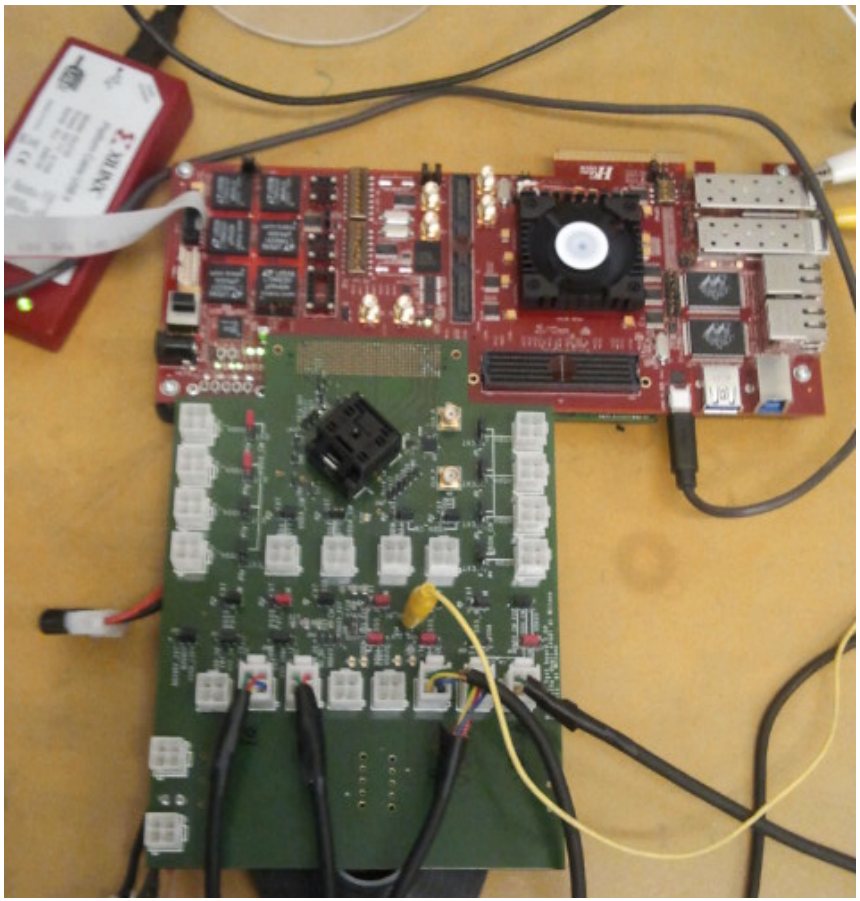


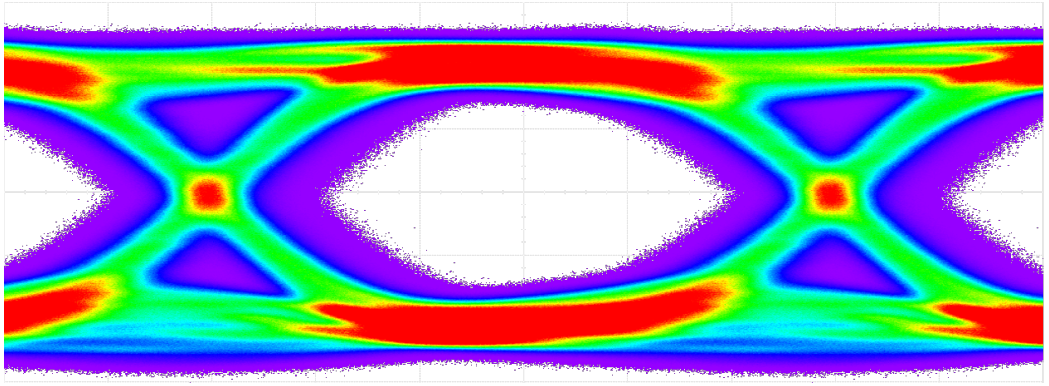
Pixels:

0	1	2	3	4	5	6	7
8	9	10	11	12	13	14	15
16	17	18	19	20	21	22	23
24	25	26	27	28	29	30	31

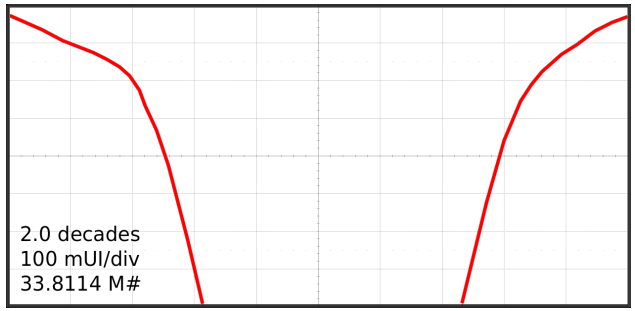
Using binary format
"01010" selects bin 10
"0001x" selects bins 2 or 3
"1x000" selects bins 16 or 24
"0x11x" selects bins 6,7,14, or 15
"111xx" selects bins 28 to 31

Serial link characterization (mini-AMChip05)





Eye diagram with serial data @ 2 Gbit/s



"Bathtub" diagram

Deterministic jitter: 55 ps; periodic jitter: 83 ps (after 18 h of measurements)
$\longrightarrow$ Bit error ratio: BER $\approx 10^{-21}$ (estimated)

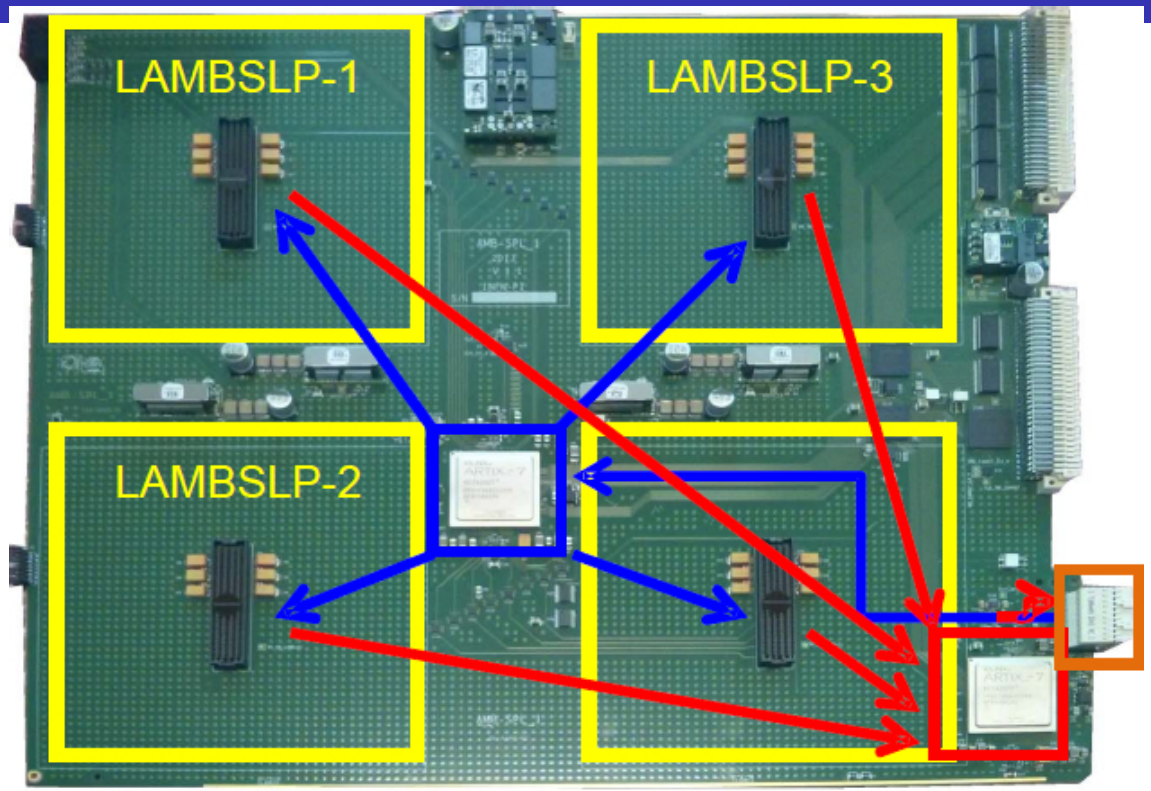
Current measurements (mini-AMChip05)

test mode	**current consumption**	
	1.0 V	1.2 V
baseline (all cells are disabled)	3.3 mA	4.0 mA
clock propagation inside XORAM	0.9 mA	1.0 mA
clock propagation inside TOP2	0.9 mA	1.0 mA
matching of 64 patterns for XORAM	2.7 mA	3.2 mA
matching of 64 patterns for TOP2	1.9 mA	2.4 mA

When the input data is changing the AMchip is active and performs the comparison between input and stored data **in parallel**

Dynamic power consumption due to the input data buses has been identified as the major contribution to the overall power $\longrightarrow$ the AMchip05 has been completely redesigned with different shape and arrangement of cells

FTK AMBoard

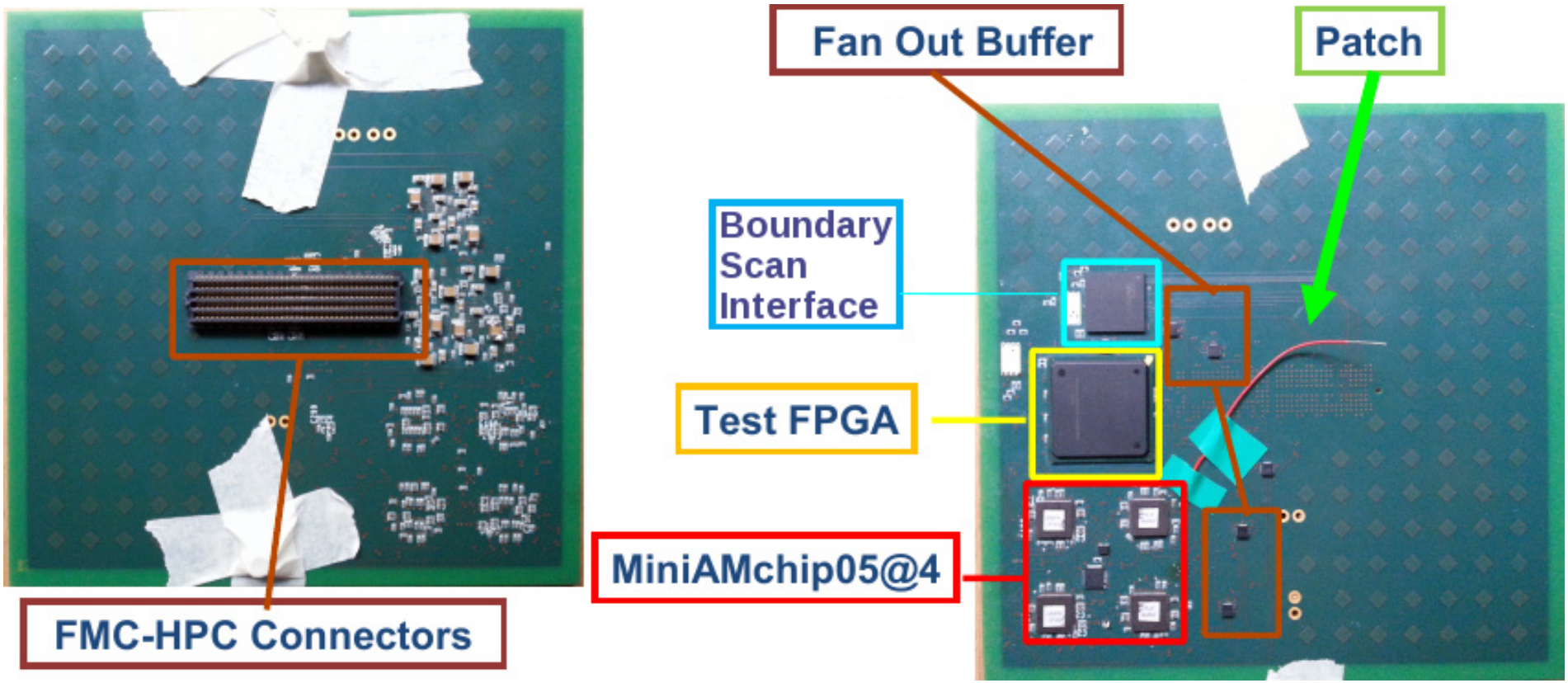


New AM Board, showing:

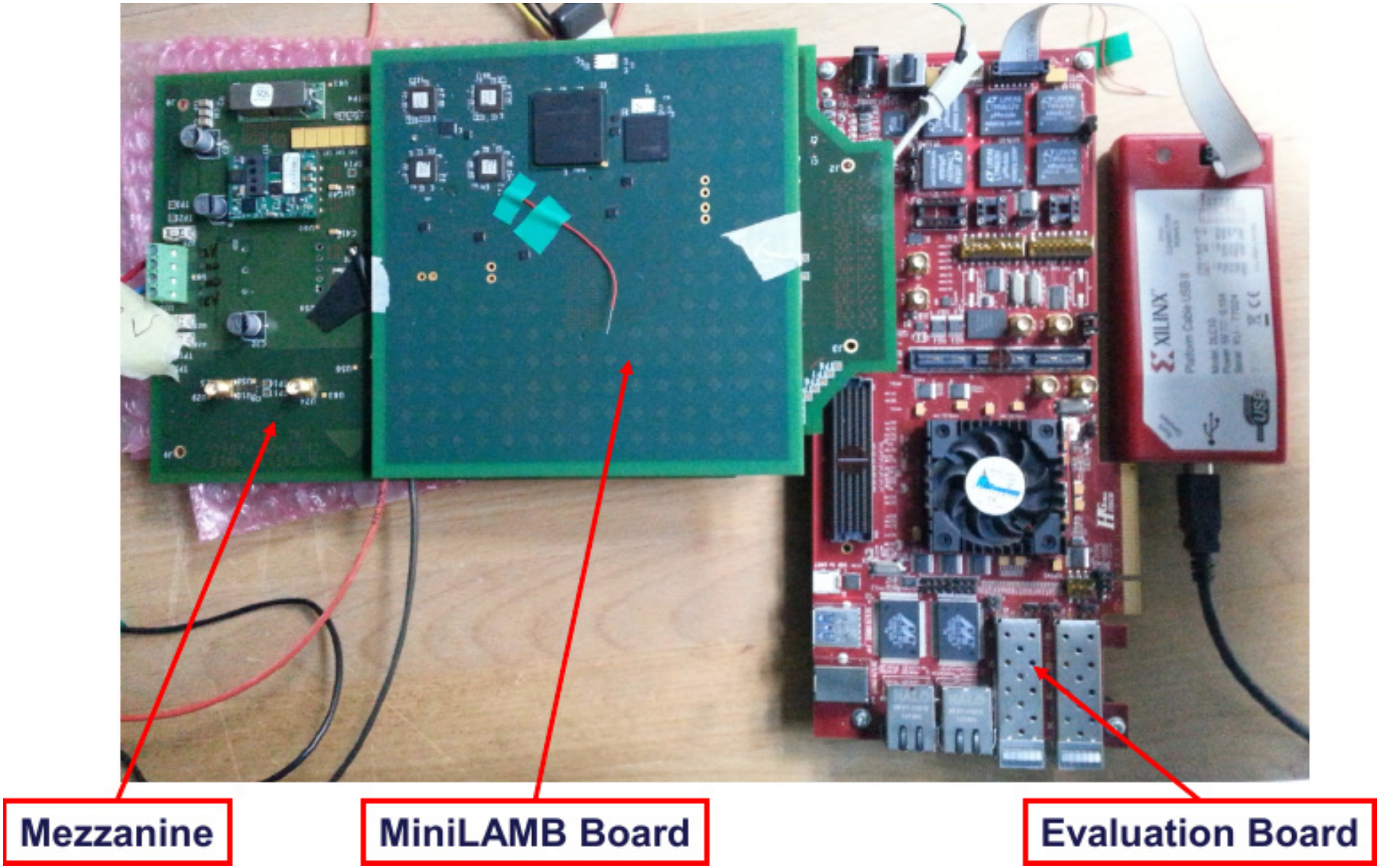
- input serial links: hit paths from ERNI 973028 ERmet ZD connector to LAMB
- output serial links: road paths from LAMB to ERNI 973028 ERmet ZD connector
- 2 ARTIX-7 FPGAs (one for the input and one for the output)

Serial link data rate = 2 Gbit/s

FTK miniLAMB prototype

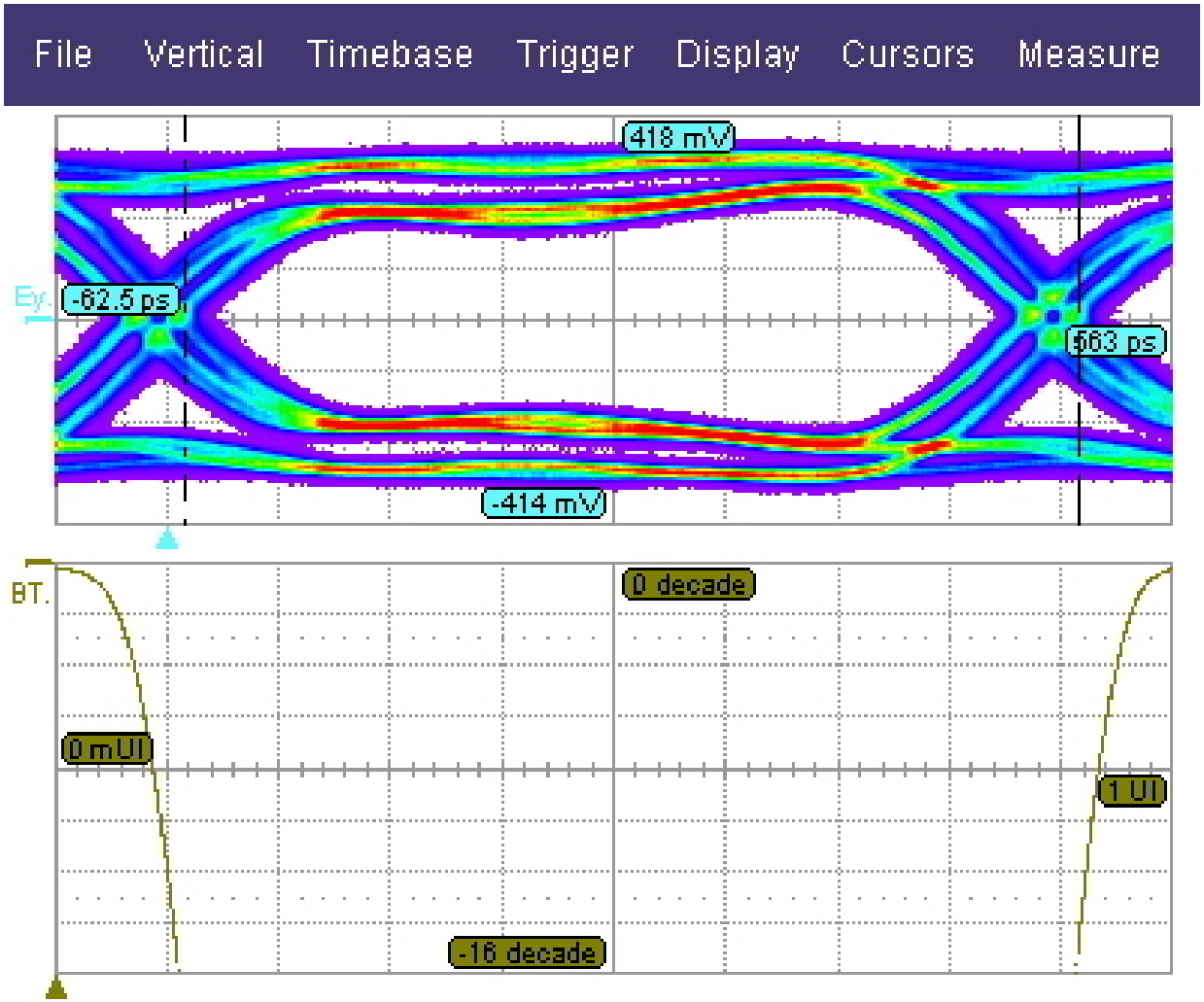


FTK miniLAMB prototype test



FTK miniLAMB prototype test

- SERDES working
- JTAG working
- PRBS test OK



AM board and chip status

Completed:

- mini-AMchip05 successfully designed and tested
- correct operation of serial links at 2 Gbit/s on mini-LAMB
- current consumption measured in different modes
- board level and crate level consumption still a concern
- AMchip05 redesigned to improve power performance; prototypes are under packaging

In progress:

- Test of AMchip05
- AMchip06 is being designed; expected area: 150 mm^2 (or even larger!)

The **FTK AMChip & AMBoard** collaboration:

- A. Andreani, A. Annovi, R. Beccherle, M. Beretta, R. Cipriani, S. Citraro, M. Citterio, A. Colombo, F. Crescioli, D. Dimas, S. Donati, P. Giannetti, K. Kordas, A. Lanza, V. Liberali, P. Luciano, D. Magalotti, P. Neroutsos, S. Nikolaidis, M. Piendibene, A. Sakellariou, S. Shojaii, C.-L. Sotiropoulou, A. Stabile

THANK YOU !