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Through Silicon Via Redistribution of I/O Pads

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Through Silicon Via Redistribution of I/O Pads for 4-Side Butt-able Imaging Detectors

Paul Seller[a*], Steven Bell[a], Matthew D. Wilson[a] and Matthew C. Veale[a]

***Abstract*– An 80x80 pixel ASIC for connection to CdTe detectors for spectroscopic X-ray imaging has been designed at the Rutherford Appleton Laboratory. The 20mm x 21.4mm ASIC is intrinsically 3-side butt-able when bump bonded to a 20mm x 20mm detector. The 4th edge has readout structures and the input/output (I/O) pads for wire bonding. This necessitates 3mm of inactive space between detectors on this edge when the detectors are tiled together. To reduce this lost space we have redistributed the I/O pads through the ASIC silicon substrate to the back of the ASIC and wire bonded on the back of the module. This wafer level technology step performed by Tohoku-MicroTec Co. Ltd. allows much greater area coverage for modular solid state detectors. The paper describes the process and results from first 8inch wafers of devices.**

Keywords: X-ray detector; CZT detector; Interconnect, X-ray imaging; Through Silicon Vias; small pixel.

I. Introduction

Cadmium Telluride and Cadmium Zinc Telluride Cd(Zn)Te based detectors have become the best prospect for room-temperature X-ray imaging detectors. They are being used for commercial applications in medical, security and science applications. Clearly one driver for this technology is to build large area devices to create X-ray cameras with a large focal plane.

There is an issue with the available and practical size of single detector segments. CdTe devices are available in many centimetre square devices but due to yield, large devices can have a cost premium. Available CdZnTe single crystals seem to be currently limited to an area of 20mm x 20mm. Also the thermal mismatch issues between Cd(Zn)Te and silicon poses problems for bonding of fine pitch imaging devices for very large areas. ASICs are limited by reticule size to just greater than 20mm x 20mm. All these constraints mean that a large focal plane area has to be build from smaller modules.

The Hexitec collaboration has built a readout system for fine pitch Cd(Zn)Te detectors suitable for imaging and spectroscopy [1]-[3]. We are now building 20mm x 20mm detector devices mounted on modules. These modules can be butted together on 3 sides but the 4th side has 1.4mm of readout components and wire bonds which require a dead space between detectors. The Through Silicon Via (TSV) technology [4]-[6] described here will allow us to create NxN multi module system with small inter module dead spaces.

(We refer to Cd(Zn)Te where the distinction between Cadmium Telluride and Cadmium Zinc Telluride is not important but use CdTe or CdZnTe where we wish to be specific.)

II. CdTe pixellated X-ray detector modules

Cd(Zn)Te detectors typically need to be 1 to 3mm thick for X-ray imaging applications to have good efficiency up to a few hundred keV photons. Figure 1 shows a prototype 1mm thick CdTe detector bump bonded to a Hexitec 80 x 80 pixel readout ASIC with the RAL technique of gold studs on the ASIC and silver loaded epoxy dispensed dots on the CdTe. The I/O pads of the ASIC are then aluminium wire bonded to the small 'door-step' readout board which is read out using the 34 way connector from the back of the module. This geometry can achieve 3 side butting but clearly from the Figure 1 there would be a large dead region for larger arrays, due to the wire bonding and the door-step card.

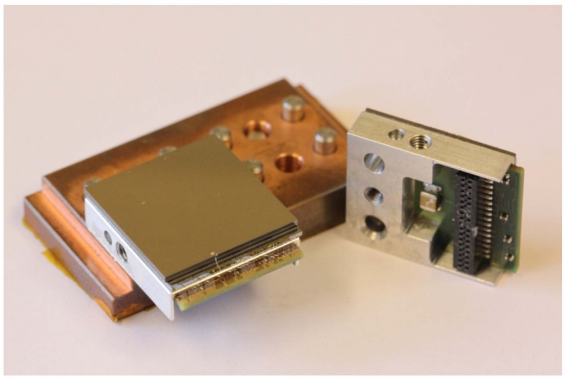

Figure 1: A 20mm x 20mm x 1mm CdTe detector bump bonded to the readout module.

The attachment point of the wire bonds cannot be very close to the CdTe due to the mechanics of the wire bonding machine. The current ASIC has two rows of bond pads; the outer row is required for wire bonding of the ASICs with a CdTe detector attached. Figure 2 shows the ASIC and the wire bonding to the outer row, the inner row appears as diamond shapes in the photograph due to the patterning of the metal surface. The 1mm thick CdTe detector is very close to the inner row. Also it can be seen how the CdTe is slightly wider than the ASIC and module mechanics allowing 3-side butting.

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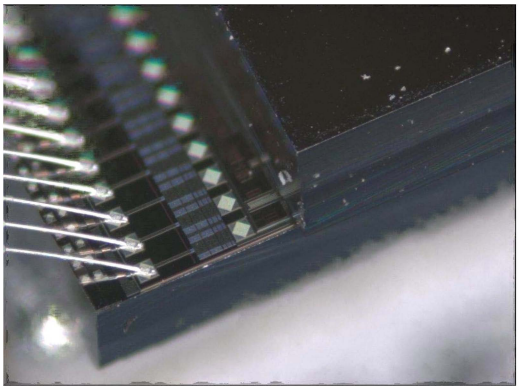

Figure 2: The conventional wire bonding geometry to the outer row of I/O pads on the detector side of the ASIC.

The current ASIC has 80 x 80 pixels [7]. Each pixel has a preamplifier followed by a 2µs CR-RC shaper and a peak-track-and-hold circuit. This circuit stores the peak value of the largest signal that occurs in the frame time. The signal represents the charge deposited in the detector and is thus proportional to the energy of the single photon stopping in the detector. This analogue voltage is held in the pixel till the end of the frame where it is transferred to the row outputs. The voltages from a row are driven to a multiplexor on the edge of the ASIC and the 80 columns of that row are multiplexed out to an off-chip ADC. The next row is then sent to the multiplexor. This is repeated until all rows are output. Each row is reset and activated immediately after row readout so that at the end of the frame the readout process can start immediately again with new data stored during the last frame readout time. The circuitry to control the multiplexing of the data and to drive the signals from the ASIC is contained on the same edge of the ASIC that has the I/O wire bonds.

III. Readout ASIC Pad Positions and TSVs

The 80 x 80 ASIC is mostly composed of the step-and-repeated 250µm x 250µm pixels. The edge readout circuitry and wire bond pads extend the ASIC by a further 1360µm on the readout edge as shown in Figure 3. The first row of pixel pads for connection to the CdTe can be seen on the extreme left and a single guard band bias pad can be seen 250µm away from this. Other power routing and multiplexing circuitry is accommodated in this area up to the first inner row of wire bond pads. The detector, when bonded will cover the guard band bias pad but not the inner row of wire bond pads. To the right of the inner row of bond pads are electrostatic damage protection diodes and then metal wires to the outer row of pads. Just past the protection diodes there is a seal ring which marks the edge of the functional ASIC.

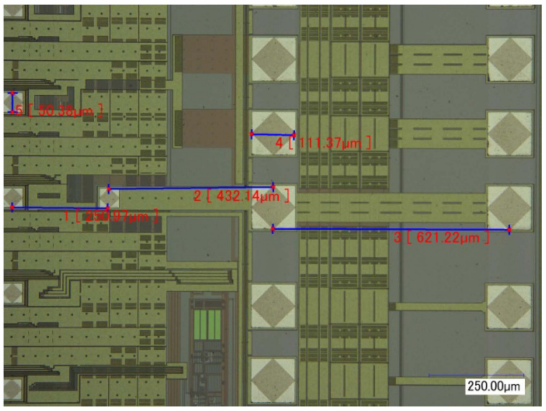

Figure 3: The readout edge of ASIC. From left to right, small pixel pads, single small guard pad, inner row of wire bond pads, seal ring line, outer row of wire bond pads to be cut off.

The 80 x 80 ASIC is being used in many systems using the conventional bonding to the outer row of wire bond pads as shown in Figure 2. The existing design included the inner row of pads in order to have separate pads for wafer level probe testing but also to investigate TSV technology. The aim of this trial is to make TSV connections from the inner row of pads to the redistribution pads produced on the back of the wafer which are then used for wire bonding. The outer row of pads can be removed with dicing to reduce the size of the ASIC.

Figure 4(a) shows the conventional bonding technique while 4(b) shows the tiling geometry which is enabled by TSV redistribution of the I/O connections. This current trial tests all the processes required to produce a new 4-side buttable ASIC. This next generation of ASIC will have compressed power supply distribution and multiplexor circuitry and smaller protection structures; this will reduce the distance from the pixel pads to the seal ring to less than 700µm. The edge circuitry and I/O pads will be covered by metal shield layer so that we can extend the detector over most of this area. In this arrangement the I/O pads for the TSV connection will not be visible from the detector side.

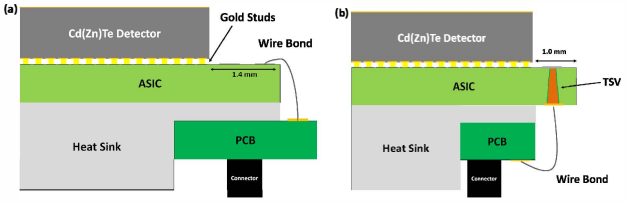

Figure 4: (a) Conventional detector bonding and (b) a bump bonded detector with TSV redistribution of I/O pads.

Two wafers of the existing 80 x 80 ASICs were processed at T-Micro [4] using a proprietary TSV and redistribution metal process. The 730µm thick AMS CMOS wafers were back thinned to 120µm and TSVs were processed to connect to redistribution pads on the back of the ASICs. Some of the ASICs were diamond saw diced and some stealth diced [8] to investigate minimum scribe lane loss. Figure 5(a) shows the

gold redistribution pads on the back side of an uncut ASIC with the TSV connections to the inner and outer wire bond pads clearly visible. The pads are on a 120µm pitch. 5(b) shows a side-on image of a laser cut through the pads and the relative thickness of the redistribution pads to the wafer thickness.

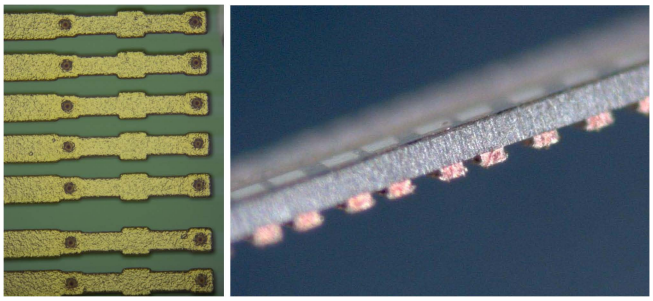

Figure 5 (a) The redistribution pads with TSV connections to inner wire bond pads in the middle of the image and TSV to outer wire bond pads on the right. The intended wire bond area is on the far left of the image. (b) A side view of a laser cut through the thinned wafer and redistribution pads.

IV. Measurements

Many detector modules have been tested using the conventional bonding configuration, the results of these measurements have been are reported previously [1], [9], [10]. The thinned TSV processed ASICs were mounted on a module with a revised 'door-step' circuit board as shown in Figure 6(a) and (b). This board has the same schematic as the conventional door-step boards but the wire bond pads are located on the reverse of the board to allow wire bonding to the redistribution pads.

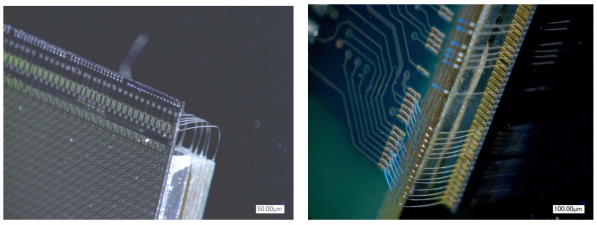

Figure 6: (a) The thinned ASIC with TSVs before the outer wire bond pads are removed. (b) A thinned ASIC with TSVs after the outer wire bond pads are removed, the image shows the reverse side of the module compared to (a).

Figure 6(b) shows the ASIC after removal of the outer pads using laser cutting; this process was completed after wire bonding. ASICs were also tested where the outer pads were removed by diamond saw cutting. After these cutting processes the devices were measured using calibration signals which exist on the input of each pixel of the ASIC. Before removal of the outer pads these devices had identical performance to conventionally bonded devices. No difference could be measured between a conventional device and a thinned device with TSVs wire bonded from the redistribution pads on the back of the ASIC.

Figure 7(a) shows the ASIC from the detector side with the outer wire bond pads removed using laser cutting. Note that the laser cut is performed on the outer side of the seal ring. After laser cutting and diamond sawing of the outer pads the ASICs were found to no longer function. To investigate this issue further, the inter-pad resistance of the outer pads was measured and found to be several Giga Ohms. This confirmed that the cutting of the aluminium and gold tracks had not caused the shorting of pads to other structures. In a separate test, two power/ground tracks were cut and the ASIC continued to function, however, after signal tracks were subsequently laser cut the ASIC failed. The reason for the failure is still unclear but it is suspected that the current induced by the UV light and heat of the laser may have caused electrostatic damage top the ASIC electronics. The outer pads of some ASICs were removed using a diamond saw. These ASICs were also found to be non-functioning. The diamond cutting was completed before wire bonding of the ASIC so it was not possible to test the functionality prior to processing. It is possible that the ASICs were not functioning before cutting.

Future ASICs will be designed with only a single row of I/O pads as shown in Figure 7(b). This single row of bond pads will remove the need for cutting which has been shown to damage the ASIC functionality. This single row of I/O pads will be shielded with a covering metal layer so that there is no electrical injection into the detector. This new design will not allow wafer level testing of the ASICs but otherwise the functionality will be identical to the existing ASIC.

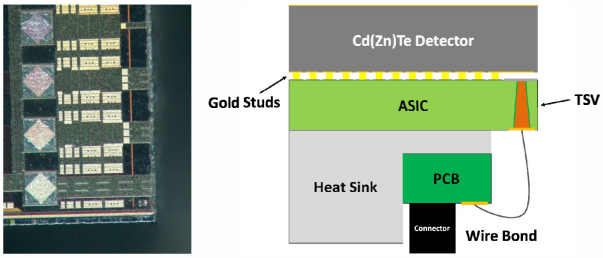

Figure 7: (a) The readout edge of the ASIC with outer wire bond pads removed by laser cutting. The laser cut is on the right hand side with the seal ring shown to the left of the laser cut. (b) The proposed 4 side butt-able geometry with bump bonded detector and TSV redistribution.

V. TSV Technology

The TSV process involves thinning the 200 mm diameter wafers by back grinding to 120µm. This is a convenient thickness so that the ASICs still have mechanical strength for wire and stud bonding but is thin enough to fabricate TSVs. The TSVs are then etched through the silicon from the back of the wafer, stopping at the first level metal of the pad structure. The process involved a Ga ion-etch combined with XeF_2 chemical etch. The important point was that the etching was not stopped by any structures under the pad metal and that it stopped at the back surface of the first metal layer of the ASIC. Following the etching a passivation layer was deposited on the silicon walls of the TSV followed by the deposition of the redistribution metal. Figure 8 shows

an optical image of a TSV and metal redistribution pad on the back of the wafer.

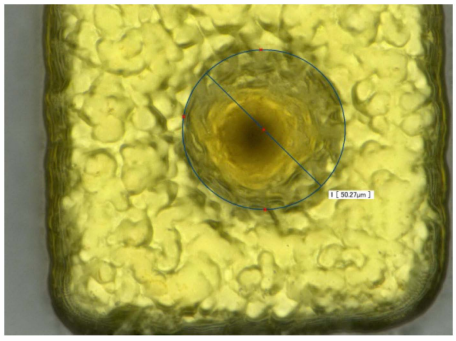

Figure 8: The 50µm conical TSV with the metal redistribution layers.

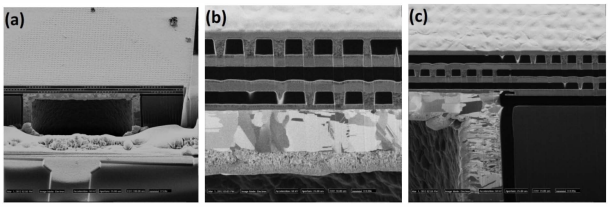

Figure 9: (a),(b) SEM images of the cross section of the TSV contact to the pad metal layers. c) corner of contact with no cracking.

Focused Ion Beam (FIB) and Scanning Electron Microscope (SEM) were used to investigate the structure of the TSVs and redistribution pads. Following the formation of TSV's, the FIB was used to mill through an I/O pad. The FIB trench exposed the different layers of the ASIC and the TSV; these were subsequently imaged using the SEM. These complimentary techniques proved important tools for investigating the quality of the TSV production.

Figure 9(a) shows a SEM image of the trench formed by the FIB milling of the ASIC I/O pad. All three of these images show the 4 metal layers of the ASIC and the vias connecting the individual layers. The vias between the first two metal layers and those between the top two layers can be seen in 9(b) while the remaining vias can be seen in 9(c).

In the images of Figure 9, the thick layer directly below the bottom aluminium layer, with its distinct crystal structure, is copper. Below this are several layers deposited using an electroless nickel/palladium/gold plating process. The TSV processing is completed with the addition of a layer of gold. The key points to note are the good electrical contact between the copper and aluminium layers at the bottom of TSV, the contact between the copper rerouting layer and the nickel/palladium/gold layers and the successful formation of a thick passivation layer between the silicon and the TSV (Figure 9(c)).

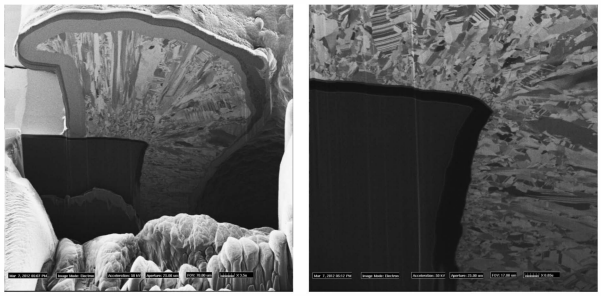

Figure 10: (a) SEM images of the cross section of the TSV redistribution pads on the back of the ASIC. b): An expanded SEM image of the cross section.

The passivation layer between the copper and the silicon of the TSV wall was low temperature PE-CVD SiO_2. The film quality produced using this technique can be inferior to that of high temperature CVD-SiO_2 but no problems were observed during these trials even during aluminium wire bonding to the redistribution metal on the back of the wafer. The passivation layer successfully isolated the TSV from the silicon as demonstrated by the ASIC functionality discussed earlier.

The redistribution pads on the rear of the ASIC were also investigated using the FIB\SEM technique. Figure 10 shows an example of a SEM image of a FIB trench through a redistribution pad and TSV. The copper and gold walls of the TSV can clearly be seen with no cracking observed at the edges of the TSV. On some of the ASICs artefacts between redistribution pads were observed; these can be seen in the microscope image in Figure 11.

These artifacts look like a failure to completely etch the gold when the inter-pad distance is small creating shorts between pads. The 200µm pitch vias had redistribution pads with a 50µm separation. For all devices the inter-pad gaps were free from artefacts. For vias on a 150µm pitch the inter-pad separation was reduced to 25µm and a number of devices showed artefacts. For this trial the shorts did not cause a serious problem as the closely spaced pads are redundant power connections but the size of the inter-pad separation will have to be carefully considered for future ASICs.

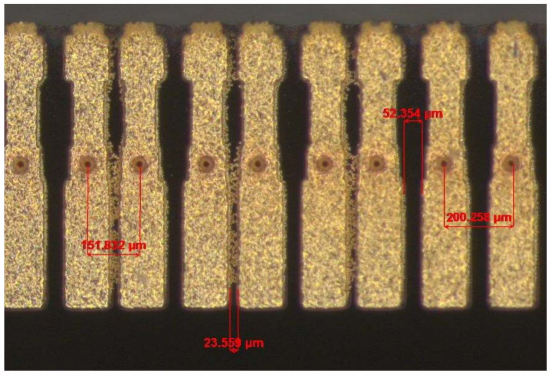

Figure 11: Gold redistribution pads with artifacts between pads.

VI. SUMMARY

We have built an 80 x 80 pixel Cd(Zn)Te based X-ray detector instrument capable of spectroscopic imaging based on a large area ASIC. We have demonstrated a wafer level back-end-of-line TSV process which allows the redistribution of the I/O pad interconnection to the back of the ASIC. This allows readout using wire bonding to the back of the ASIC which in turn leads to the possibility for reduced insensitive regions in tiled X-ray focal plane array sensors. The technology demonstrated here is conceptually simple but has a major implication for the future of focal plane imaging detectors.

Because of the failure of laser and diamond saw cutting of active I/O lines, the next 8080 X-ray imaging ASIC intended for 4-side butting will be built with a single row of shielded I/O pads. This successful T-Micro TSV process will be used to redistribute the wire-bond pads to the back of the ASIC.

ACKNOWLEDGMENT

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