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SLID Interconnected n-in-p Pixel Modules with 75 Micrometer Thin Silicon Sensors

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Abstract

The performance of pixel modules built from 75 micrometer thin silicon sensors and ATLAS read-out chips employing the Solid Liquid InterDiffusion (SLID) interconnection technology is presented. This technology, developed by the Fraunhofer EMFT, is a possible alternative to the standard bump-bonding. It allows for stacking of different interconnected chip and sensor layers without destroying the already formed bonds. In combination with Inter-Chip-Vias (ICVs) this paves the way for vertical integration. Both technologies are combined in a pixel module concept which is the basis for the modules discussed in this paper.

Mechanical and electrical parameters of pixel modules employing both SLID interconnections and sensors of 75 micrometer thickness are covered. The mechanical features discussed include the interconnection efficiency, alignment precision and mechanical strength. The electrical properties comprise the leakage currents, tunability, charge collection, cluster sizes and hit efficiencies. Targeting at a usage at the high luminosity upgrade of the LHC accelerator called HL-LHC, the results were obtained before and after irradiation up to fluences of 10^{16} n_{eq}/cm^2 (1 MeV neutrons).

Keywords: Pixel detector, Solid Liquid InterDiffusion, 3D-Integration, Thin sensors, HL-LHC, Radiation hardness

1. Future Pixel Modules and 3D-Integration Technology

The ATLAS pixel detector [1] is built from 1744 pixel modules comprising three barrel layers located at radii from the beam line between 50.5 mm and 122.5 mm as well as three end-cap discs on each side of the detector. Each module consists of 16 FE-I3 read-out chips [2] which are interconnected via the solder bump bonding technique [3] to a 250 μm thick n-in-n planar silicon sensor. The size of individual pixel cells is 50 μm $\times$ 400 μm. Sensors and read-out chips are specified for a maximum fluence of 10^{15} n_{eq}/cm^2 (1 MeV neutrons) and a dose of 500 kGy.

A large upgrade to the LHC accelerator chain is planned culminating at around the year 2022 in the so called HL-LHC. The peak luminosity will eventually be increased up to $5{\cdot}10^{34}$ $cm^{-2}s^{-1}$ [4]. To maintain the detector performance, several upgrades of the ATLAS pixel detector are planned. The first of these upgrades, the so called Insertable B-Layer (IBL) [5], is a new fourth pixel layer, which is planned to be mounted on a new smaller beam pipe at a radius of 32 mm, and to be operational by the end of 2014. Due to the smaller radius, the modules cannot overlap along the beam direction as they do for the present ATLAS pixel detector. Thus, the active fraction of the new pixel modules was increased [6–8]. Additionally, the harsher radiation environment and the higher occupancy demanded for a new read-out chip, the FE-I4 [9], specified up to a received fluence of $5{\cdot}10^{15}$ n_{eq}/cm^2 and with a reduced pixel size of 50 μm $\times$ 250 μm. Furthermore, the number of pixel cells increased from 2880 to 26880 per chip. While it is expected that the upgraded pixel detector retains sufficient tracking capabilities until around 2022, a full replacement of the tracking detector is required afterwards. Given the extreme radiation levels of up to $2 \cdot 10^{16}$ n_{eq}/cm^2 in the innermost layer a new generation of read-out chips will be needed for the inner layers, featuring even smaller pixels to cope with the otherwise largely increased pixel occupancy. The current baseline detector layout [10] consists of four pixel layers in the barrel part, with a minimal radius around 39 mm and a maximal radius around 250 mm. In addition, six pixel discs are foreseen for the forward region, i. e. at a pseudo-rapidity range of about $1.8 \leq |\eta| \leq 2.8$. Depending on performance simulations, it is planned to further increase the maximal radius, or to add an additional fifth pixel layer.

1.1. Module Concept

To answer the challenges of this upgrade, a module concept for the pixel layers is investigated, which employs several novel technologies in the field of pixel detectors: n-in-p pixel sensors are thinned using a Max-Planck-Gesellschaft Halbleiterlabor (MPG-HLL) developed process [11] and connected via the Fraunhofer EMFT [12] Solid Liquid Inter-Diffusion (SLID) technology to the read-out electronics, where the signals are routed via Inter-Chip-Vias (ICVs). Additionally, the active fraction is maximised by an optimised guard ring design in combination with or without implanted sensor sides [13]. In Figure 1 the schematics of (a) the present and (b) the investigated concept are shown.

Advantages of this approach are: the n-in-p technology allows for single sided processing of wafers resulting in a lower cost, which is of special importance for the large areas foreseen in future pixel detector upgrades. In addition, the radiation

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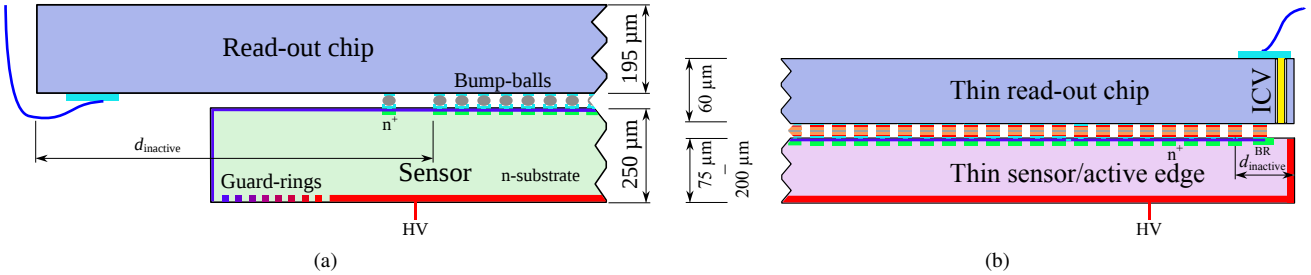


Figure 1: (a) Schematics of the current pixel detector module within the ATLAS experiment and (b) the investigated design. The read-out chip is shown in blue, the sensor in light green (violet) for the current (new) concept. The pixel implants as well as the bias ring n^+-implants are indicated in green, where the implant closest to the edge is the bias ring implant. The back-side implantation, and for the new concept also the edge implantation, is indicated in red. Wire bond pads are drawn in light blue, ICVs in yellow.

hardness is comparable to the presently used n-in-n technology [14, 15]. Thinner sensors not only reduce the material budget and therefore multiple scattering but also, at the same applied bias voltage, they exhibit higher electric fields than thicker devices. This leads to a high charge collection efficiency (CCE) after high radiation doses at moderate bias voltages [15–17]. While on the sensor side the inactive area is removed by activated edges, in a 3D compliant design of the pixel electronics, ICVs could eventually avoid the need for the cantilever area where presently the wire bonding pads are located. Combining these ICVs with SLID interconnections enables fully 3D-integrated modules. Furthermore, SLID interconnections could allow for a pitch reduction with respect to the 50 μm pitch limit given by the solder bump bonding.

In this paper results on the SLID interconnection and thin sensor aspects of this module concept are presented and discussed. Some preliminary results were already given in [18–22] as well as in the PhD-theses [15, 23]. All SLID modules presented here use the FE-I2 [24] ATLAS readout chip that has the same footprint as the FE-I3 chip. The two chips only differ in minor details, e. g. they need slightly different chip analogue and digital voltages documented in [25]. These differences are not relevant for the work presented in this paper. Consequently, in the following no distinction is made and both chips are referred to as FE-I3 chips. Further results on the other technologies used in the module concepts, as n-in-p sensors, active edge pixel devices and ICVs, can be found in [13, 15, 23, 26].

In the presentation of the results first a short introduction to SLID will be given, followed by the technical and mechanical results. Finally, the performance for prototype pixel modules employing SLID and 75 μm thick sensors will be discussed and compared to results from modules exploiting bump-bonding, and other sensor types.

1.2. Solid-Liquid InterDiffusion

SLID is a class of interconnection techniques, where the formation of the interconnection takes place at temperatures significantly lower than the ones the connections can withstand afterwards without dissolving. The concept was introduced in the 1960s [27, 28] and is based on binary, ternary, or even higher-order metal systems, where one low-temperature melting metal is coated on a high-temperature melting core. By bringing the temperature of the metal system above the melting point of the low-temperature melting metal and applying high pressure, this metal dissolves and diffuses into the high-temperature melting metal. Inter-metallic compounds with melting points above the heating temperature are formed by the two metals and the liquid phase solidifies. While many different metal systems are known to form SLID bonds, certain constraints apply when using this technique in real applications [29]. For example, the melting point of the low-temperature melting metal should be below 400 °C, which is the maximum temperature most Application Specific Integrated Circuits (ASICs) can withstand. In the presented module concept, the SLID process developed by the EMFT is used. The process steps are shown in Figure 2. In this approach Sn (T_{melt} = 231.9 °C) is used as the low-temperature melting component and Cu (T_{melt} = 1083.0 °C) as the high-temperature melting component. Out of these, Cu_3Sn (T_{melt} = 676 °C) and Cu_6Sn_5 (T_{melt} = 415 °C) are formed. The high melting point of the interconnecting alloy opens the possibility of subsequent stacking of additional SLID-interconnected layers, but at the same time inhibits the re-work of badly connected devices.

A comparison of the process flows of the conventional bump bonding techniques and SLID, shown in Figure 3, reveals further advantages and challenges. While the first step is a patterned electroplating step needed for the deposition of the Cu and Sn, which is similar for both technologies, the so-called reflow step is not needed to form SLID interconnections. In the reflow step, the alloy or metal, e. g. PbSn or In that are used in the bump bonding process is melted; the surface tension leads to solder ball formation. Since the diameter of the balls is determined by the initial pad size, all bump-bond connections have to be of equal size to form good connections (compare 3rd connection to the neighbouring ones in Figure 3). In contrast, a SLID bond can have an arbitrary shape and size, with the only constraint that its dimensions exceed 5 μm by 5 μm. Additionally, the reduction of one process step is expected to lower the costs once the process is established in industry. In the interconnection-step the read-out chip and the sensor are brought together. In the bump-bonding process a built-in self alignment due to the surface tension of the bump-balls is exploited, while the SLID interconnection has to rely on the pick-and-place precision for the placement of the read-out chips on

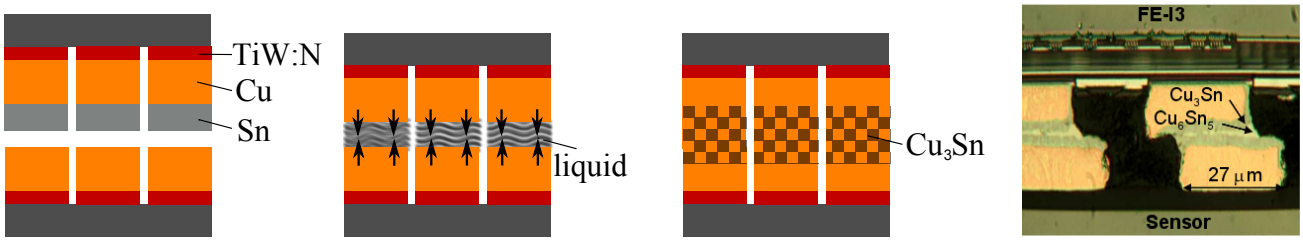


Figure 2: (a-c) Process flow of the SLID interconnection, adapted from [29]. For an explanation of the individual steps please refer to the text. (d) Cross section of SLID pads in a pixel module built from an FE-I3 read-out chip and a dummy sensor (aluminium and silicon oxide only). Photograph taken by [12].

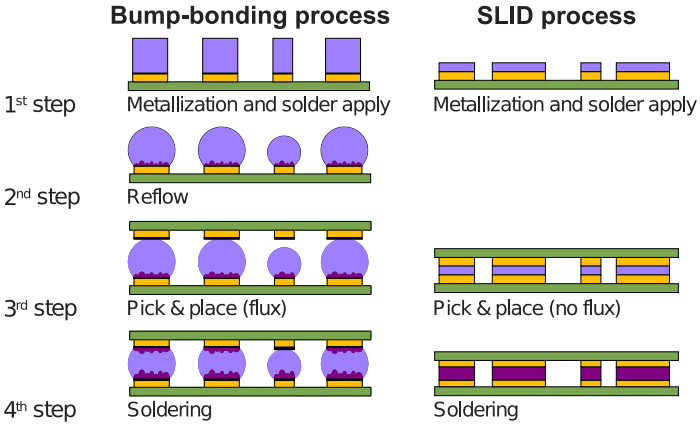


Figure 3: Step-by-step comparison of the bump-bonding and SLID interconnection technologies [12].

the handle wafer, when the technique is applied in the chip-to-wafer approach. If a high accuracy can be achieved in the pick-and-place procedure, the pitch of the SLID connections can be as low as approximately 20 μm [30], which is not possible for the bump-bonding offered for industrial applications. In the final step, the actual bond is formed by pressing the two layers together. While a non functional bump-bonded module with a broken read-out chip or sensor can be separated again for repair by reheating, due to the larger temperature needed this is not possible for SLID assemblies.

Other innovative interconnection technologies are presently investigated for pixel modules for use in high energy physics experiments. These are the Ziptronix Direct Bond Interconnect (DBI) oxide bonding and the copper thermo-compression [31], both under evaluation at Fermilab, and also the copper pillar interconnects [32], offered by CEA-LETI [33].

2. Technical Aspects and Mechanical Properties

2.1. Influence of the SLID Process on Silicon Sensors

Since the SLID interconnection was only known to work with integrated circuit (IC) devices, a production of diodes subjected to the SLID metallization and temperature treatment was carried out. Compared to IC devices, the performance of sensors that are usually made from high resistivity silicon, is much more sensitive to high leakage currents caused by a diffusion of copper atoms into the silicon bulk. In the SLID process, to prevent diffusion of copper into the silicon bulk a barrier layer of Titanium Tungsten (TiW) is needed. The diodes were used to verify the functionality of this TiW diffusion barrier with thin silicon sensors.

To model both sides of the SLID metallization, two 6-inch wafers with various thin p-in-n diodes were produced. The sensor concept uses an SOI technology with an active sensor wafer that can be thinned to a desired thickness, and that is oxide bonded to a handle wafer for mechanical stability. The p-in-n option was chosen since no difference in the sensitivity of p-in-n and n-in-p sensors towards copper atoms is expected and the n-type wafers were easily procurable. The implemented diodes have an area of 10 mm^2 with different guard-ring designs and are thinned down with the HLL thinning technology to an active thickness of 50 μm. Together with the handle wafer, the total thickness of the wafers is 500 μm.

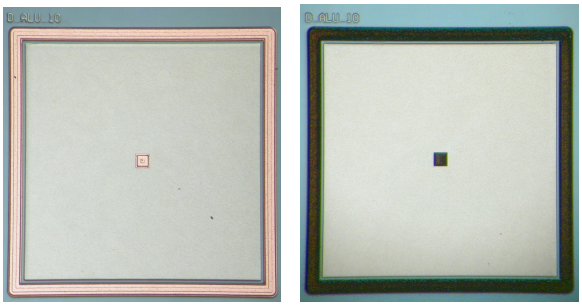


Figure 4: Photographs of thin p-in-n diodes used to test the performance of the TiW diffusion barrier. The Cu can be seen as a pale orange surface while the Sn appears black under the coaxial illumination.

On both wafers shown in Figure 4, a 100 nm thin layer of TiW was applied to the aluminium contact pads of all diodes, followed by an electroplating of Cu. For the first wafer, shown in Figure 4(a), the thickness of the Cu is around 1 μm and no further layers are applied. The second wafer, which is displayed in Figure 4(b), was equipped with 5 μm of Cu and 1 μm of Sn. Hence, both sides of the SLID metallization are replicated separately. The reduced thickness of the Cu layer on the first wafer of 1 μm, compared to the 5 μm used in the SLID interconnec-

tion, is assumed to be sufficient for an investigation of the full impact caused by a possible copper diffusion. For the second wafer, the thickness of the Sn was chosen to be a little less than half of the 3 μm used in the SLID process. This ensures, that the Sn can be completely absorbed by the single Cu layer of the wafer.

In a first step the leakage currents of the diodes were measured before the application of any SLID metal layers. The same diodes were measured after the application of the TiW and Cu for the first wafer and TiW, Cu, and Sn for the second wafer. Shown in Figure 5(a) are the ratios of these leakage currents of the measured diodes of both wafers obtained after various production steps and at 50 V. The currents were determined by a linear fit to the plateau region of the leakage current characteristics. The uncertainties assigned are the combination of the one standard deviation uncertainties calculated from the measurement uncertainties of the Keithley-487 picoamperemeter [34] and the fit uncertainties. The leakage currents of the diodes on both wafers do not increase to a level that could be dangerous for the sensor operation. On wafer 1, the average current of the diodes at 50 V is unchanged while on wafer 2, it increases by about 51%. Removing the outlier from the analysis, which showed a defect not related to the SLID interconnection, an average increase of only 18% is found. These measurements show that during the application of the SLID metallization no copper diffuses into the sensor, since this would lead to an increase of the leakage current by several orders of magnitude.

In a next step, both wafers were heated in the standard processing atmosphere to 320 °C for 15 min to simulate the SLID temperature treatment, and to start the solid-liquid interdiffusion of the Sn into the Cu. An actual connection of the wafers was not performed. After the temperature treatment the leakage currents of the diodes showed a slight decrease, as shown in Figure 5(b). Compared to the measurements before any SLID processing steps, the currents are only 69% and 73% of the initial values for wafer 1 and 2, respectively. This is expected to be due to the annealing of defects in the silicon bulk caused by the applied temperature.

2.2. *Alignment Precision and Interconnection Efficiency of the SLID Interconnection*

One of the key performance parameters to judge the applicability of the SLID interconnection technology is its connection efficiency p. It is defined as the probability that a given single SLID interconnection is successful. The corresponding inefficiency, i. e. the probability $p_{\text{not}} = 1 - p$ of a fault of a given connection, is the figure of merit commonly used and given in the results below. To calculate the inefficiency from measurements of structures with a group of serial SLID interconnections, a binomial probability distribution is assumed. From the number n of SLID interconnections per group and the fraction P of groups with all connections working,

$$p_{\text{not}} = 1 - P^{1/n} \tag{1}$$

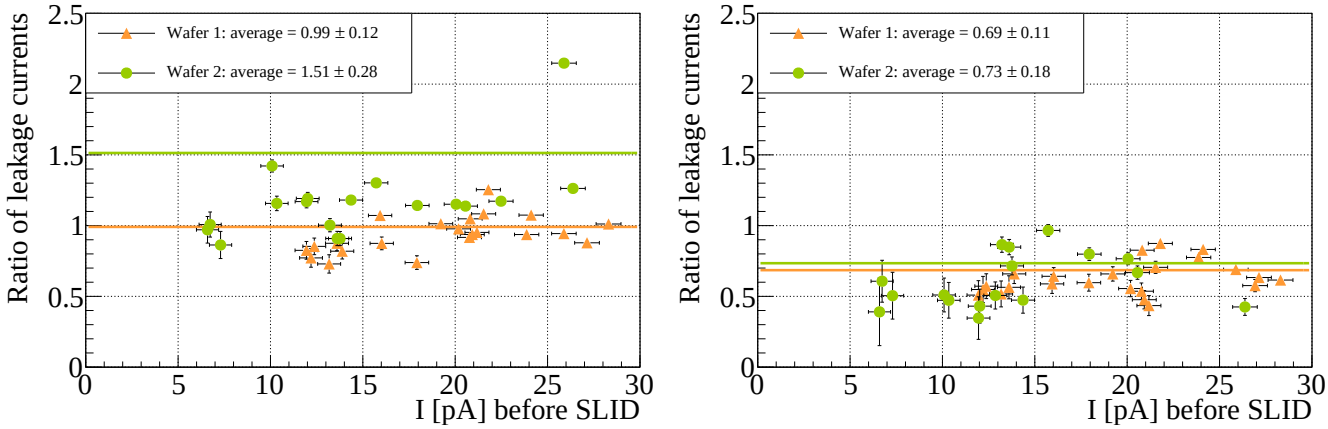
is derived. The inefficiency should be as low as possible; for example it was required to be smaller than 10^{-4} for the present ATLAS pixel modules [35].

To measure p_{not} of the SLID interconnection, its dependence on the alignment precision, and the sensitivity to disturbances of the device planarity, a SLID prototype production was carried out. For this, a 6-inch-wafer layout designed at the MPP, and shown in Figure 6(a), was used. The layout includes a total of 152 test devices, which rely solely on structured metallization directly on the SiO_2 but do not have any implants. The SLID contact positions, shown in Figure 6(b), are symmetric with respect to the x-axis and hence, two of these wafers can be connected by rotating one around its symmetry axis by 180° and placing it onto the other. Through this, the 76 devices in the northern half of one wafer, which are referred to as sensor devices, are connected to the 76 chip devices of the southern part of the other wafer.

A large fraction of the area of each device is filled with daisy chains which are a serial wiring scheme of a large group of SLID interconnections in a row with alternating aluminium traces on the sensor- and chip-side, as shown in Figure 6(c). If a potential difference is applied to the ends of a daisy chain, a current can only flow provided all SLID interconnections are functional. Hence, a large number of SLID interconnections is tested at the same time. The daisy chains of the 76 devices of the sensor side are equipped with aluminium traces leading to contact pads for needle probes at the ends of the daisy chains. On the chip devices, there are no traces since this part of the devices is cut off during the singularization to enable access to the contact pads of the sensor devices. Hence, after connecting two wafers only those 76 structures can be used where the sensor devices are on the lower wafer which is not cut.

Rows 1 and 2 of larger devices above the horizontal wafer axis contain daisy chains which have the same geometry as an ATLAS pixel sensor. This means that the metal traces occupy the same areas as the pixel implants do in the sensors. In addition, aluminium lines are implemented to connect every second pair of traces to form an open chain. The SLID interconnection of open chains from chip and sensor devices leads to closed, i. e. conducting chains, as shown in Figure 6(c). In row 1, the SLID pad size is $27 \times 58\,\mu\text{m}^2$ with a small pitch of 50 μm and a large pitch of 400 μm. This corresponds to the SLID pad dimensions used for the prototype pixel modules discussed below. The chains of row 2 have identical pitches but the SLID pads are of similar size as the n-type implants in the ATLAS pixel sensors, i. e. $27{\times}360\,\mu\text{m}^2$. Within the smaller devices in rows 3 to 6 of the wafer, a variety of SLID pad sizes and pitches are implemented in different daisy chains. They range from $30 \times 30\,\mu\text{m}^2$ with a pitch of 60 μm to $80 \times 80\,\mu\text{m}^2$ with a pitch of 115 μm as detailed in Table 1. In addition, in rows 3 and 4 special chains are implemented which have a part, where deliberately either the SiO_2 or the aluminium layer is missing. This leads to a lowering of the SLID pads by 100 nm or 1 μm as illustrated on the right side of Figure 6(c). With these degradations of the device planarity the sensitivity of the SLID interconnection to surface imperfections is investigated.

Furthermore, electrical and optical alignment structures are introduced in the devices. The electrical alignment structures consist of SLID pads that are only connected if the devices are misaligned. A section of the wafer map containing one of the



(a) (b)

Figure 5: Ratio of leakage currents of the thin p-in-n diodes with respect to the untreated diodes as a function of the leakage current. The ratios are shown in (a) after the application of the SLID metallization and in (b) after the SLID temperature treatment.

Pad size [μm^2]	Pitch [μm]	Aplanarity [μm]	Connections measured	Inefficiency $p_{not}[10^{-3}]$
30×30	60	–	8288	< 0.36
80×80	115	–	1120	< 2.7
80×80	100	–	1288	< 2.3
27×60	50, 400	–	24160	0.5 ± 0.1
30×30	60	0.1	5400	1.0 ± 0.4
30×30	60	1.0	5400	0.4 ± 0.3

Table 1: Geometrical parameters and performance of various SLID interconnection options.

alignment structures which measures a misalignment of (2.5–15) μm is shown in Figure 6(d). The structures shown in green are located on the sensor wafer, while those drawn in red are on the chip side. Depending on the size of the misalignment different counterpart pads match, and are electrically conducting, which is verified with probe needles on external pads. Further alignment structures on each device allow for measuring a misalignment of up to 30 μm. The optical alignment structures are aluminium vernier scales that are implemented partly on the sensor- and partly on the chip side of the packages, as shown in Figure 7. Using an infra-red microscope they allow to determine the relative misalignment with an accuracy of 3 μm. The measurements of the SLID daisy chains were carried out with a Keithley-6517A electrometer [34], supplying a small voltage to the ends of the chains and measuring the current. Through this, also the resistance of the chains are measured and a mean resistance per SLID connection is determined. Using an infra-red microscope the relative misalignment is determined.

2.2.1. *Wafer-to-Wafer Interconnection*

The wafers were interconnected in a wafer-to-wafer approach. For the majority of the chains all SLID connections were functioning resulting in finite resistances ranging from $(0.25 \pm 0.12)\,\Omega$ to $(1.5 \pm 1.7)\,\Omega$ per SLID connection, where the uncertainties are the one standard deviations of the measurements from various equivalent chains. The chain resistances do not directly correlate to the size of the SLID pads but rather to the number of SLID connections per row ranging from 46 to 302 connections. This leads to the conclusion that the dominating contribution to the resistance is not caused by the SLID metal layers, but rather by the contact between them and the aluminium traces. This contact is made by creating an opening in the BCB passivation layer covering the whole wafer, displayed in Figure 6(c), and it has the same diameter for all pads of all chains.

Table 1 summarizes the results of all daisy chain measurements and includes the total number of SLID connections tested. The SLID inefficiency is less than 10^{-3} for most of the chain types. In those cases, where no interrupted contacts were found, an upper limit at a 90% confidence level is reported. This was the case for almost all daisy chain types without the variations in the SLID pad height, introduced by missing layers of aluminium or SiO_2. Only in the case of the structures of row 1 where 24160 contacts were measured, 10 out of 80 chains with 302 connections each were interrupted. Those chains which have a variation of the SLID pad height also show small inefficiencies comparable to the other chains. Even the chains with the missing aluminium below the SLID pads result in a connection inefficiency per pad of $(0.4 \pm 0.3) \cdot 10^{-3}$, clearly showing that the SLID interconnection is not severely affected by variations of the surface planarity up to 1 μm.

The optical inspections of the vernier scales as well as the measurements of the electrical alignment structures showed a very good alignment accuracy of better than 5 μm for the first and about (5–10) μm for the second pair of interconnected wafers.

2.2.2. *Chip-to-Wafer Interconnection*

In another prototype run ATLAS FE-I3 read-out chips were interconnected to fully functional thin pixel sensors. The sensors were produced on p-bulk FZ wafer using the MPG-HLL

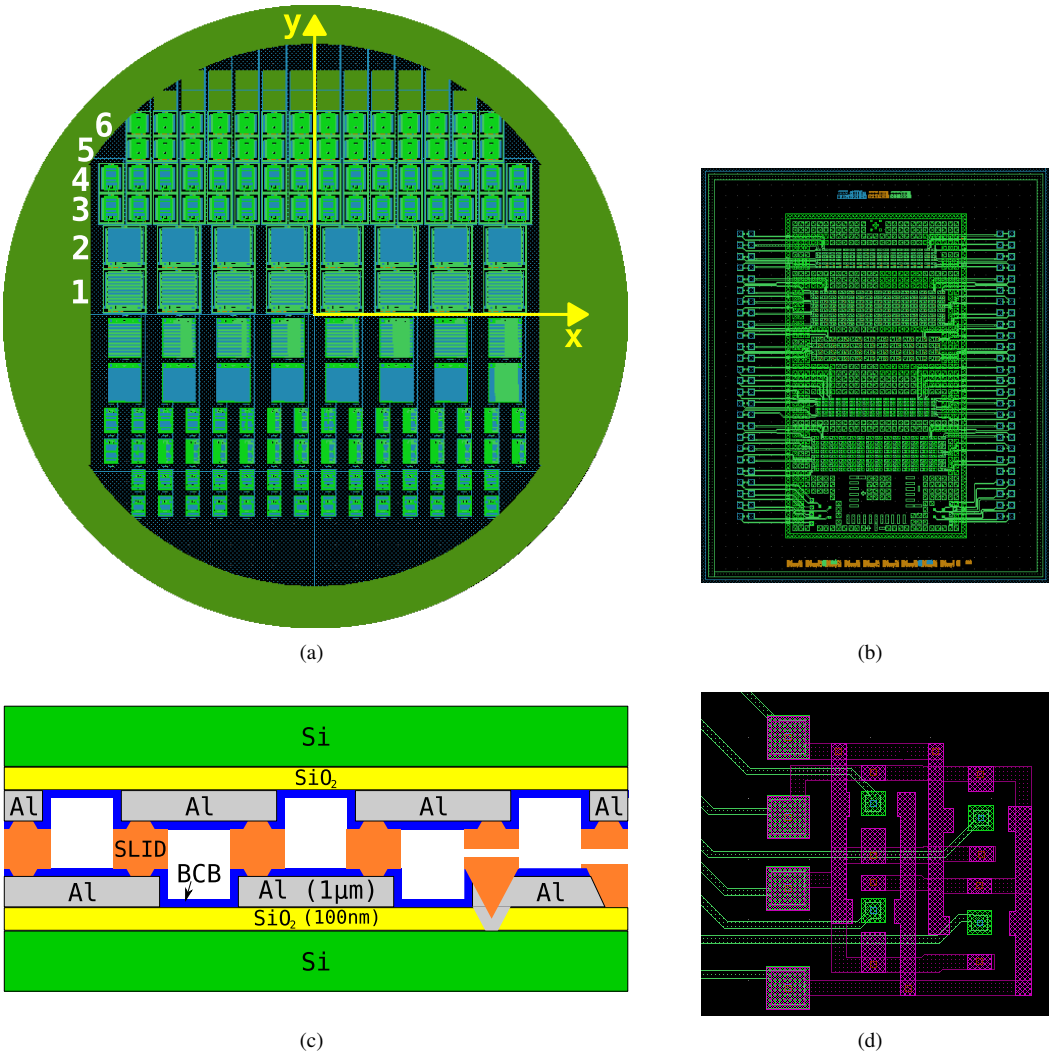


Figure 6: An overview and detailed schematics of the SLID prototype production. In (a) the wafer map of the SLID dummy devices is shown, (b) shows a sensor device with the contact pads for the probe needles. In (c) the schematics of an individual daisy chain is displayed, and finally, (d) shows an electrical structure to verify the mechanical alignment.

thinning process with a final active thickness d_{active} of 75 μm. The specific resistivity of these wafers is $\rho \geq 2\,\text{k}\Omega\text{cm}$. A discussion of the electrical characteristics of all structures within this production can be found in [23]. The full depletion voltages V_{fd} were found to be (30 ± 5) V, with the exception of one pixel device that did not reach a plateau in the leakage current, i. e. where the breakdown voltage V_{bd} was lower than V_{fd}. This corresponds to a yield of $79/80 \approx 98.8\%$. For the 79 pixel devices, an overdepletion $V_{\text{bd}}/V_{\text{fd}}$ of 3.7 ± 1.0 up to 15 ± 2 can be reached. Finally, their leakage currents in the plateau region were determined to be below $10\,\text{nA/cm}^2$.

For the interconnection, a handle wafer was populated with known working read-out chips at the positions of compatible pixel structures on the sensor wafer side as indicated by the red numbered rectangles in Figure 8. Due to the high applied pressure in the process, a homogeneous population of the handle wafer is mandatory, thus, the rest of the handle wafer was populated regularly with read-out chips (indicated in black). The electroplated SLID pad structure is the same for the working and for the dummy read-out chips. An excellent alignment of the read-out chips on the handle wafer is needed, given the small pitch and SLID pad sizes in combination with the needed minimal overlap of $5\,\mu m \times 5\,\mu m$. Additionally, it is important that rotations of the read-out chips are below about 0.5°. Although, a global misalignment can be corrected for by adjusting the relative position of the two wafers in the interconnection process, these requirements demand cutting-edge pick-and-place technology.

The positions of the alignment marks (cross and circle) are indicated in red in Figure 9(a). In Figure 9(b), an infra-red picture of a cross alignment mark is depicted for a connected stack. Based on these images, the quality of the alignment was determined after interconnection. The residual misalignment after interconnection is summarised in Table 2. In total, six out of ten assemblies were built successfully, i. e. without shorts or open connections caused by misalignment. For the assemblies

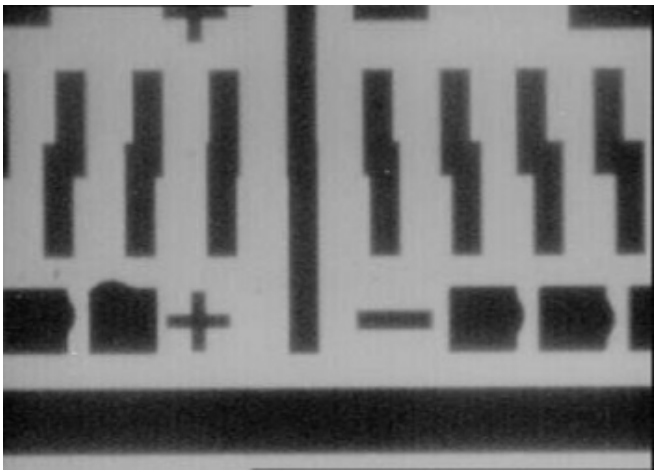


Figure 7: Infra-red image of a well aligned vertical alignment vernier scale. A perfect alignment is reached if only the central long aluminium lines of both wafers completely overlap. For each 6 μm of misalignment, the lines that completely overlap are shifted by one to the left or right.

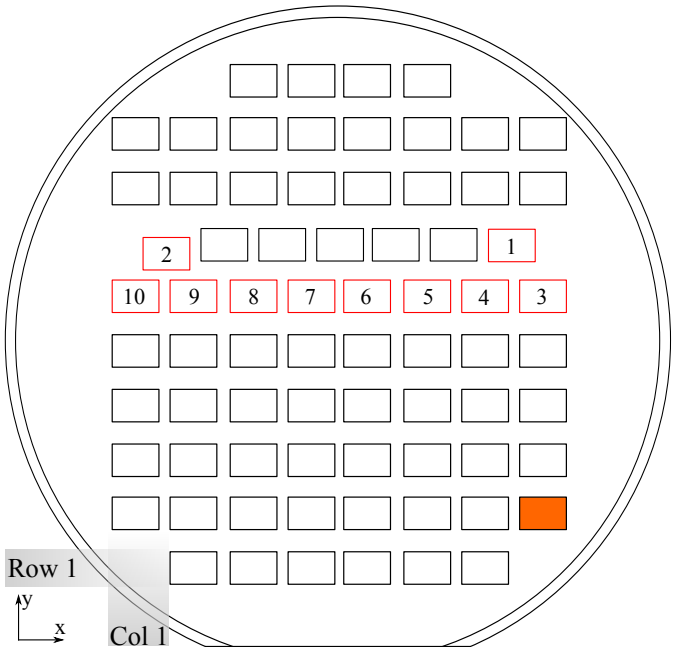
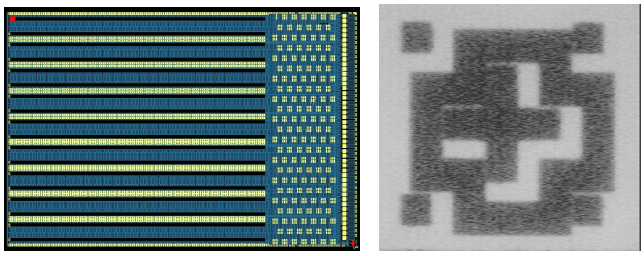


Figure 8: Population layout of the handle wafer. Read-out chips corresponding to a compatible sensor in the wafer layout are indicated in red. The given numbers indicate the modules for further reference. Dummy read-out chips for mechanical stability are drawn in black. The read-out chip indicated in orange is missing. The coordinate system referred to in the following is also indicated.

2, 4 and 5 the misalignment is too large for the pixel assemblies to be functional. To improve the precision of the alignment for future productions, a new and more precise pick-and-place machine will be employed. Additionally, the possibility to exploit self alignment via evaporative liquid glues while populating the handle wafer is currently investigated at the EMFT.

Open connections were identified with a high statistics radioactive source measurement in which not connected pixel cells exhibit a low hit rate, because they can only contribute



(a) (b)

Figure 9: (a) SLID pad distribution over the FE-I3 read-out chip (yellow rectangles). The alignment marks are indicated in red. The pad is in the upper left corner, the cross is in the lower right corner. (b) Infra-red image of an alignment cross after interconnection. The cross has a total dimension of 150 μm in both directions.

Module	Δx [μm]	Δy [μm]	Tilt [°]	Connected [%]
1	−6	−22	−0.25	100
2	−139	−40	−0.25	
3	−23	−34	−0.38	100
4	44	73	0.72	
5	−34	−58	−0.61	
6	−8	−19	−0.21	$70.1^{+0.3}_{-0.3}$
7	−16	−18	−0.21	$66.5^{+0.4}_{-0.4}$
8	−17	−25	−0.23	$88.7^{+0.3}_{-0.5}$
9	−17	−21	−0.24	$94.5^{+0.1}_{-0.3}$
10	−16	−25	−0.26	100

Table 2: Residual misalignment of the alignment cross for the interconnected modules and the fraction of connected pixel cells. For the definition of connected and the evaluation of uncertainties, please refer to the text. Assemblies 2, 4 and 5 were not investigated due to their misalignment.

via electronic noise, but not via genuine signal. For the used statistics, and in the centre of the beam spot, around 150 events per pixel are expected. A pixel cell is defined as connected, if it exhibits more than 50 hits. Uncertainties are assessed by varying this threshold by ±10%. The percentages of connected pixel cells per module are summarised in Table 2. While for module 1, 3 and 10 all pixel-cells are connected, module 6 exhibits around 30% of not connected pixel cells. A trend of the fraction of not connected channels to rise towards the centre of the wafer is found.

Subsequent optical re-inspections of not yet connected sensor wafers from the same production revealed that the cause for these not connected pixel cells is an imperfect opening of the BCB passivation layer underneath the SLID pad. Photographs of such not fully opened layers are depicted in Figure 10(a) and Figure 10(b). For future module assemblies, a removal of residual BCB in the openings using an SF_6 plasma descum process offered by the Fraunhofer IZM [36] was investigated. In the optical inspection after the treatment all BCB contacts were found to be fully opened. Figure 10(c) and Figure 10(d) are photographs of fully opened contacts. Thus, this is not an issue for future productions.

Another crucial factor is the stability of the connections in experimental conditions, where, in addition to high radiation

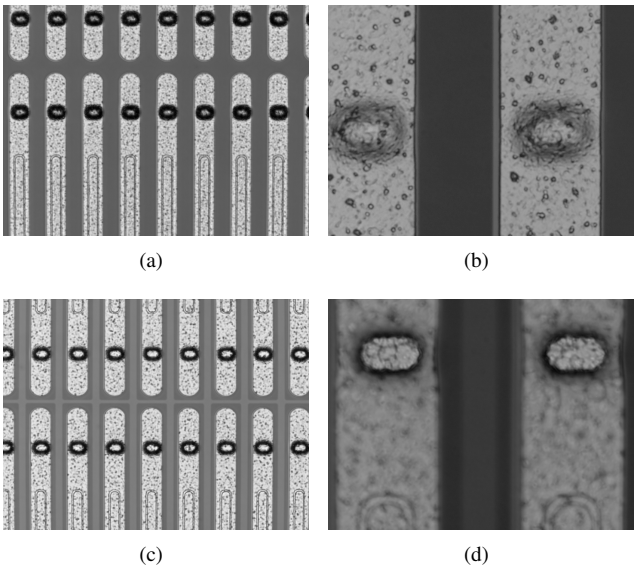


Figure 10: Photographs of (a, b) an insufficiently opened BCB passivation layer in the position corresponding to the SLID pads, and (c, d) a fully opened BCB passivation layer. The horizontal distance between two openings is 50 μm in all photographs.

levels, temperature cycles are present. Within the laboratory and during beam test measurements for all modules the numbers of not connected pixel cells did not change with numerous thermal cycles between 20 °C and −50 °C. Furthermore, no changes after irradiation up to a fluence of 10^{16} n_{eq}/cm^2 were observed. This is a strong indication that SLID interconnections are radiation hard and withstand thermal cycles.

2.3. Mechanical Strength

A high mechanical strength is desirable for an interconnection technology, as it eases the handling of the device, ensures that bonds do not break accidentally, and that they are stable in time. To determine the mechanical strength, a piece of plexiglass was glued onto each dummy read-out chip (black in Figure 8) in the lower half of the handle wafer. Subsequently, weight was hanged onto the plexiglass holder while the sensor wafer was stabilised in its position by a plexiglass support covering the full area except for the region around the read-out chip under study. After each increase of weight the strain was relieved using a small hoisting platform to apply the force in a controlled manner. Before adding the next weight the hoisting platform was lifted again. A photograph of the setup is depicted in Figure 11. Due to the construction, the minimum weight applied is 0.6 kg.

The distribution of the weight needed to break the connection between sensor and read-out chip is given in Figure 12. No systematic trend across the wafer is appreciable and the weight needed is approximately two kilograms, which corresponds to 0.01 N per SLID connection. This is of the same order of magnitude to what is found for other interconnection technologies [37–41]. With the exception of extreme cases of misalignment, no significant correlation between the misalignment and the connection is found.

Figure 11: Photograph of the mechanical strength test setup.

In Figure 13 photographs of the pulled off read-out chips are shown. In almost all cases the whole SLID stack is appreciable, indicating that the weakest point of the interconnection is at the electroplated layers, i. e. layers that are similar in other technologies as for example bump bonding.

3. Electrical Properties of the Pixel Modules

In the following the performance of the successfully built pixel modules from the chip-to-wafer prototype production are discussed based on results obtained before and after irradiation. These results comprise: leakage currents, tuning properties, charge collection measurements, and in addition hit efficiencies and cluster sizes determined in beam test measurements.

3.1. IV Characteristics and Irradiation Programme

As basic functionality test, the IV characteristics of all seven modules are summarised in Figure 14(a). All IV characteristics were taken with the read-out chip powered, but not configured, to ensure a defined ground potential and exclude temperature changes [14]. At an over-depletion of about 10 V, i. e. at 30 V, the leakage currents are below 50 nA and thus far below the operational limit of 300 μA [1].

The breakdown voltage lies for one module at 100 V, for additional four modules at or above 140 V. Additional two structures were measured only up to a bias voltage of 55 V, and no

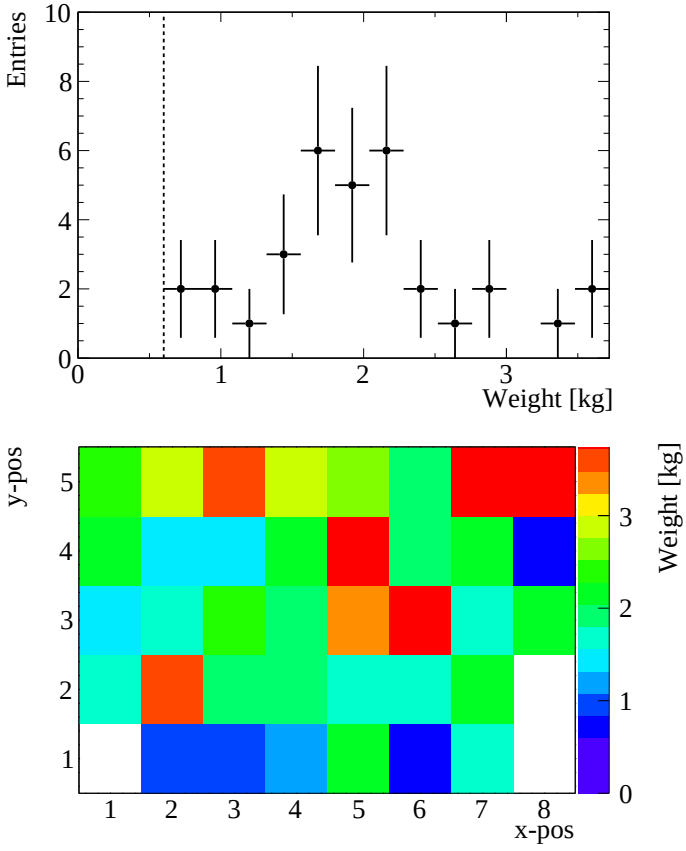
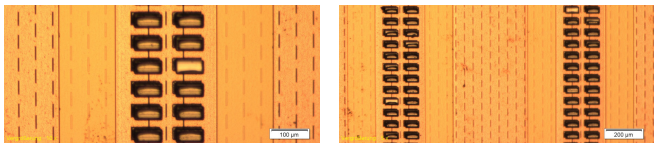


Figure 12: The weight at which the read-out chip was separated from the sensor. In the top figure the distribution is shown. The dotted line indicates the minimal weight applied. In the lower figure the position of the read-out chip on the wafer is indicated. The read-out chip at position (8,2) fell off before the test; the positions (1,1) and (8,1) are not populated by design, as shown in Figure 8.



(a) (b)

Figure 13: Well aligned SLID stacks in the centre of the structure for a read-out chip after its separation from the dummy sensor. The SLID connections can be seen. The horizontal scale is (a) 100 μm and (b) 200 μm.

breakdown was observed. For the structures measured up to the breakdown voltage, V_{bd}, this corresponds to a good over-depletion ratio $V_{bd}/V_{fd} \geq 3$.

Subsequently, the modules were irradiated at the Karlsruhe institut of Technology (KIT) with 25 MeV protons [42, 43] and at the Jožef Stefan Institute (JSI) with reactor neutrons [44]. The full irradiation programme is summarised in Table 3. The range (0.6–10)·10^{15} n_{eq}/cm^2 was covered mainly with reactor neutron irradiations.

In Figure 14(b) the leakage current as a function of the applied bias voltage is summarised for the irradiated assemblies. All measurements were taken at an ambient temperature of

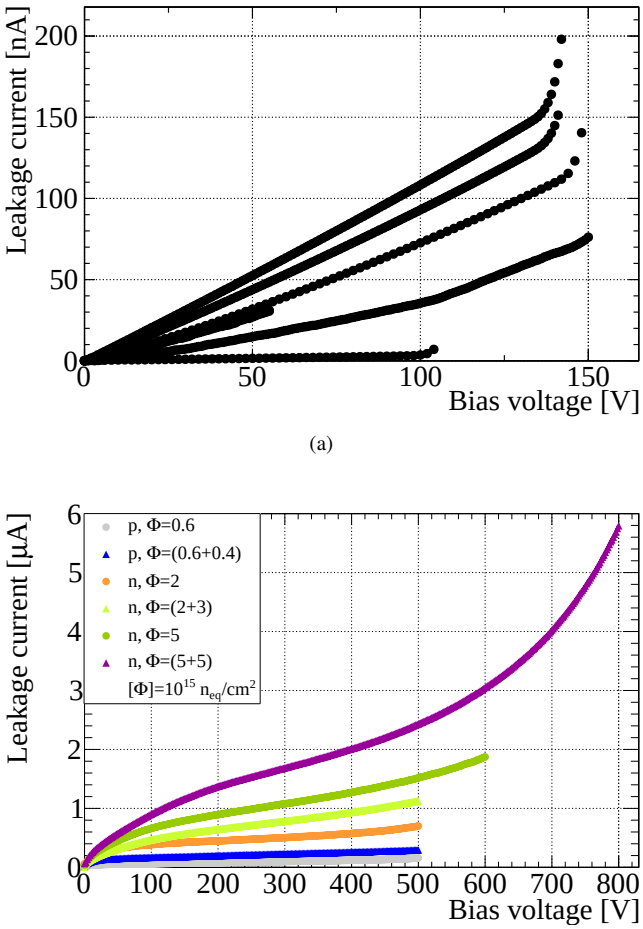


Figure 14: IV characteristics (a) before and (b) after irradiation for the pixel modules. The curves for the two structures measured up to 55 V before irradiation are indistinguishable. All measurements before (after) irradiation are taken at an environmental temperature of 20 °C (−50 °C). The statistical uncertainties are smaller than the symbols.

−50 °C to simulate as close as possible beam test environment temperatures where dry-ice cooling is employed. Again, the read-out chips were powered but not configured. The breakdown voltage of the irradiated sensors shifts to higher values and exceeds 500 V for all modules. Furthermore, the leakage currents are in agreement with expectations, showing increasing leakage currents with increasing fluences. Annealing effects are visible when comparing the module irradiated directly to a fluence of $5 \cdot 10^{15}$ n_{eq}/cm^2 with the module irradiated in two steps, since for irradiations at JSI an annealing time of about 1.5 d is unavoidable due to handling after each irradiation step. The latter module could not be investigated further, since the FE-I3 read-out chip failed after the second irradiation and remounting onto the test card. The leakage currents for all modules are found to be $\leq 6\,\mu$A and thus again far below the operational limit.

Assuming that all irradiated modules are fully depleted well below 450 V, it was verified that the damage factors are about $6 \cdot 10^{-17}$ A/cm, i. e. in agreement with theory predictions for the

Fluence [10^{15} n_{eq}/cm^2]	Irradiation site	Beam test
0.6	KIT	yes
0.6+0.4	KIT	
2	JSI	yes
2	JSI	
2+3	JSI	
5	JSI	yes
5+5	JSI	

Table 3: Overview of the received fluences for the irradiated modules and their respective irradiation sites. Assemblies tested in beam tests are indicated in the beam test column.

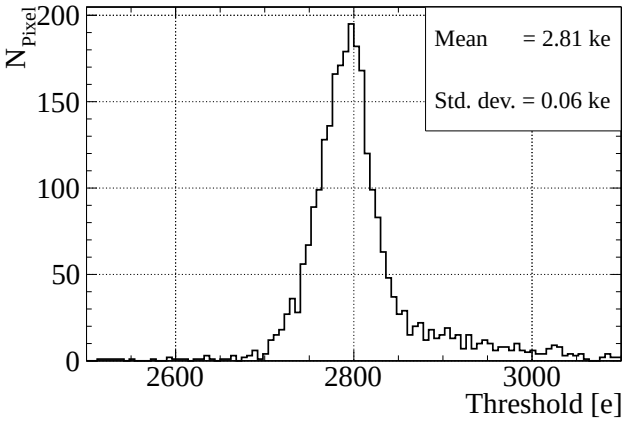
different target fluences and received periods of annealing [45].

3.2. Module Tuning

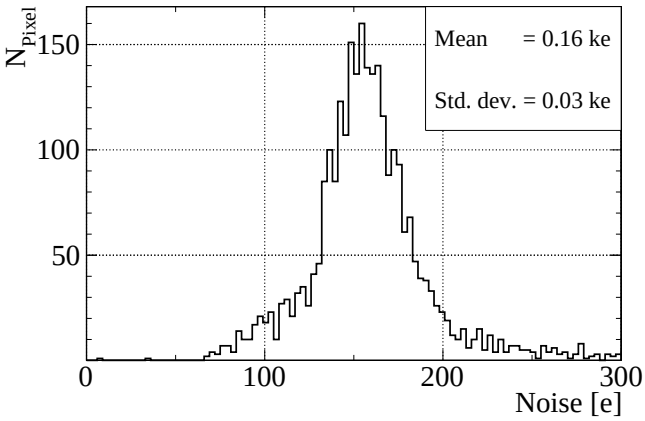
The module tuning and the charge collection measurements with radioactive sources were performed with the ATLAS USBPix read-out system [46]. The expected MPV for the charge induced by β-electrons of the ^{90}Sr decay chain is about 4.9 ke for the sensors with $d_{active} = 75\,\mu$m [47, 48]. Therefore, the tuning is focussed on lowering the threshold as far as possible for each individual module. For the present FE-I3 read-out chip used in this R&D programme thresholds down to 3.2 ke are generally achievable. For some single chip modules even lower thresholds down to (2.0–2.5) ke have been reached. This signal to threshold ratio is challenging for modules employing the present read-out chip. However, results for the new ATLAS read-out chip FE-I4 show that it can be operated at thresholds as low as 1.6 ke [49], which is more than sufficient for the sensor thicknesses around 75 μm presented here. An additional complication for the prototype modules is imposed by the not connected pixel cells for some of the modules. This implies that in the tuning two very different states of the read-out chip in adjacent regions have to be accommodated.

The threshold and noise distributions for a typical tuning are shown in Figure 15. The target threshold of 2.8 ke was reached for about 90% of the pixel cells with a standard deviation of 0.06 ke. The corresponding noise is 0.16 ke with a standard deviation of 0.03 ke over the module and thus not significantly different from the noise found for other n-in-n and n-in-p modules with thicknesses in the range (250-285) μm [1, 14].

In Figure 16 the results of the tuning with the lowest achieved threshold and the corresponding noise among all modules before and after irradiation is depicted. It was achieved for the module irradiated to a fluence of 10^{16} n_{eq}/cm^2. The mean threshold, shown in Figure 16(a), was tuned as low as 2.32 ke with a standard deviation of 0.54 ke across the module. The corresponding noise, shown in Figure 16(b), is 0.20 ke with a standard deviation of 0.05 ke across the module. The long tail of the distributions is mainly caused by pixel cells which could not be tuned to such low thresholds. The pixel-by-pixel correlation of threshold and noise, shown in Figure 16(c), demonstrates that the outliers in both distributions coincide. Since this is a known issue of the FE-I3 read-out chip, which is not planned to be used for future ATLAS upgrades, these outlier pixel cells are



(a)



(b)

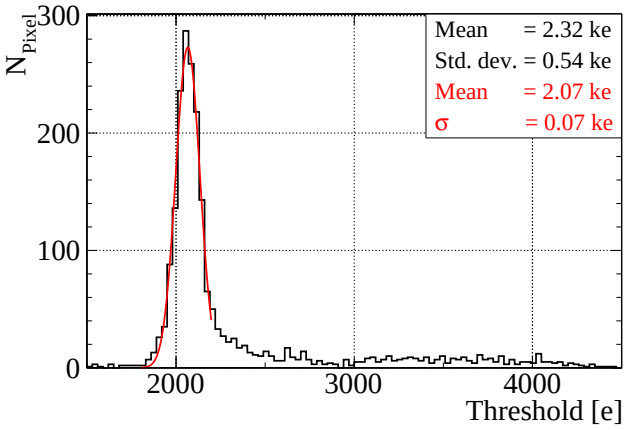
Figure 15: Typical (a) threshold and (b) noise distribution for a prototype pixel module.

disregarded in the following. For the shown tuning the threshold thus lies at (2.07 ± 0.07) ke and the corresponding noise is (0.18 ± 0.02) ke.

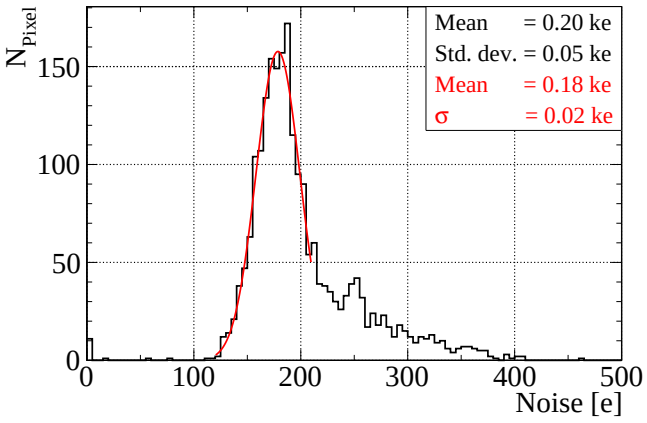
An overview of the threshold tuning and corresponding noise values of all modules before and after irradiation is given in Figure 17, where the lowest achieved thresholds and their corresponding noise values are given for each module. The uncertainties shown correspond to the standard deviation of threshold and noise, respectively. The average noise observed for all assemblies is (0.21 ± 0.01) ke. The slightly increased value with respect to currently used modules is due to the lower threshold target values and the influence of the not connected pixel cells. The effect of the not connected pixel cells is especially pronounced in the assemblies with the highest number of not connected cells, number 6 (open squares) and 7 (open circles). Nonetheless, an excellent threshold to noise ratio exceeding ten (red dotted line) in all but one case is achieved for assemblies before as well as after irradiation.

3.3. Charge Collection

Thin sensors show a higher CCE after irradiation, since the full depletion voltages are reduced, and higher electric fields are



(a)



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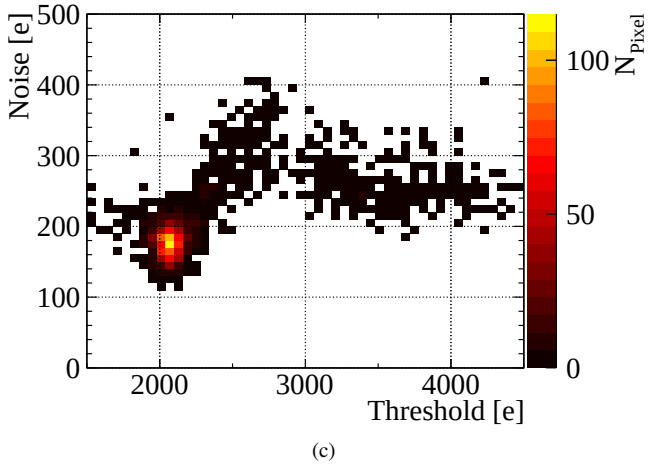


(c)

Figure 16: (a) Threshold and (b) noise distribution for the module irradiated to 10^{16} n_{eq}/cm^2. In (c) the pixel-by-pixel correlation of threshold and noise values is given.

achieved when applying the same bias voltage. To investigate the charge collection, measurements using either photons from an ^{241}Am source, or β-electrons from a ^{90}Sr source, were conducted. While for photons the internal trigger logic was used, for β-electrons an external trigger was employed. Within uncertainties no significant difference in charge collection was found between the modules.

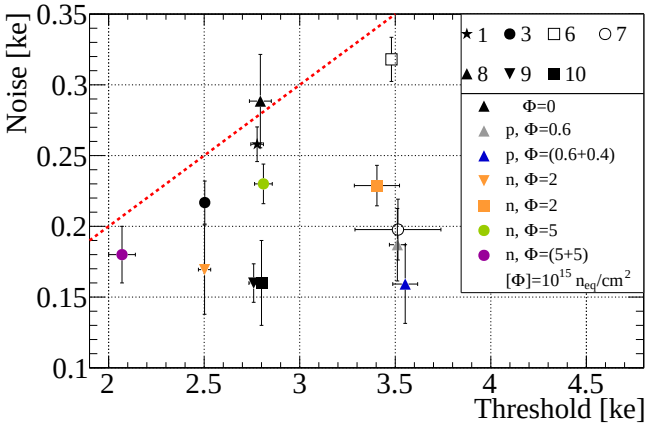


Figure 17: Best achieved mean thresholds and their respective noise values for the modules before and after irradiation. The symbol style denotes the module and the colour the received fluence. Irradiations with protons (neutrons) are indicated by p (n). For better visibility, the data point for module 9 before irradiation has been slightly displaced horizontally by -30 V. The uncertainties indicate the standard deviations of the respective distributions. Before irradiation the environment temperature is kept at 20 °C, afterwards at −50 °C. The red dotted line indicates a threshold to noise ratio of ten.

3.3.1. Radioactive Source Measurements

In Figure 18 the ^{241}Am photon spectra obtained with a module biased at different bias voltages between 5 V and 55 V are depicted. Each histogram is normalised to its bin with the highest content. For a high resolution reference spectrum taken with a high purity Germanium detector please refer to [50, 51]. At 55 V the prominent 59 keV γ-line is measured at $(14.4 \pm 0.5(\text{fit}) \pm 1.1(\text{syst.}))$ ke (Gaussian fit not shown), which is in good agreement with the expected peak position of 16.4 ke, when taking into account the calibration bias of the FE-I3 read-out chip. The first uncertainty denotes the one from the fit, and the second the systematic uncertainty stemming from the charge calibration of the read-out chip. The second prominent line in the spectrum at 26 keV is expected at 7.2 ke. However, due to the charge resolution it merges with the lines below, such that only the upper edge is appreciable, which lies between 6 ke and 7.5 ke.

At lower bias voltages a fraction of the sensor volume does not contribute to the charge collection and thus the full charge is only collected for events where the photo-electric process occurred in an already depleted region. For those events where it instead occurs in the not yet depleted part, only the fraction of the charges diffusing into the depleted volume can be measured. This leads to a broadening of the peaks and to a less defined spectrum. Due to the small thickness of the sensor, only the measurements below 15 V are significantly affected.

A charge distribution of a ^{90}Sr measurement of a module operated at a bias voltage of 55 V is shown in Figure 19(a). The threshold in this measurement was tuned to 3.0 ke and is indicated by the red dotted line. Entries below threshold occur because the threshold corresponds to the 50% efficiency

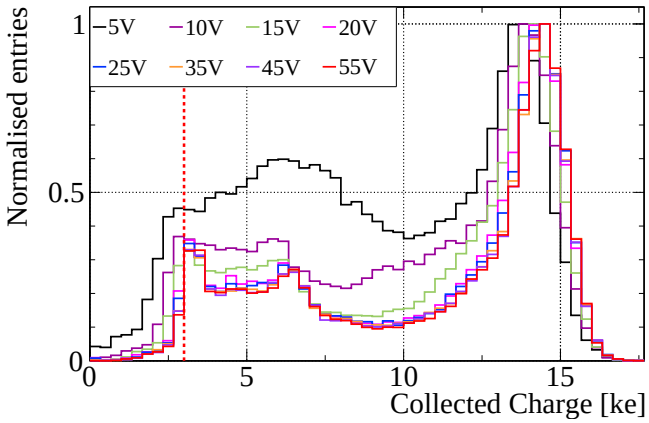
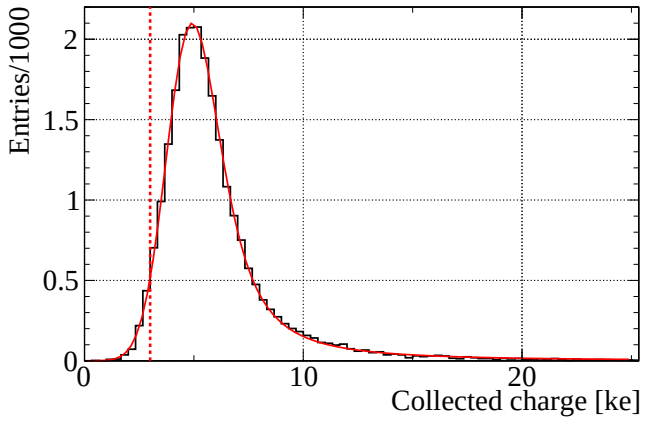


Figure 18: Evolution of an ^{241}Am source energy spectrum with the applied bias voltage. The threshold of 3.0 ke is indicated by the red dotted line.

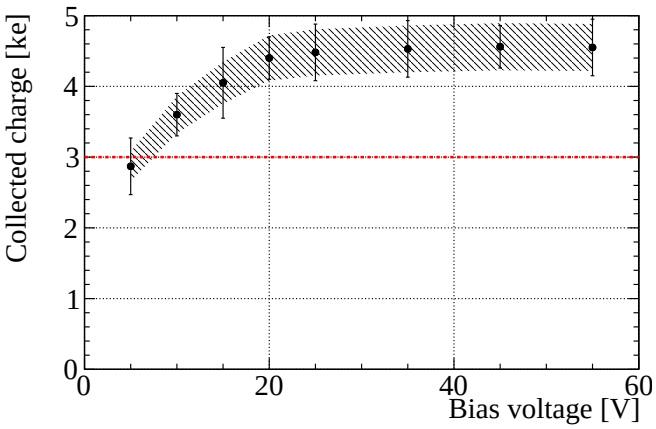
point. A convolution of a Landau distribution with a Gaussian describes the measurement well. The resulting most probable value (MPV) of the collected charge as a function of the bias voltage is summarised in Figure 19(b). The uncertainty, shown as a band, is fully correlated from point to point and caused by the calibration uncertainty. Since the MPV of the collected charge is close to the threshold, the uncertainties arising from the fit are increased due to the deformation of the Landau distribution. They are indicated by the uncertainty bars. Full charge collection is reached at a bias voltage of (21 ± 0.7) V as determined by the intersection of two linear functions describing the different parts of the charge collection measurement. This agrees well with the infra-red laser measurements on strips from the same production. For the module shown the charge saturates at $(4.6 \pm 0.4(\text{fit}) \pm 0.3(\text{syst.}))$ ke and thus is in good agreement with the expectations for a sensor with $d_{\text{active}} = 75\,\mu$m.

Aiming for usage at the expected HL-LHC environment, a high CCE at high irradiation levels is of utmost importance. The measured values of this parameter are summarised for all irradiated modules as a function of the applied bias voltage and for different received fluences (colour) in Figure 20(a). Since the uncertainties stemming from the charge calibration before and after irradiation are highly correlated they almost completely cancel, when investigating the ratio. Still, as a conservative estimate a 5% uncertainty is assigned to the ratio. As expected from the strip measurements [15], within the assessable voltage range, a saturation is found up to the highest fluences. The onset of the saturation increases with fluence, but lies for all fluences at comparably low voltages, i. e. below 500 V. These low bias voltages, in combination with the fact that all modules saturate within uncertainties to a CCE of 100% up to a received fluence of $5 \cdot 10^{15}$ n_{eq}/cm^2 and to 90% at a received fluence of 10^{16} n_{eq}/cm^2, allows to operate them in a restricted bias voltage range over the entire life-time of an experiment. This leads to looser requirements on the read-out electronics.

For comparison in Figure 20(b) the results obtained from infra-red laser measurements on strip sensors from the same



(a)



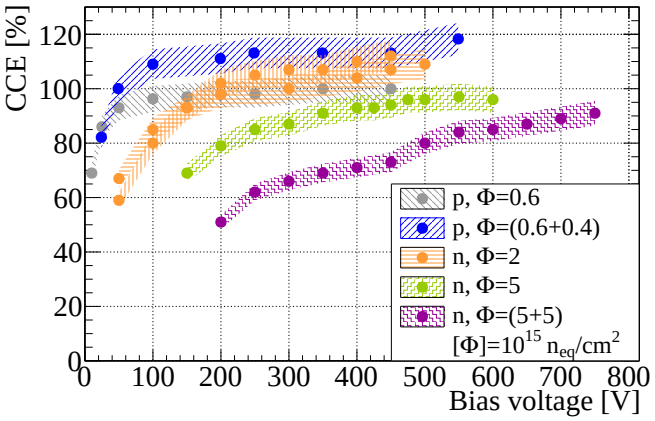
(b)

Figure 19: (a) Distribution of collected charge induced by a ^{90}Sr source for a module biased at 55 V. Shown in red is the fit function, a Landau distribution convoluted with a Gaussian. The resulting MPV of the collected charges as a function of the bias voltage is shown in (b). The uncertainty bars account for the fitting uncertainty and the band for the fully correlated systematic uncertainty. The dotted red line indicates the threshold.

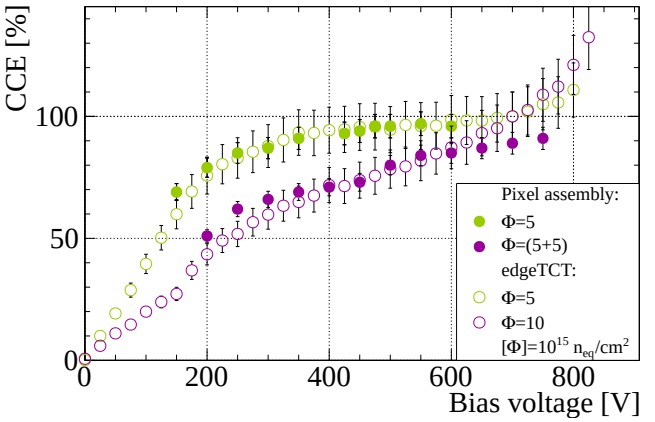
production are depicted together with the results obtained with the pixel modules for the two highest received fluences [15]. For this figure the infra-red laser measurements were renormalised globally to achieve comparable scales. For the measurement at $5 \cdot 10^{15}$ n_{eq}/cm^2 an excellent agreement is found over the entire range. At the higher fluence slight deviations at low and high applied bias voltages are observed, which are most likely caused by the different annealing history of the structures, given the two step irradiation procedure for the pixel module. However, considering the use of a single scaling factor over the entire range, a good agreement is achieved.

3.3.2. Charge Collection for Different Sensor Thicknesses

The absolute collected charge as a function of the applied bias voltage after irradiation is given in Figure 21. The results for the SLID prototype modules and for modules employing sensors with different thicknesses [13, 14, 18] are grouped by comparable fluences. The sensors with thicknesses of $d_{\text{active}} =$



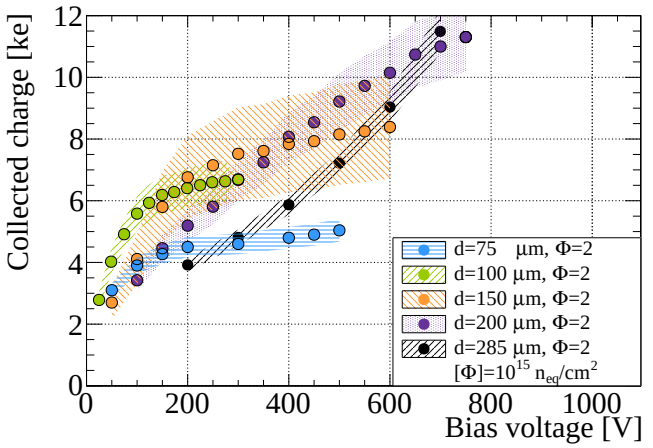
(a)



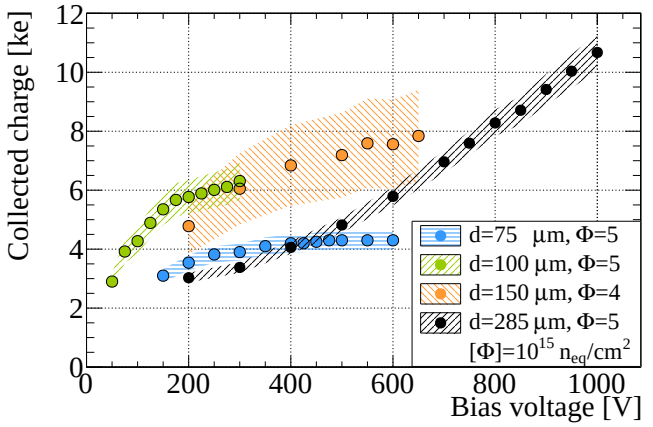
(b)

Figure 20: (a) CCE with respect to the charge collected by the respective module before irradiation as a function of the applied bias voltage for irradiated modules. Proton (neutron) irradiated samples are denoted with p (n) in the legend. The uncertainty band accounts for the overall time-over-threshold to charge calibration. (b) Comparison of the MPV of the collected charges obtained with pixel modules (full symbols) to infra-red laser measurements on strip sensors from the same production [15] (open symbols). For a better visibility the fully correlated uncertainty bands are drawn as simple bars.

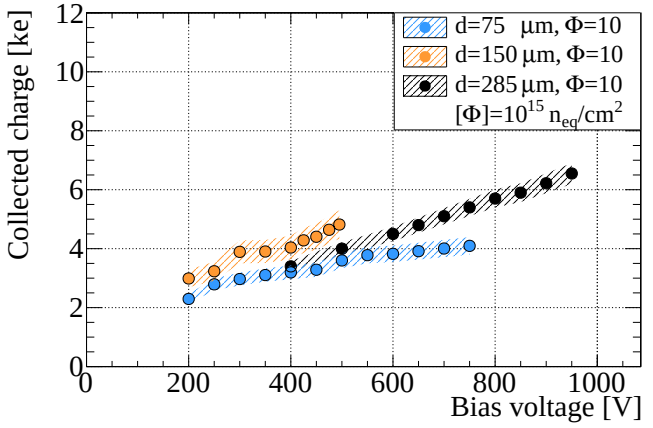
75 μm and d_{active} = 150 μm were produced with the MPG-HLL process, those with thicknesses of 100 μm and 200 μm were produced by VTT [52], and finally, the sensors with a thickness of 285 μm were produced by CiS [53]. Some modules (the d_{active} = 75 μm and the 285 μm thick modules) employ the FE-I3 chip. The others are built with the new FE-I4 chip version A. For some modules with FE-I4 chips a refined charge calibration is not available. For those, i. e. the d_{active} = 150 μm sensors measured at fluences of $2 \cdot 10^{15}$ n_{eq}/cm^2 and $5 \cdot 10^{15}$ n_{eq}/cm^2, a conservative uncertainty of 20% is assigned. For the remaining modules with FE-I4 chips a calibration based on a ^{109}Cd source has been performed, resulting in a reduced uncertainty of 10%. In Figure 21(a) the comparison at a fluence of $2 \cdot 10^{15}$ n_{eq}/cm^2 is shown, in Figure 21(b) the one at $5 \cdot 10^{15}$ n_{eq}/cm^2, where for the 150 μm thick modules a similar fluence of $4 \cdot 10^{15}$ n_{eq}/cm^2 is used. Finally, the results at a fluence of 10^{16} n_{eq}/cm^2 are shown in Figure 21(c). The data in all figures exhibit similar



(a)



(b)



(c)

Figure 21: Comparison of charges collected with irradiated pixel modules of different thicknesses and received fluences. In (a) the result for a received fluence of $2 \cdot 10^{15}$ n_{eq}/cm^2 is shown. In (b) results for fluences of $4 \cdot 10^{15}$ n_{eq}/cm^2 and $5 \cdot 10^{15}$ n_{eq}/cm^2 are shown, while (c) summarises the results at 10^{16} n_{eq}/cm^2. For better comparability all plots share the same scale. The bands denote the systematic uncertainty that originates from the charge calibration of the respective read-out chip. Within each graph, this uncertainty is fully correlated from point to point.

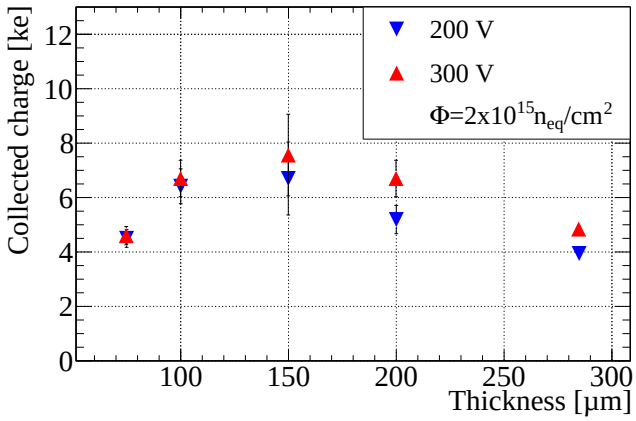


Figure 22: Overview of collected charges at different voltages. The collected charges at 200 and 300 V for the modules shown in Figure 21(a) are compared. The uncertainties of the points at a thickness of 285 μm are smaller than the symbol size.

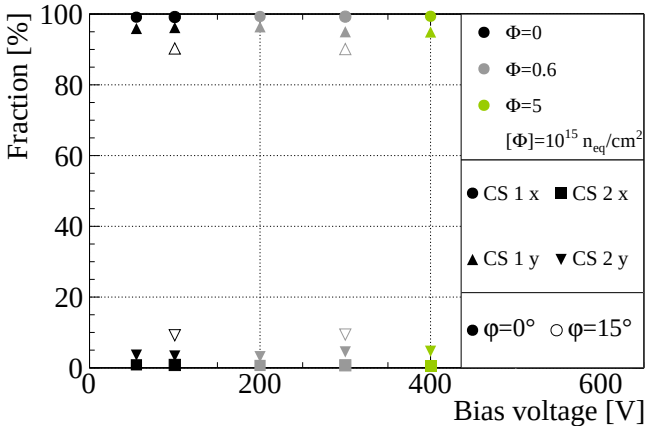


Figure 23: Summary on the cluster size fractions as a function of the bias voltage before and after irradiation. The uncertainties are calculated according to [55] and are smaller than the symbol sizes. The colours represent the received fluences and the marker type the cluster size as well as its spatial coordinate. Filled (open) markers stand for measurement at perpendicular (φ = 15°) incidence.

characteristics. While for the 200 μm and 285 μm thick modules no saturation is found up to the highest probed bias voltages, the thinner modules saturate at bias voltages below 500 V. Comparing the collected charges at 200 V and 300 V for the different thicknesses irradiated to a fluence of $2 \cdot 10^{15}$ n_{eq}/cm^2, as given in Figure 22, a trend for the largest CCE to occur at a thickness of about 150 μm is present. Measurements using the second revision (version B) of the FE-I4 chip, or using FE-I3 read-out chips, will diminish the uncertainties in the future. Still, already now, these measurements imply that the optimal thickness for future tracking detectors lie around 150 μm and that 75 μm thick sensors, despite their high CCE, can only be used with improved read-out chips like the FE-I4.

3.4. Cluster Size

The cluster size and hit efficiency were determined with test beam data obtained with 120 GeV pions at the CERN SPS. The position within a given pixel assembly under test where the particle traverses the assembly is determined from external information provided by the EUDET beam telescope [54]. Analysing the signals from the pixels around this position the cluster size and the hit efficiency can be determined.

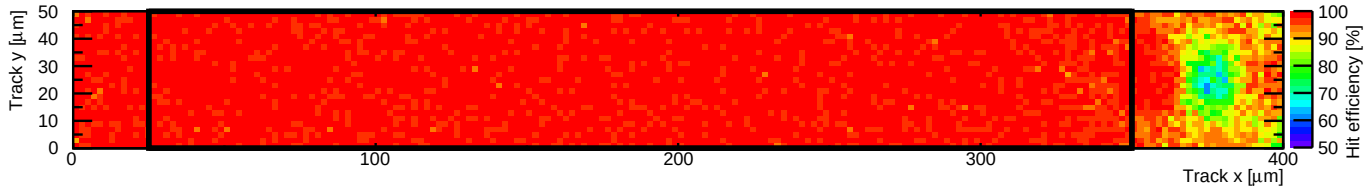
For thinner sensors the spatial resolution is expected to differ from the one observed for thick sensors given the different cluster size abundances. However, when comparing the resolution on events with a specific cluster size between different thicknesses no difference is expected. In any case, lower cluster sizes lead to a reduced occupancy.

The low absolute collected charge to threshold ratio is reflected in the smaller abundances of higher multiplicity clusters. In Figure 23 a summary of the cluster size as a function of the bias voltage for different received fluences (colour), spatial coordinates (symbol style), and particle incidence angles φ (closed/open symbols) is given. The uncertainties are calculated according to [55] and are smaller than the symbol sizes. In the direction of the short pixel pitch y only about 5% of two-hit clusters are observed for perpendicular incidence. If the modules are tilted by φ = 15°, as it is foreseen for the IBL, about 10% of the clusters in y are composed of two hits. As expected from the CCE measurements, no difference is found before and after irradiations, provided that the applied bias voltage is around or above the value corresponding to the charge saturation.

3.5. Hit Efficiency

Besides the resolution, the tracking efficiency of the pixel detector is the key figure of merit. For a high tracking efficiency, a high hit efficiency of the pixel assemblies is mandatory. The latter is mainly driven by the ratio between collected charge and threshold. Consequently, for thinner sensors the lowest possible threshold is desirable as discussed before. This criterion is especially challenging since the difference between the mean threshold and the MPV of the collected charge is so small that a part of the distribution lies below threshold, as shown for example in Figure 19(a). Since the threshold corresponds to an efficiency of 50% for the electronic circuit of the pixel cell this considerably diminishes the overall hit efficiency. In Figure 24(a) the mean hit efficiency as a function of the impact point predicted by the beam telescope is depicted for a bias voltage of 100 V. For this measurement, the thresholds was tuned to 2800 e.

The impact of the comparably high threshold is most pronounced in the area of the punch-through bias structure, and in the corner regions, where it leads to a loss of hit efficiency due to the sharing among several pixels. Anyhow, both effects are most pronounced for perpendicular impinging particles, occurring only for the very central part of a high energy physics experiment. Therefore, the quoted hit efficiency has to be understood as a lower bound. The overall hit efficiency is found to be (98.1 ± 0.3)%. If just the central region, indicated by the box in Figure 24(a), is considered, the hit efficiency rises to (98.5 ± 0.3)%. Although this hit efficiency is still high when



(a)

(b)

Figure 24: (a) Map of the mean hit efficiency as a function of the impact point predicted by the beam telescope at a bias voltage of 100 V. For reference in (b) the design of a single pixel cell is given. The implantation extends over the entire structure shown, and has a ring shaped opening at the punch through bias dot displayed on the right side. The metal layer, covering most of the implant, is shown as a large rectangle with rounded corners on the left side. The T-shaped structure at the far right end comprises the metal lines, connecting the bias dot to the bias ring. The opening in the nitride and oxide layers is displayed as the rectangle in the centre of the pixel. The small circle at the left end of the pixel is the opening in the passivation, where the pixel will be connected with bump bonding.

taking into account the challenging charge to threshold ratio, it clearly shows that the present ATLAS read-out chip in combination with sensors of 75 μm is not optimal for tracking purposes. Notwithstanding the high CCE, the situation stays challenging after irradiation and thus a discussion of the hit efficiencies is not sensible and omitted here.

The lower minimal thresholds offered by the FE-I4 read-out chip improves the charge to threshold ratio, and might allow to use sensors as thin as 75 μm. Nonetheless, already sensors as thin as 150 μm exhibit a very good CCE after irradiation and are operable at comparably low bias voltages.

4. Conclusions

Mechanical and electrical results obtained with SLID interconnected structures from an R&D campaign towards a new pixel module were discussed. The investigated concept is based on several new technologies, namely n-in-p sensors, thin sensors, slim edges with or without active edges, and 3D-integration incorporating SLID interconnections as well as ICVs.

The 3D-integration is foreseen in the module concept to achieve compact module. The SLID interconnection technique by EMFT was qualified for use on pixel sensors by verifying the effectiveness of the TiW diffusion barrier and determining the needed vertical and horizontal alignment precision. Especially, it was shown that deliberate height mismatches of up to 1 μm are not detrimental for the connection efficiency. First prototype modules employing the ATLAS FE-I3 read-out chip and 75 μm thick sensors were built. It was shown that SLID interconnections have a stability and durability similar to other interconnection technologies used. Furthermore, all pixel cells were interconnected for assemblies where the underlying BCB passivation layer was fully opened in correspondence to the SLID interconnections. An SF_6 plasma descum process will guarantee that in future interconnections the BCB passivation layer is opened sufficiently everywhere. Also at the moment new tools and processes are installed and implemented at EMFT to further improve on the alignment precision, which will allow for even smaller pitches.

For the prototype modules the CCE and the absolute collected charge were investigated systematically as functions of the received fluence and the applied bias voltage. The results were compared to results of pixel sensors of different thicknesses from a number of producers and to results obtained with strip sensors from the same production. It was shown that after an irradiation to a received fluence of 10^{16} n_{eq}/cm^2, assemblies with a thickness of $d = 285\,\mu$m collect about one third of the charge that had been collected before irradiation, assemblies with $d_{active} = 150\,\mu$m collect around 60% to 70%, and assemblies with $d_{active} = 75\,\mu$m even saturate at a CCE of 90% to 100%. For an application within an experiment, in addition to the CCE also the absolute charge and its relation to the threshold of the read-out chip has to be taken into account. Although, with the low thresholds possible with the new FE-I4 read-out chip using a sensor thickness down to about 75 μm seems feasible, the absolute charge measurements indicate that the optimum lies at a thickness of about 150 μm. Anyhow, other factors like the lowered occupancy of thinner detectors might render thinner sensors still to be the better choice. Furthermore, the requirements on high voltage stability are relaxed for thinner sensors since thinner sensors exhibit a high CCE already at moderate bias voltages. In conclusion, the good properties of the sensors and modules presented here make them well suited for use in ATLAS when operating at the HL-LHC.

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