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Deliverable Report

Publication of Specification Documents for the Common DAQ

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DELIVERABLE REPORT

PUBLICATION OF SPECIFICATION DOCUMENTS FOR THE COMMON DAQ

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Abstract:

The requirement and specifications for a Data Acquisition system (DAQ) common to devices of R&D for ILC are here described. After a review of existing systems, the key elements to perform such a task are detailed: they boil down to a common hardware device for fast signal dispatching and synchronisation (TLU2), and some relatively loose requirements on software communication and data format.

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Delivery Slip

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Executive summary

The FP6 EUDET program has been quite successful in fostering the R&D for the ILD R&D. Two main acquisition system were developed in this framework: 1) the CALICE DAQ (version2) dedicated to the digital readout of the technological prototypes of the CALICE collaboration; 2) the EUDAQ system designed to read the EUDET beam telescope sensors and allowing for easy to use plug-in for the devices in test. The other system will use this plug-in mechanism.

The existing systems are quite heterogeneous, but they all share common functionalities to DAQ; the minimal level of modification foreseen here involves common synchronization electronics and analysis framework.

A quick overview of the existing Acquisition systems (EUDAT, CALICE, RD51 SRS) is provided in correspondence with the existing detector systems developed in AIDA.

1. INTRODUCTION

Within the AIDA collaboration there are two reasons for considering a common approach to Data Acquisition (DAQ): firstly, the ability to synchronize multiple detectors at common beam-tests. Secondly, the opportunity to share hardware/firmware/software design effort between groups.

Many devices are being tested by the WP9 groups, all requiring a Data Acquisition. The following ones are susceptible of being integrated:

- WP9.2 TPC + sALTRO chip (considered subWP : 9.2.3 common readout)
- WP9.2 TPC + AFTER chip
- WP9.3.1 Mimosa Telescope
- WP9.3.1 Timepix Telescope
- WP9.3.1 FEI4 Telescope (for LHC)
- WP9.3.2 OffBeam Telescope
- WP9.4 Silicon Tracking (SILC)
- WP9.5.1 AHCAL
- WP9.5.2 DHCAL
- WP9.5.3 ECAL
- WP9.5.4 FCAL

This document describes the approach to common DAQ likely to be taken by groups conducting beam-tests. The DAQ and synchronization for neutrino detector is not concerned.

2. PHILOSOPHY

A complete DAQ is composed of several components. With the finest granularity, the following elements can be isolated (in parenthesis, some examples of use in the ILC R&D program related to AIDA):

c1 Synchronisation electronics (ex: TLU's, CCC's, TPC's Local Trigger Box's)

c2 Readout chips (ROC), elsewhere also dubbed Very Front-End (VFE)

c3 Transport electronics (DIF's, LDA's, GDCCs', ODR's for calorimetry; CMC's and SRU's for TPC; NIDAQ for the telescope)

c4 Data acquisition Software (Data Producer from XDAQ, EUDAQ, DATE, …)

c5 Slow control Software (DOOCS, XDAQ, Scripts, …)

c6 Reconstruction, aggregation and storage software (Marlin [10])

c7 Connectivity, Configuration databases (MySQL, Oracle, LCCD in EUDAQ)

c8 Conditions database (MySQL, LCCD)

We choose to structure our integration effort in different layer clustering the previous components:

- Synchronization level (c1)
- Acquisition level (c2, c3, c4)
- Control/command level (c5, c7)
- Analysis level (c6, c8)

Such an approach has been used successfully by the EUDET pixel beam-telescope.

The integration at the synchronisation level is based on a common time-stamp, distributed to all the different components of the detectors so that the data can be synchronised at the bunch
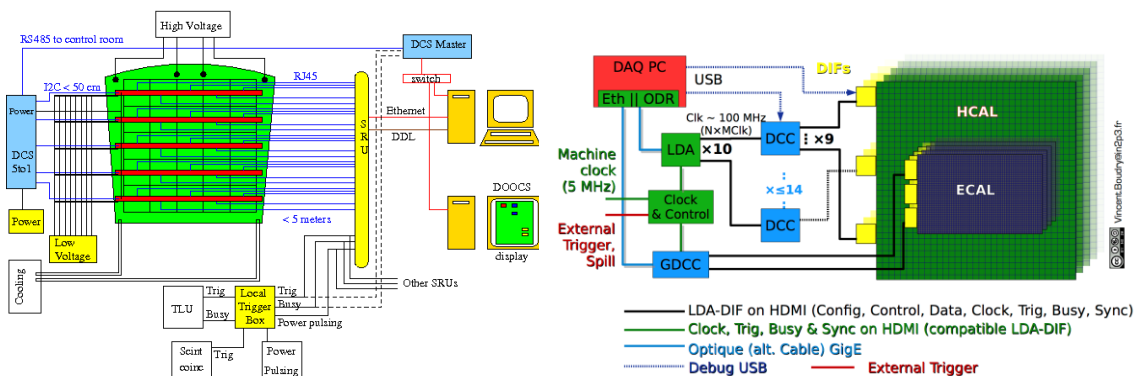

Figure 1: DAQ scheme for the TPC (left), for CALICE (right)

crossing frequency or better. Some basic controls (fast command and busy signals) need also to be dispatched/collected over all the components to maintain them synchronized.

At the acquisition level, data from different readout chips are sent through the transport electronics. The acquisition software receives them and records them in a common format in one of several synchronized files.

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At the control/command level, a global command system is able to manage the different components by sending them slow control and orders, and reading their status. This part should integrate a configuration database and a connectivity database.

At the analysis level, data from different detectors are reconstructed and aggregated into the same framework so that a common analysis can be performed. Online, immediate checks are done on selected subsample of the data.

A system of gathering and publication of the run conditions should be provided too.

A common approach is mandatory for the first and the fourth point. For the two others, a common gathering/scattering of commands and data is enough.

3.   DAQ SYSTEMS

All the considered detectors are actually using EUDAQ, CALICE DAQ2 or RD51 SRS are planning to migrate to one of them in near future.

3.1.   EUDET TELESCOPE DAQ

This DAQ has been developed for the EUDET JRA1 Beam Telescope [1]. It is composed of a trigger and logic unit (TLU2) and an acquisition software, EUDAQ [2]. They have been designed to easily integrate external systems by adapting "data producers".

EUDAQ is a simple and easy to use data acquisition framework. The overall structure has some resemblance to the XDAQ framework (hence the 1name EUDAQ) but it is greatly simplified, and relies on as few external libraries as possible. EUDAQ is designed to be portable. It allows the generation of LCIO files.

It has a large user panel and the corresponding infrastructure (documentations [3]) with regular meetings in the framework of WP9.3.

The TLU2 is a synchronisation hardware device. It has been designed to give a simple but flexible interface to trigger/timing signals. It distributes clock and fast commands to transport and readout electronics. It is described in [4].

A preliminary readout format has been defined as:

3.2. CALICE DAQ2

CALICE DAQ2 [5] is a global DAQ system from the CALICE Collaboration, partly inherited from the EUDET DAQ for calorimeters. It integrates a chain of electronic cards (DIF's → DCC's → LDA's or GDCC's, see Figure 1) to collect, centralize and dispatch the data from the calorimeters. It includes also an acquisition and control & command low level software (CALICOES) [6].

The DIF is the low-level interface card: it adjusts the electrical level from the acquisition chips and aggregate data from different chips to produce chunk of data. These packets are sent on a Fast-Ethernet-like links to the aggregating cards; the DCC is a optional first level aggregating card. It allows regrouping up to nine DIFs on the same LDA port. The LDA is the second (and last) level aggregating card. It takes data from DIFs or DCCs and aggregates them to produce Ethernet packets. The LDA's also merge the fast signal from/to the CCC on a single link to the DIF's. The GDCC ("GigaDCC") is a consolidated version of the DCC equipped with Giga-Ethernet aiming at replacing the aging LDA's.

The CCC card is the trigger/timestamp provider. This card distributes its signals through the LDA's. An extended version CCC2 has been designed to cover additional needs (Trigger validation scheme, interface to EUDAQ) and as backup solution for the standard CCC.

The acquisition software receives the Ethernet packets from the LDA's (or GDCC's), dispatch data in streams and make it available through multiples channels (files, shared memories, sockets...). It allows reconstructing LCIO events from the raw data format.

CALICOES is a generalised slow control software. It allows dispatching specific configurations to all components from a centralized and human readable configuration file format.

3.3. RD51 SCALABLE READOUT SYSTEM (SRS)

The Scalable Readout System [7] is a global DAQ developed by the RD51 group at CERN. It is composed of a Front-End Card (FEC) converting data readout to Ethernet. A second level card named SRU aggregates the links from FEC's and sends data to an acquisition PC through a high-speed Ethernet link. It also sends clock and trigger to the FECs.

The Alice DATE software [8] is used to acquire data (local data concentrator). It can also aggregate the data at a higher level by combining data from different parts of the detector (global data collector).

4. DETECTOR SYSTEMS

Different groups will, in general, have different DAQ systems and will need adapted approaches to perform the integration. The Table 1 summarizes the current interfaces of each system to the common DAQ.

Table 1: Interfaces to the common DAQ for individual systems

Level System	Synchro-nization	Acquisition HW	Config. & Control	Analysis
TPC sALTRO	TLU2	SRS	DATE	Root

Mimosa Telescope	TLU2	EUDAQ	EUDAQ	LCIO+Root+ EUTelescope SW
Timepix Telescope	TLU2	TimePixDaq	EUDAQ	LCIO+Root+ EUTelescope SW
Silicon Tracking	TLU2	EUDAQ	EUDAQ	LCIO+Root+ EUTelescope SW
AHCAL	CCC	USB	Labview	LCIO+Root+Marlin
DHCAL	CCC	DAQ2+USB	XDAQ	LCIO+Root+Marlin
ECAL	CCC	DAQ2	Calicoes	LCIO+Root+Marlin
FCAL	CCC	USB	Labview	LCIO+Root or text

5. SPECIFICATIONS

5.1. HARDWARE SYNCHRONISATION

5.1.1. Communication TLU–CCC

Based on the current schematics of the Mainz passive VME fan-out[1] a HDMI cable interface between TLU and CCC is possible. The proposed pin-out is displayed in Table 2

Table 2: Suggested pin-out for HDMI cable carrying fast signals to CCC.
Based on: https://twiki.cern.ch/twiki/bin/view/CALICE/DifEcal
http://www.staff.uni-mainz.de/degele/Calice/CCC_VME/CCC_VME_V3.SCH.pdf

Pin Number	Signal Name	Signal Description	Pin Number	Signal Name	Signal Description
1	T2C_CLK+	TLU to CCC LVDS Clock +	2	RG1	T2C_CLK shielding
3	T2C_CLK-	TLU to CCC LVDS Clock +	4	T2C_CONTROL+	TLU to CCC LVDS Control+
5	RG2	T2C_CONTROL shielding	6	T2C_CONTROL-	TLU to CCC LVDS Control-
7	C2T_BUSY+	CCC to TLU Busy +	8	RG3	C2T_BUSY shielding
9	C2T_BUSY-	CCC to TLU Busy +	10	C2T_SPARE+	CCC to TLU Spare +
11	RG4	C2T_SPARE shielding	12	C2T_SPARE-	CCC to TLU Spare -
13	N/C	Not connected	14	3V3	3V3 power for HDMI add-ons

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[1] http://www.staff.uni-mainz.de/degele/Calice/CCC_VME/CCC_VME_V3.SCH.pdf

15	T2C_TRIGGER+	TLU to CCC Trigger + (not shielded)	16	T2C_TRIGGER-	TLU to CCC Trigger - (not shielded)
17	RG5	HDMI shield	18	GND	Ground (for power)
19	GND	Ground (for power)			

*T2C_* = signals from TLU to CCC*
C2T_* = signals from CCC to TLU
Signal standard = LVDS

Notes: 1) Clock frequency and jitter specification to be decided
2) T2C_CONTROL likely to be spill information?

The CALICE CCC2 might possibly have all the functionality of pixel-beam-telescope TLU with a lot more interfaces; the FPGA-based Calice CCC2 might then become the hardware platform for a "full" AIDA TLU with the mini-TLU being used for small scale tests and for preparations for beam-test in home institutes (cheaper). This has to be confirmed/investigated.

The same physical connector standard (HDMI) is used for the fast control signals and the trigger information data path; this way the CCC could be programmed to operate as a "master" if the CALICE DAQ was operating stand-alone or capture/fanout trigger information from a TLU if operating with other detectors. Alternatively the CCC could have firmware added so it could be the master TLU.
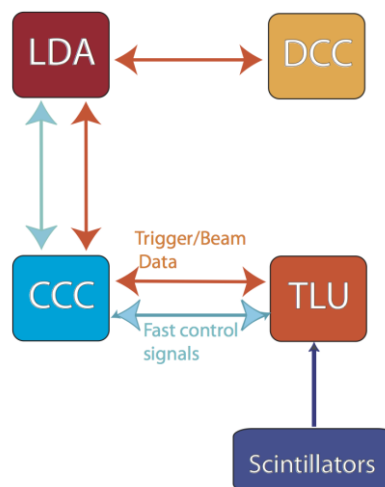
5.1.2. TLU–SALTRO connection

A simple passive fan-out and connector adaptor could insure the connection between the TLU and the SRS readout system.

5.1.3. Synchronisation to LHC type detectors

The timing diagram of a "fast synchronous" interface to LHC type detectors needs to be specified. There will be Clock (TLU to DUT), Trigger (TLU to DUT), Spill-On (TLU to DUT) and BUSY (DUT to TLU) signals. The trigger will go high for a single cycle of the clock. The TLU will respond to BUSY in no more than 5 clock cycles.

The existing EUDET-style (asynchronous TRIGGER/BUSY handshake) will remain unchanged.

5.2. INTEGRATION AT ACQUISITION LEVEL

Both CALICE DAQ2 and EUDAQ systems propose LCIO [9] outputs with sequential records. Thus it seems obvious to make a convergence from the two acquisition systems. A conversion step will be needed from the DATE format.

The problems comes from the necessary merging of the different data to provide a global data streams where all individual events should be aggregated with all the others with same bunch crossing $BCID\pm n$ (global event building; n is equal to 1 for prompt systems but might be greater for some specific timing studies).

This can be achieved by storing records, each corresponding to a single acquisition (be it an external Trigger or a Spill).

To the first order the data stream to files will be parallel; multiple timestamps (Trigger number dispatched from the TLU, and from internal long counter; BCID of the trigger from a global start; timestamp of triggers; spill start/end; …) should allow for disambiguation and error recovery.

The merging of the data can easily be done offline within the Marlin framework (or from plain text files if needed by some analysis framework).

5.3. CONTROL/COMMAND INTEGRATION

At that time, the different projects have all a slow control system, sometimes only a Labview interface.

A central system should store the different part configurations and distribute them to the different parts of the global detector. Alternatively for large existing systems, it should store the configuration number used by the attached systems and distribute the order to load them. It is not in the primary scope of the common DAQ to implement running parameters (loops, scans …).

This should be implemented with a central database where all the different teams could store the parameters they need, classified by run. Such a system has been implemented for the CALICE Physical prototypes and independently for the SDHCAL project: a database contains all the necessary parameters of every run of the beam-tests.

For the control/command, all the different parts of the system should be controlled by a central SCADA. It should ask the different specific software for state variables or global orders. For enabling such a global control, all the specific software's have to implement a high level state machine with action labelled transitions. The whole point is to have a consensus on such a state machine.

As an example the following simple system is implemented in the CALICOES library:
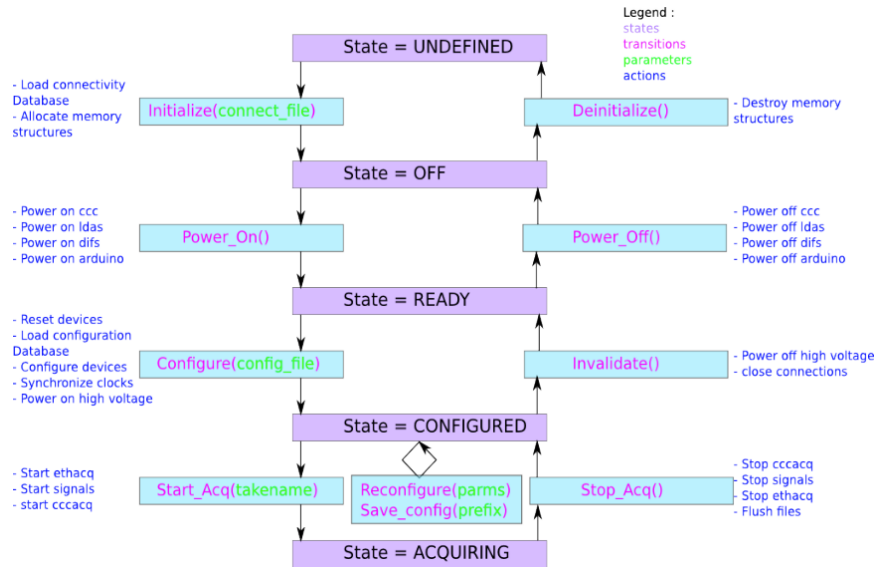

Figure 2: Simple configuration machine state.

5.4. INTEGRATION AT ANALYSIS LEVEL

The event builder will provide a unified file format, which will be usable on any analysis framework.

6. PENDING QUESTIONS

In this section, we are listing number of pending questions that have to be discussed between all the participants of the AIDA collaboration. We split them into the four previous categories.

6.1. INTEGRATION AT SYNCHRONIZATION LEVEL

6.1.1. Running modes

What running mode do we need?

Currently, at least these four modes are used:

- ILC Mode: 5 Hz Spill structure and auto-trigger
- External Mode: External trigger only
- Validation Mode: Internal trigger plus validation
- Calibration Mode: External trigger plus calibration signal

The ILC mode is used by default for the Calorimeters technical prototypes and should be as much as possible the one used for all systems.

6.1.2. Beam Synchronization

In order to synchronize all the detector systems on the machine, clocks and signals need to be fan-out. The AIDA TLU2 is the natural candidate for such a work, but a bunch of question still remains:

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- What signal is delivered: simple spill signal, BCID clock?
- What latency to choose to be compatible with all the distribution systems?
- What clock frequency to use?
- How can we align the phase of the clocks (BCID phase) ?
- Should we consider a common connector for this clock
- What electrical characteristics for the signal.

A note on the TLU and compatibility test are in preparation to address these questions.

6.1.3. External Trigger

Almost the same question remains for the external trigger fan-out: latency, connector, signal shape... It will probably mandatory to have a system for verifying the triggers alignment.

6.2. INTEGRATION AT ACQUISITION LEVEL

The optional text format has to be described, as well as the timestamps in various systems.

6.3. CONTROL/COMMAND INTEGRATION

The exact implementation of the commands for the control / command has to be implemented. This will be tested between the EUDAQ and CALICOES (work started).

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EUDAQ code is available on https://github.com/eudaq
Up-to-date documentation is available from this repository.

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ANNEX: GLOSSARY

Acronym	Definition
TLU	Trigger Logic Unit
FEC	Front End Card (SRS system)
DIF	Detector InterFace card (CALICE)
DCC	Data Concentrator Card (CALICE)
LDA	Link Data Agregator (CALICE)
GDCC	Giga DCC (CALICE)
CCC	Clock and Control Card (CALICE)
EUDAQ	
CALICOES	Calice OnlinE System (low level CALICE SW interface to HW).
Event	Physical Event (Particle, Cosmics, Noise)
Record	Data corresponding to one Acquisition/Trigger/Spill (depending on acquisition mode)
Trigger	External prompt start signal
Spill	External long signal (logical equivalent to a Machine train of bunches)
…	