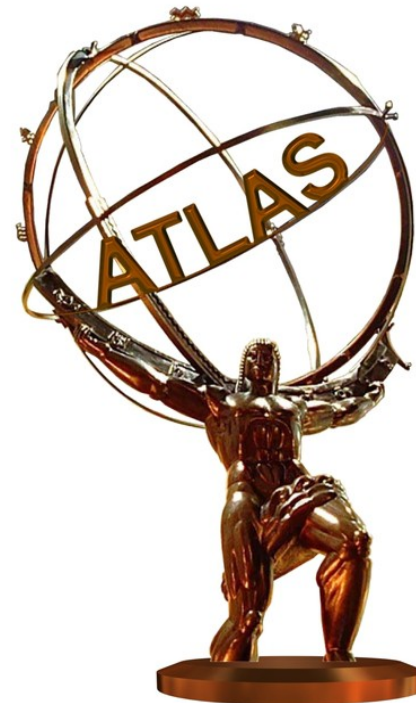# The Associative Memory system for the FTK processor at ATLAS

Saverio Citraro – University of Pisa & INFN
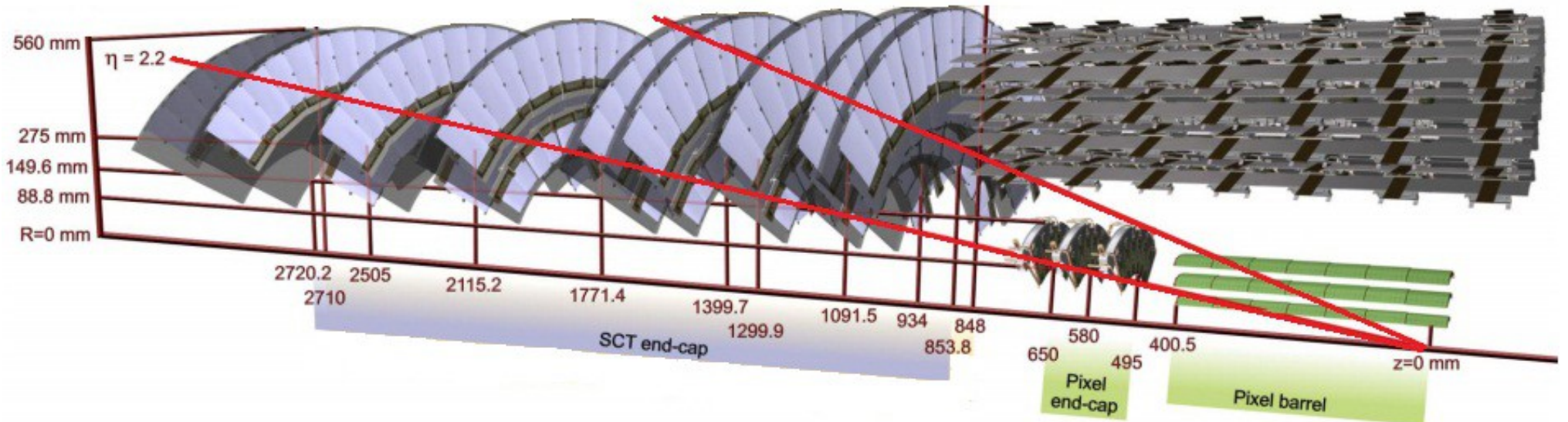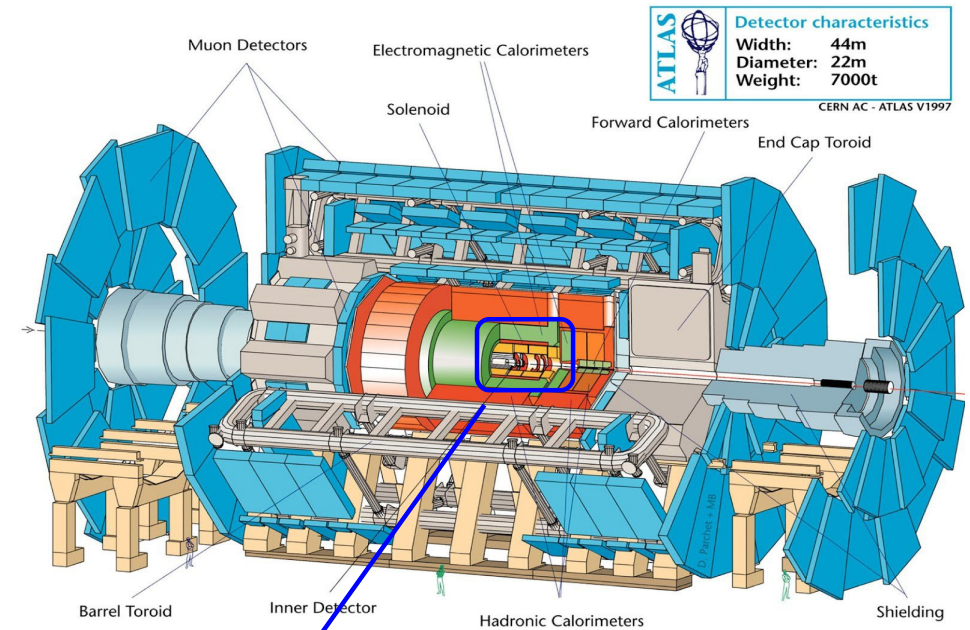
- Fast TracKer (FTK): New online silicon detector tracker for Atlas upgrade based on Associative Memory technique

- FTK working principles

- FTK architecture, with a detailed description of the

  Associative Memory system

- Test of the prototypes

  - High speed links

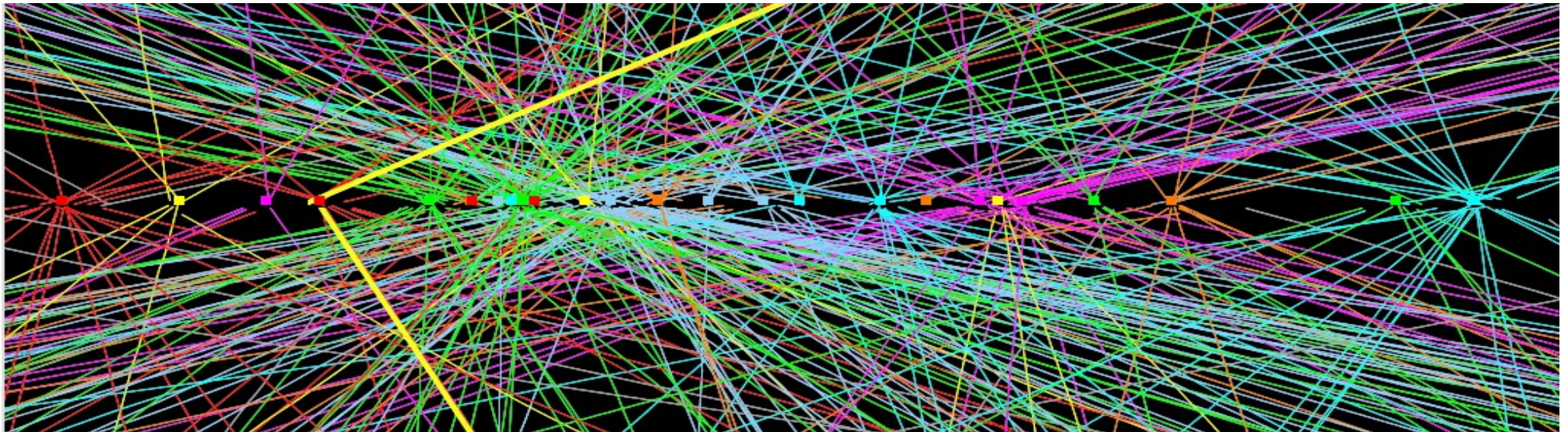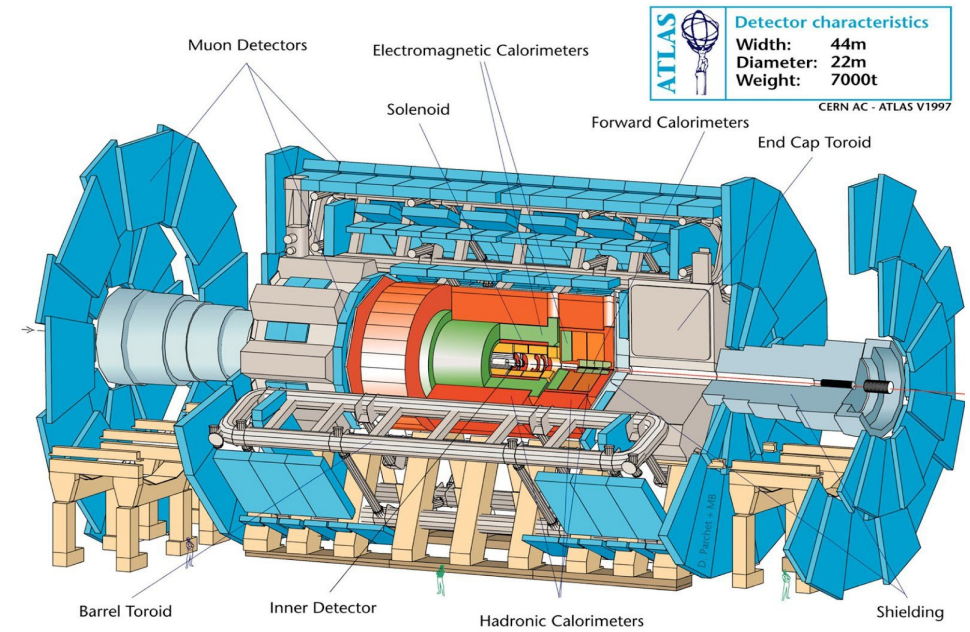 - Pattern Matching in the AM chip

  - Crate cooling

- FTK reconstructs charged particles trajectories in the silicon detectors (Pixel & SCT) at "1.5" trigger level.

- Extremely difficult task

  25 ns inter-bunch time

  ~70 overlapping events (pile-up) at Phase I highest luminosity.

Detector characteristics
Width: 44m
Diameter: 22m
Weight: 7000t

CERN AC - ATLAS V1997

Muon Detectors
Electromagnetic Calorimeters
Solenoid
Forward Calorimeters
End Cap Toroid
Barrel Toroid
Inner Detector
Hadronic Calorimeters
Shielding

$\eta = 2.2$

560 mm
275 mm
149.6 mm
88.8 mm
R=0 mm

2720.2 2505
2710
2115.2
1771.4
1399.7
1299.9
1091.5 934
853.8
848
650
580
495
400.5
z=0 mm

SCT end-cap
Pixel end-cap
Pixel barrel

- FTK reconstructs charged particles trajectories in the silicon detectors (Pixel & SCT) at "1.5" trigger level.

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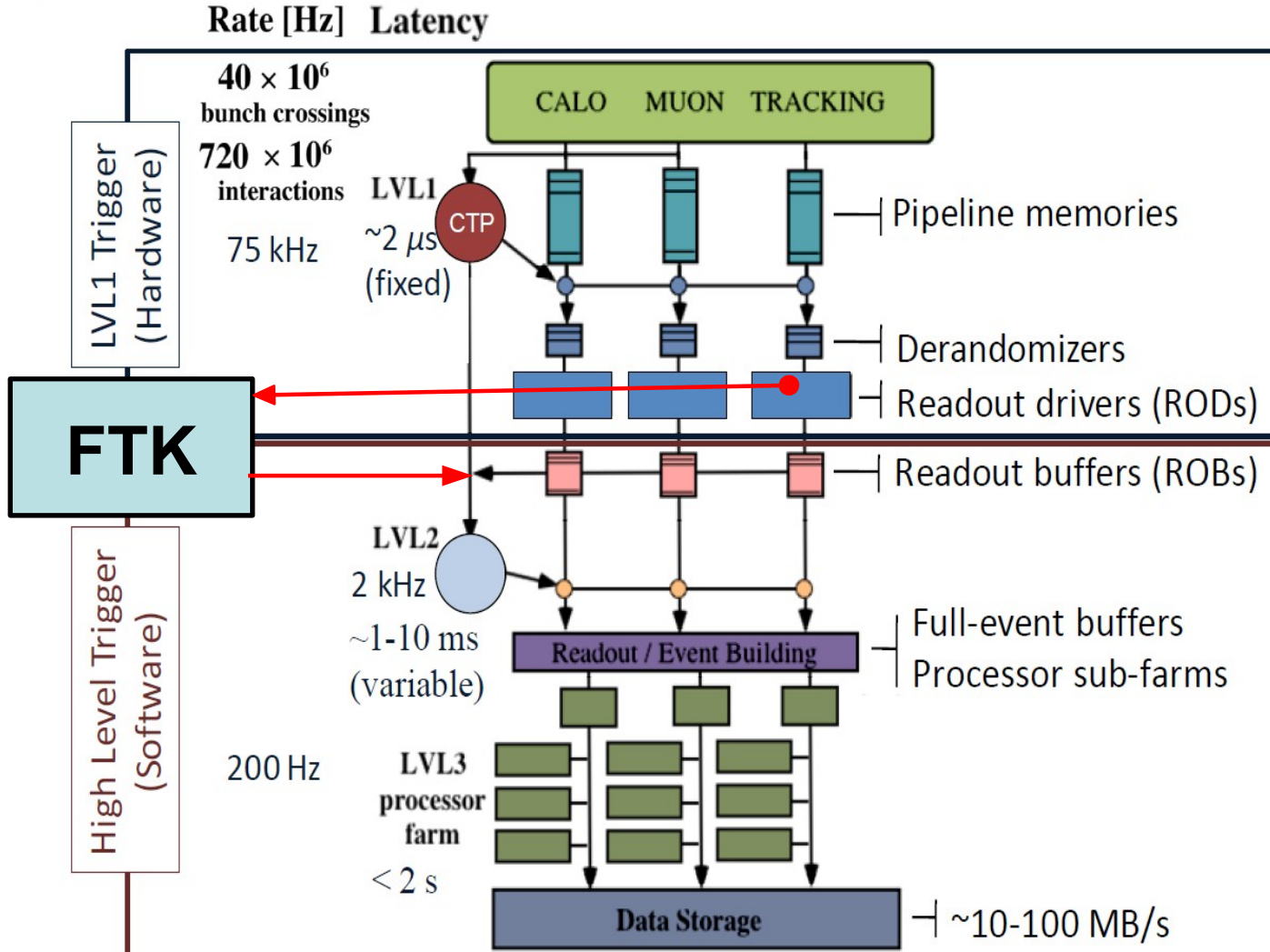 ~70 overlapping events (pile-up) at Phase I highest luminosity.

ATLAS Detector characteristics
Width: 44m
Diameter: 22m
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CERN AC - ATLAS V1997

Muon Detectors
Electromagnetic Calorimeters
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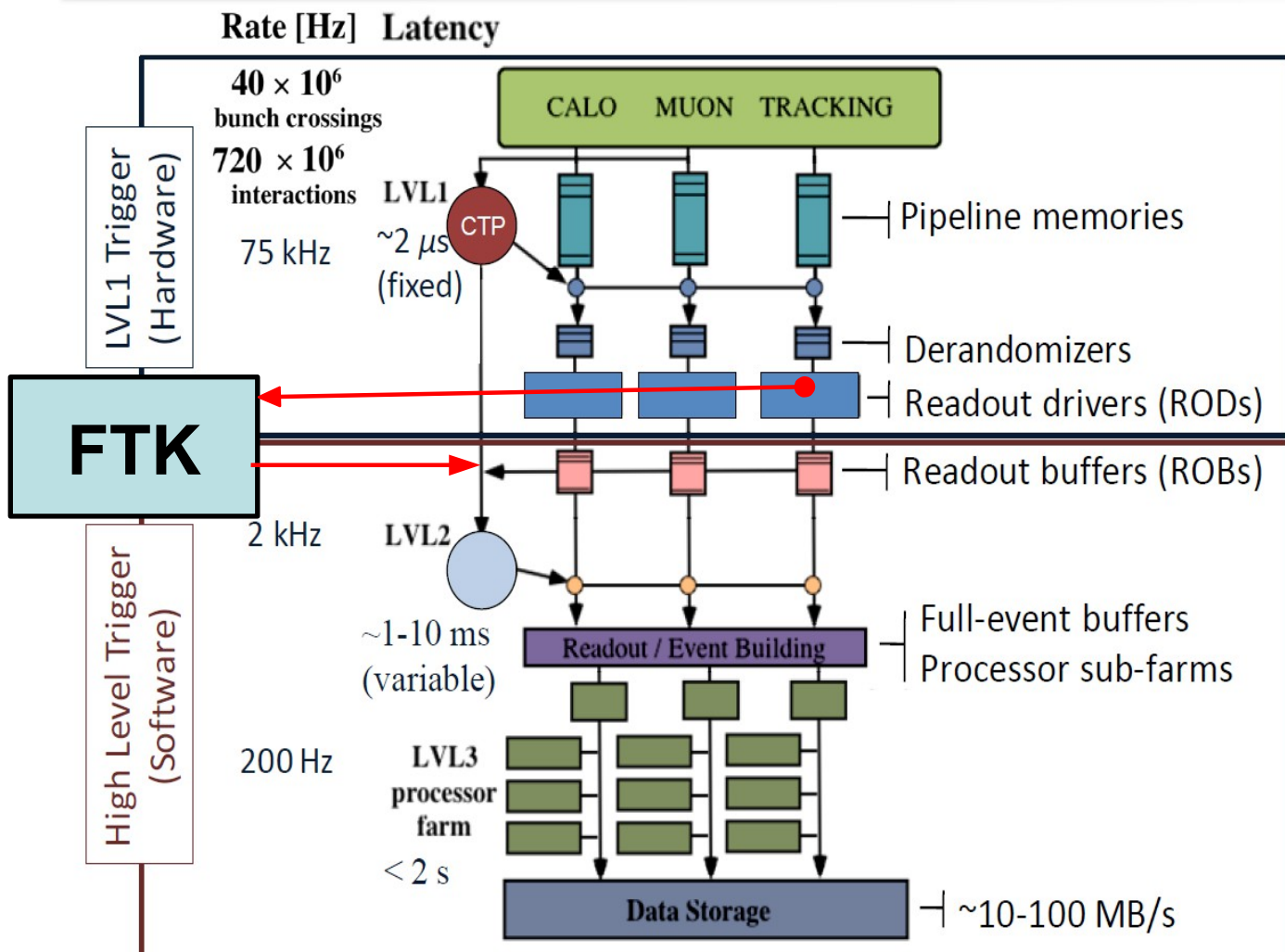Inner Detector
Hadronic Calorimeters
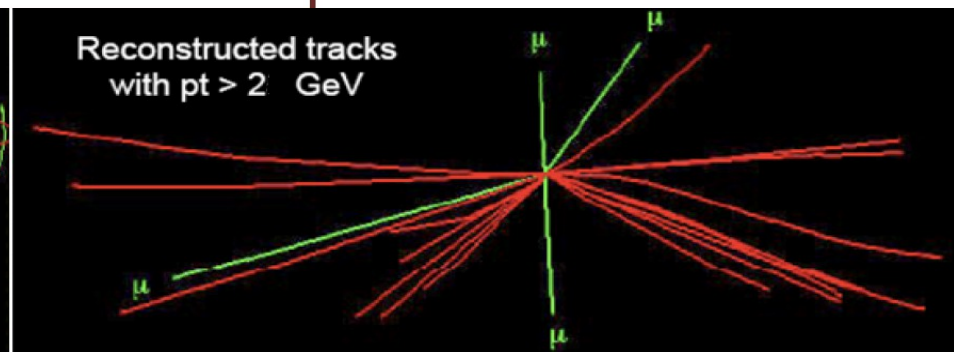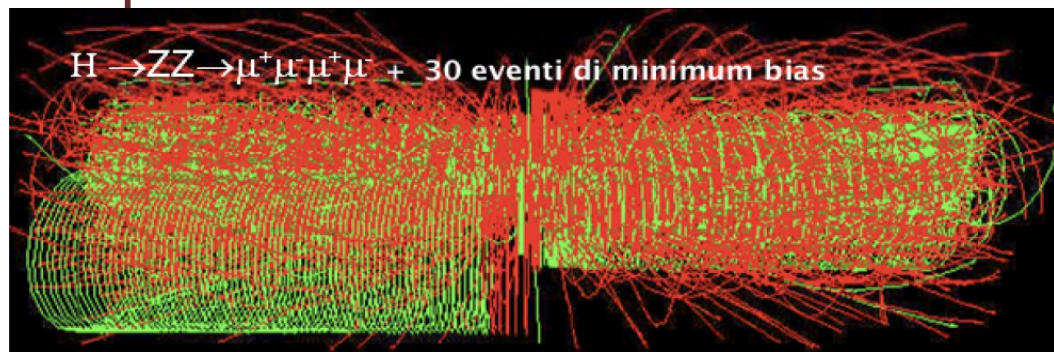Shielding

"1.5" Level Trigger processor

- Silicon data currently used only locally (ROI) and late in Level 2.

- FTK reconstructs <u>all</u> tracks with <u>PT>1 GeV/c</u> in time for Level 2.

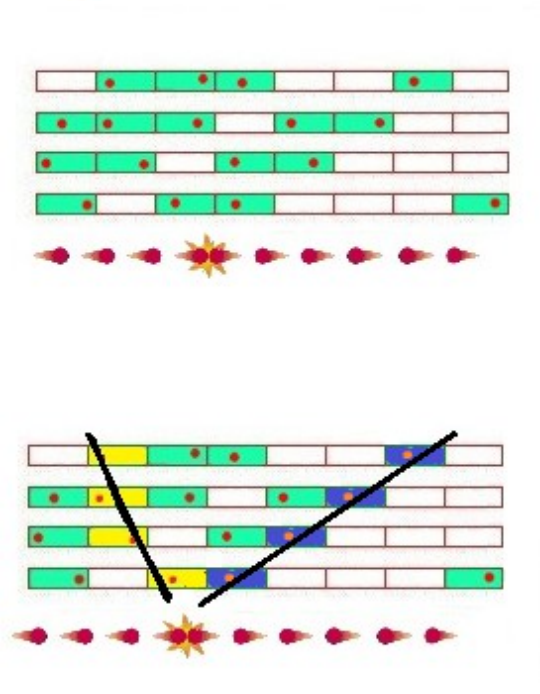- Track parameters are computed with full detector resolution.

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- FTK reconstructs all tracks with PT>1 GeV/c in time for Level 2.

- Track parameters are computed with full detector resolution.

- Pattern Bank: All the possible patterns (low resolution real track candidates) are precalculated and stored in the Pattern Bank.

Comparison

Hits

Roads

Road = Low resolution Track
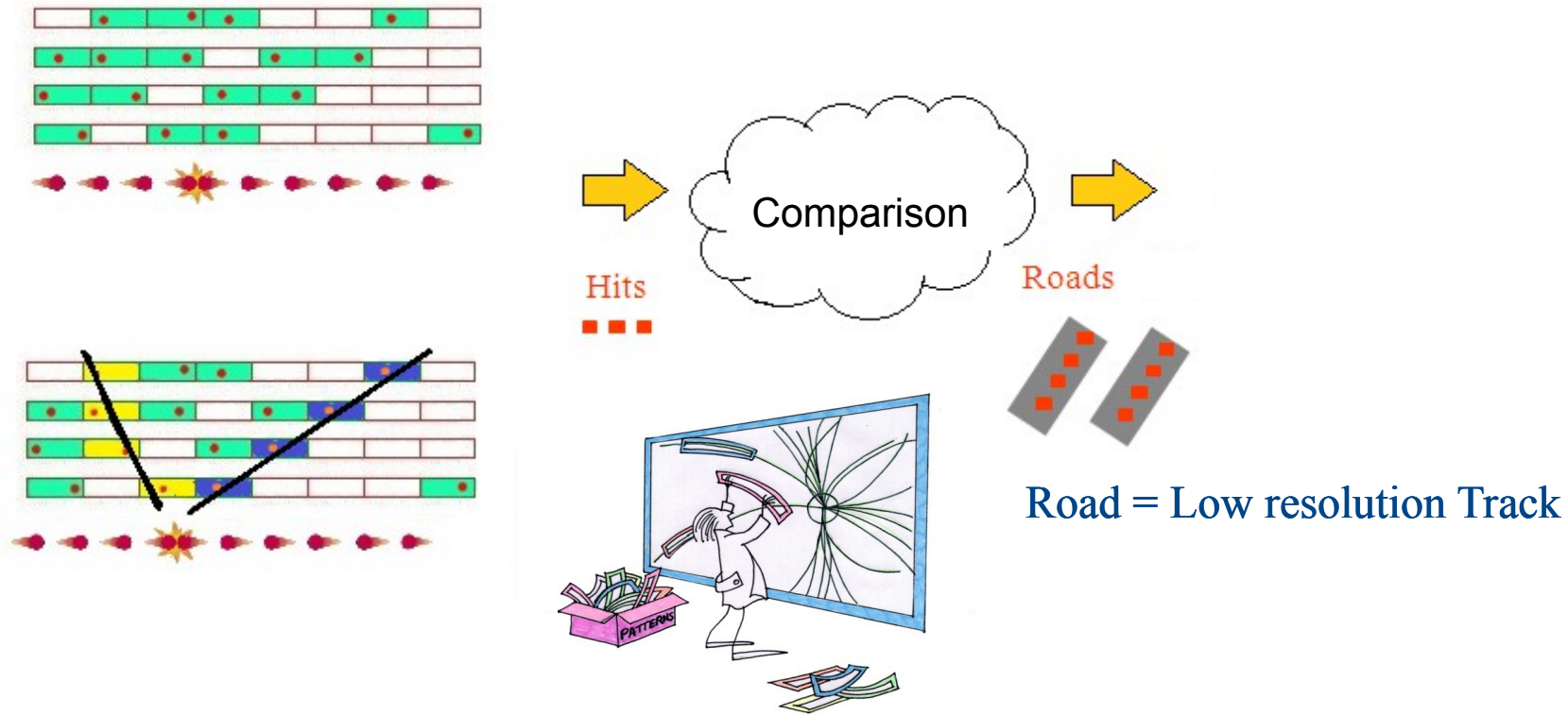
- Pattern Bank: All the possible patterns (low resolution real track candidates) are precalculated and stored in the Pattern Bank.
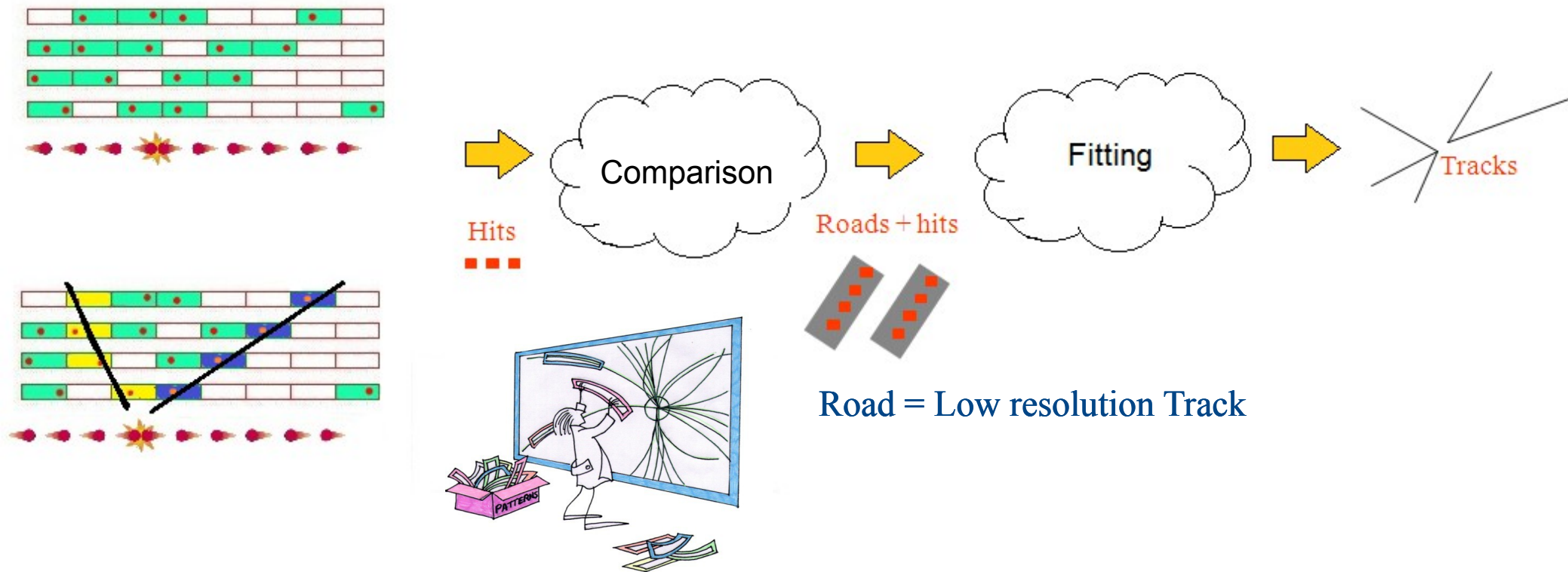- Pattern matching: All the hits in each event are compared with all the patterns in the Bank and track candidates (ROADs) are found.
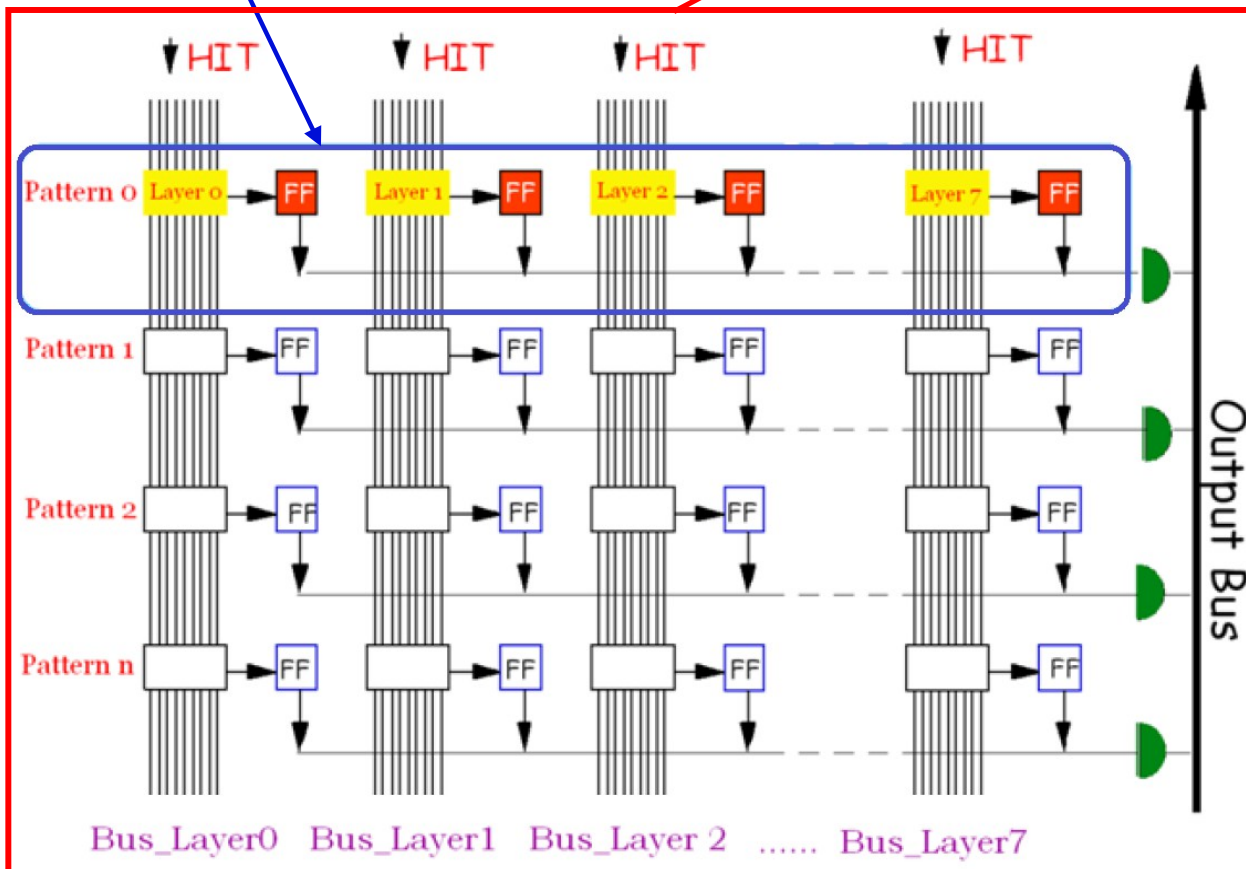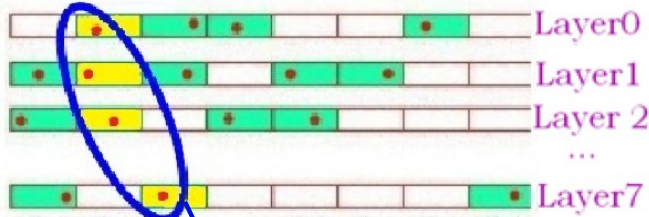
Pattern matching

Road = Low resolution Track

- Pattern Bank: All the possible patterns (low resolution real track candidates) are precalculated and stored in the Pattern Bank.
- Pattern matching: All the hits in each event are compared with all the patterns in the Bank and track candidates (ROADs) are found.
- Track Fitting: Fits of the full resolution silicon HITs contained in each ROAD determine particle tracks parameters.

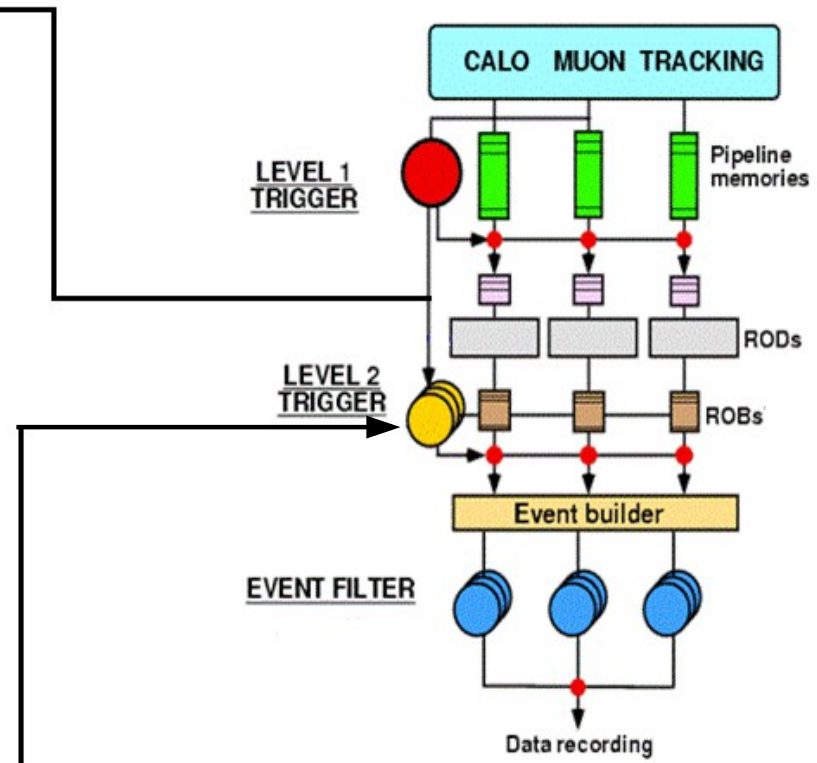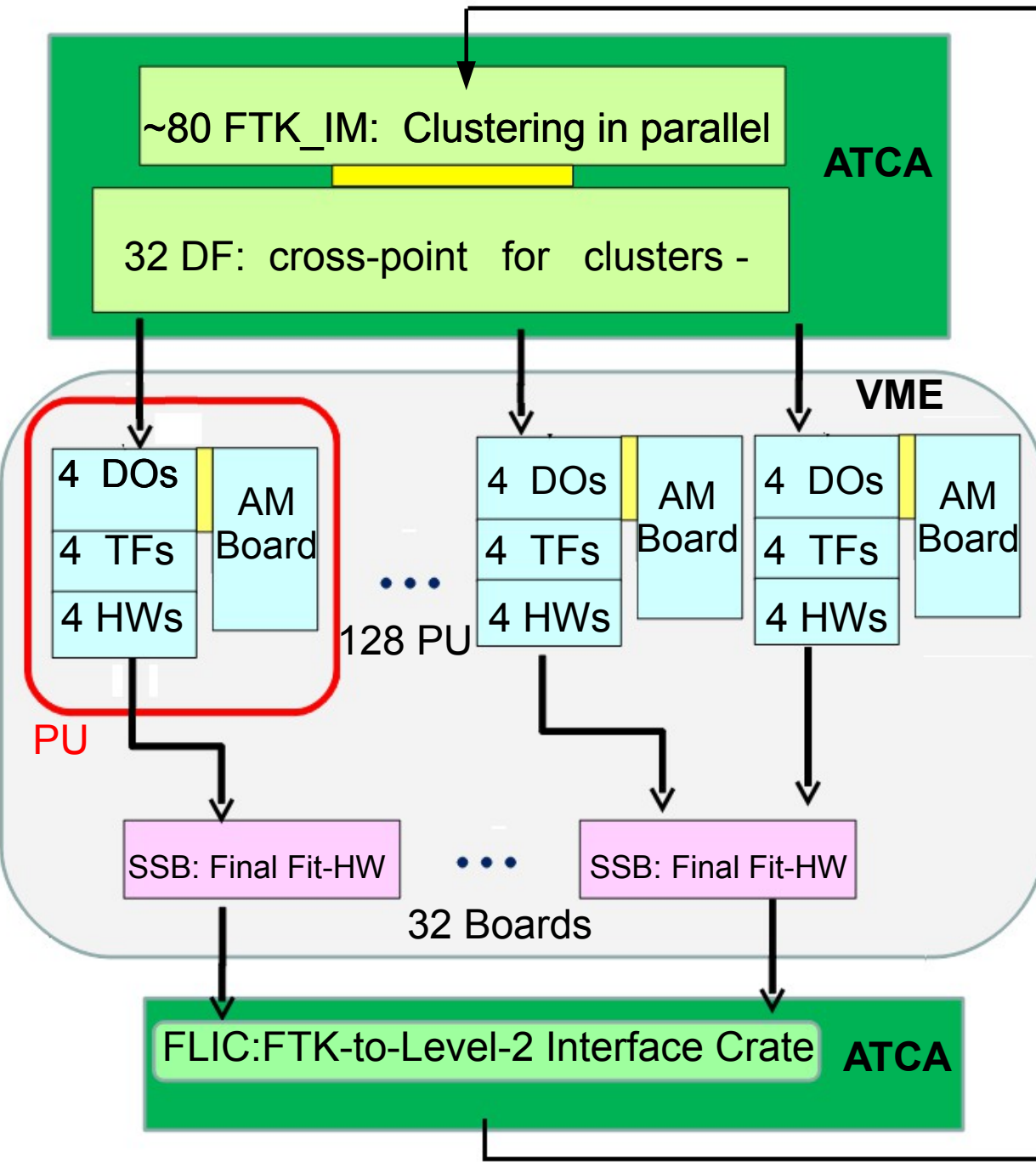AMchip

- Custom Associative Memory

- Base element of Pattern Bank

- 1 Pattern stored in 1 row

- Data from 8 silicon layers flow separately on 8 parallel buses (vertical lines)

- Programmable matching threshold

- Matched pattern's addresses are read-out

FTK architecture

- FTK processor: 8 VME Crates
  5 ATCA Crates
- Processing Unit: track reconstruction core

- 128 Processing Unit: ~1500 FPGAs
  ~8200 AMChips
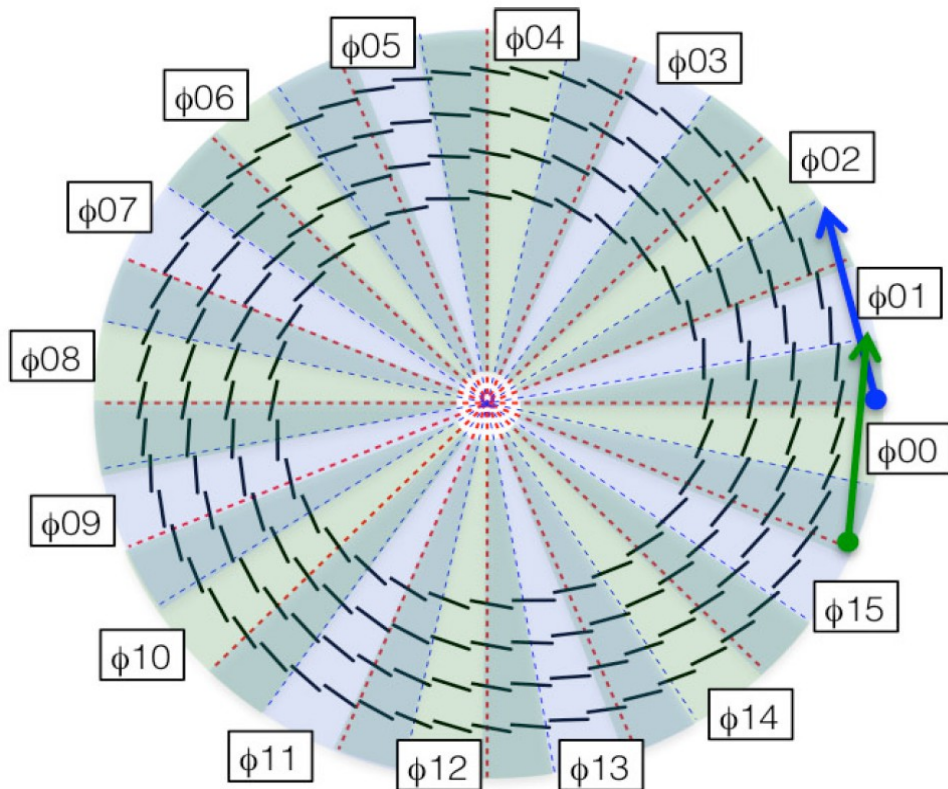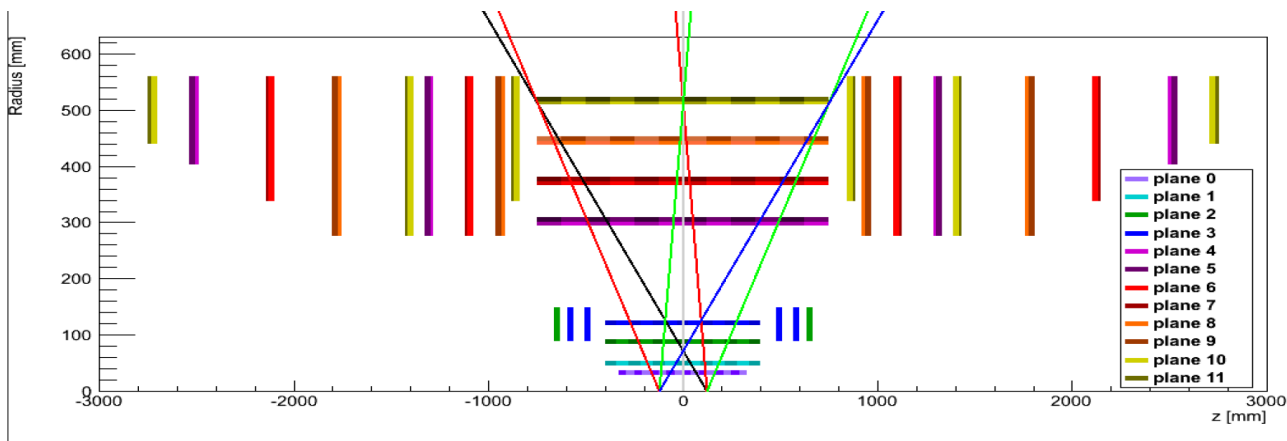
- FTK is organized in 64 η-Φ towers.

- 4 η sectors times 16 Φ sectors.

- The blue and green arrows is an example of overlap coverage.

FTK Processor Unit

AMB-FTK LAMB-FTK AUX-Board
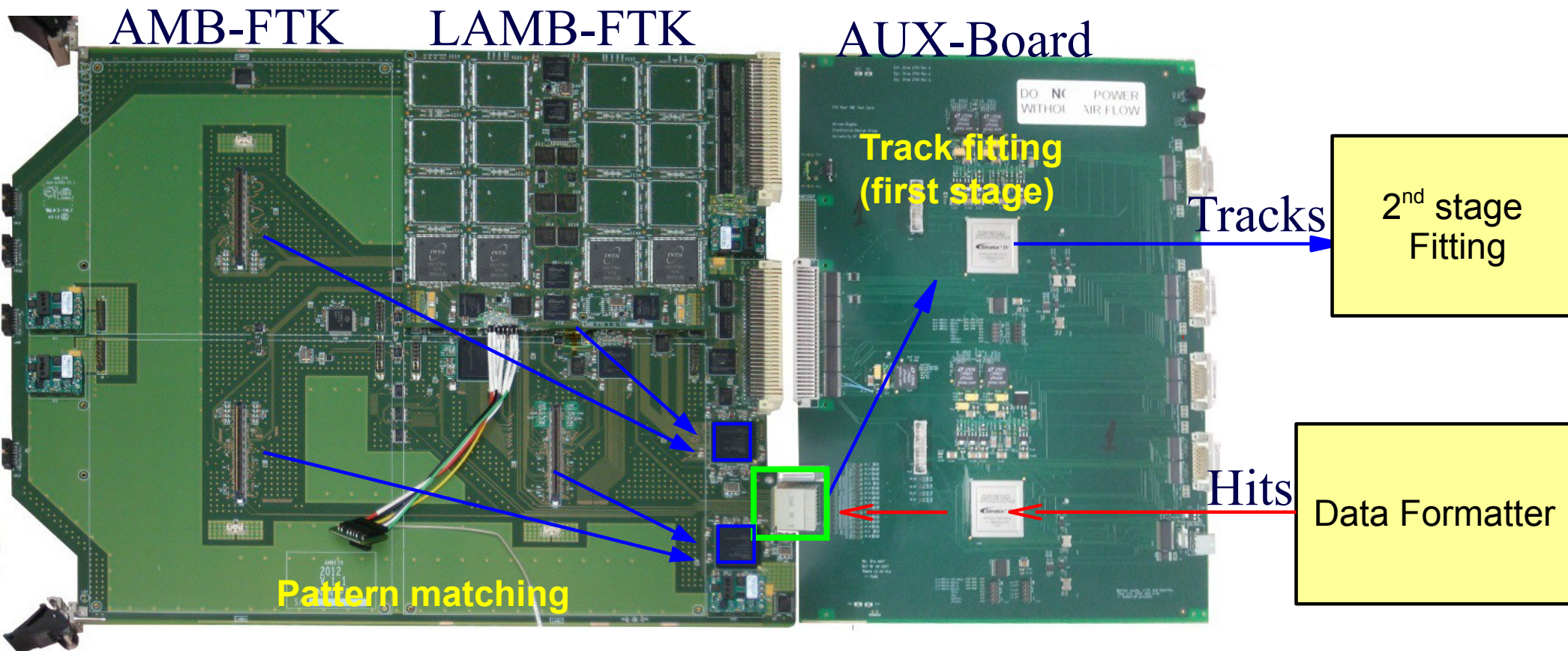
Track fitting (first stage)

Pattern matching
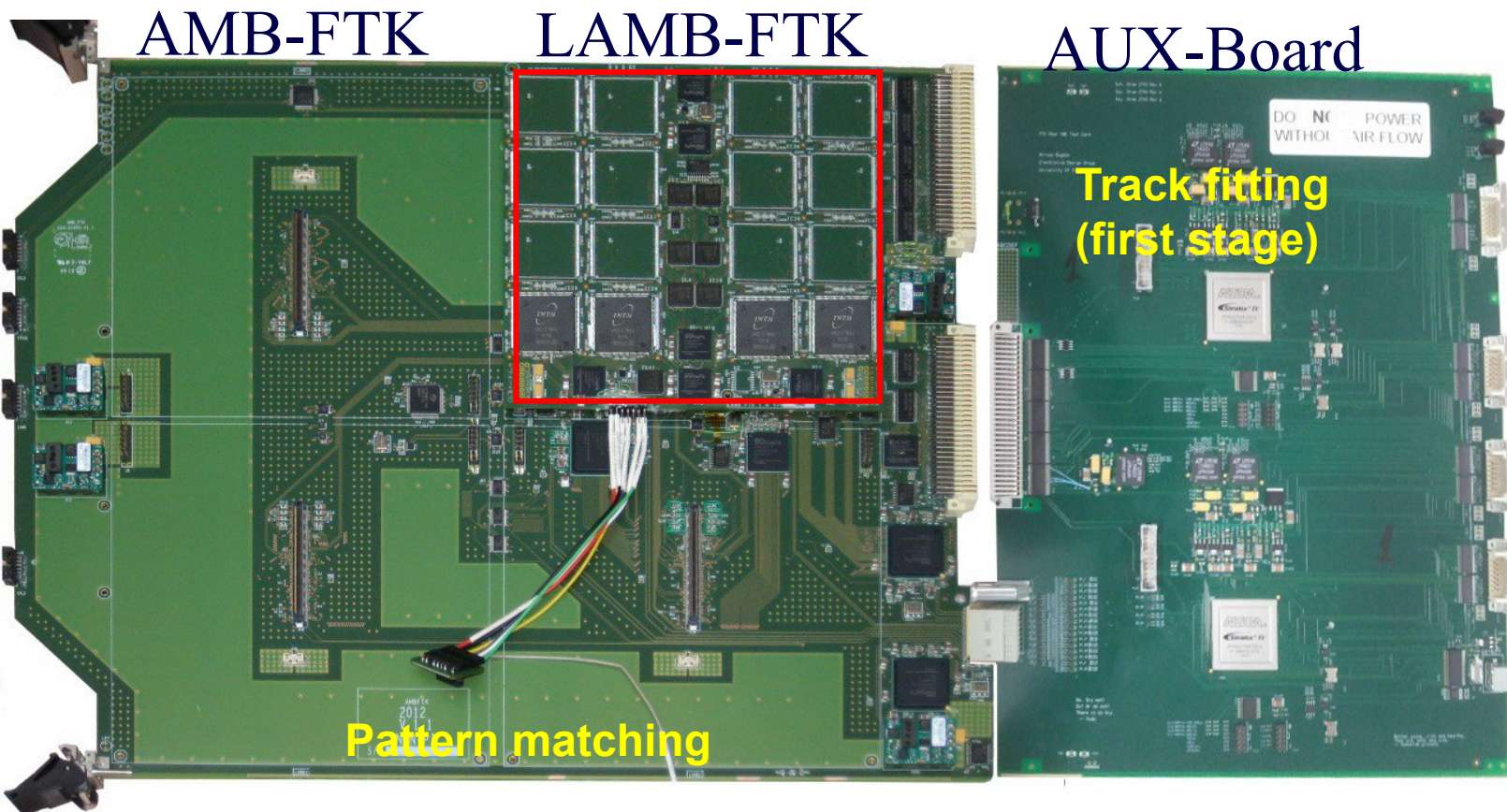
- Processing Unit: 9U VME board (AMB-FTK) + large Rear card (AUX Card) + 4 little mezzanines (LAMB-FTK).
- Silicon HITs relative to events accepted by Level 1 are distributed to all Amchips, this is done in parallel for the 64 tower (1 tower =128 AMChips).

- 1 HIT is compared with ~ 8million of Precalculated pattern.

FTK Processor Unit

AMB-FTK LAMB-FTK AUX-Board

Track fitting (first stage)

Pattern matching

Hit
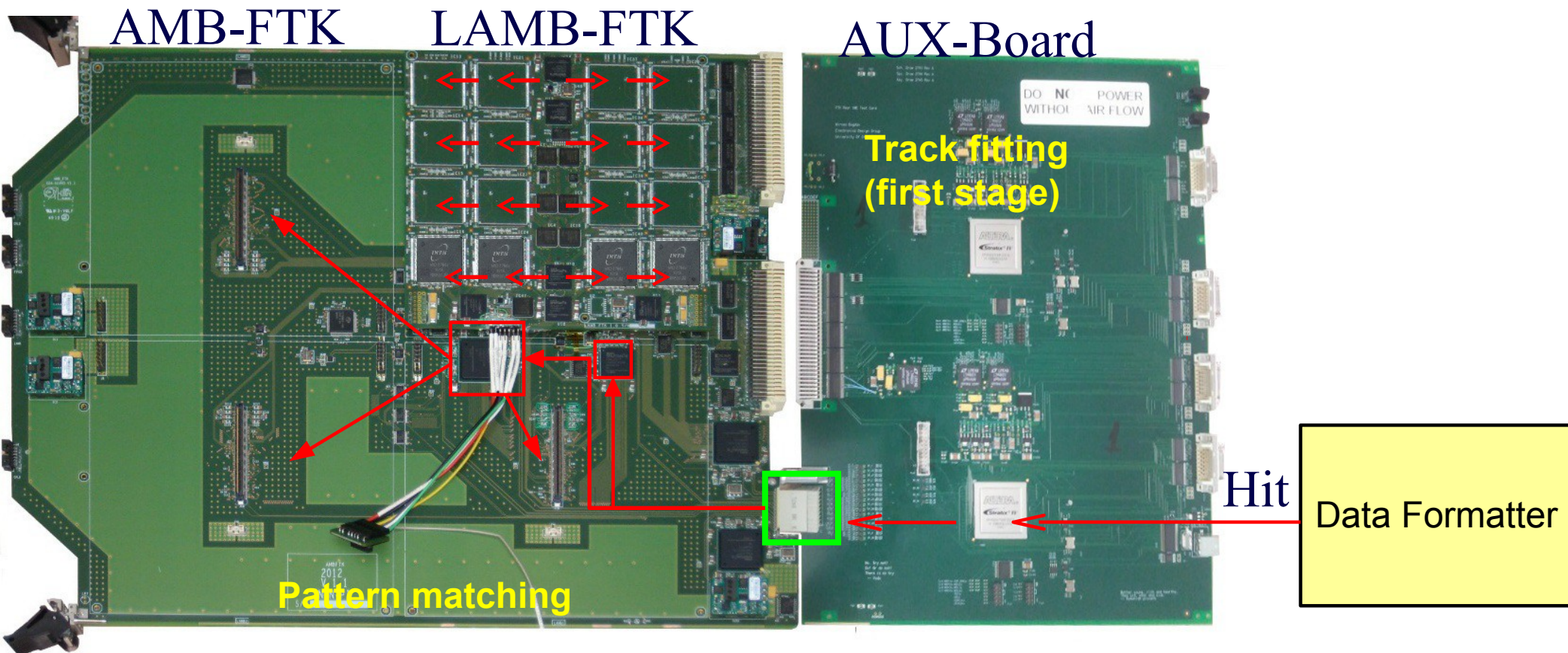
Data Formatter

- Data from Data Formatter are distributed by 12 2Gb/s serial links from Data Formatter to the Input FPGAs on the AMBoard.

- Through 4 LAMB connectors to all AMchips.

AMB-FTK   LAMB-FTK   AUX-Board

Track fitting (first stage)

Tracks → 2nd stage Fitting
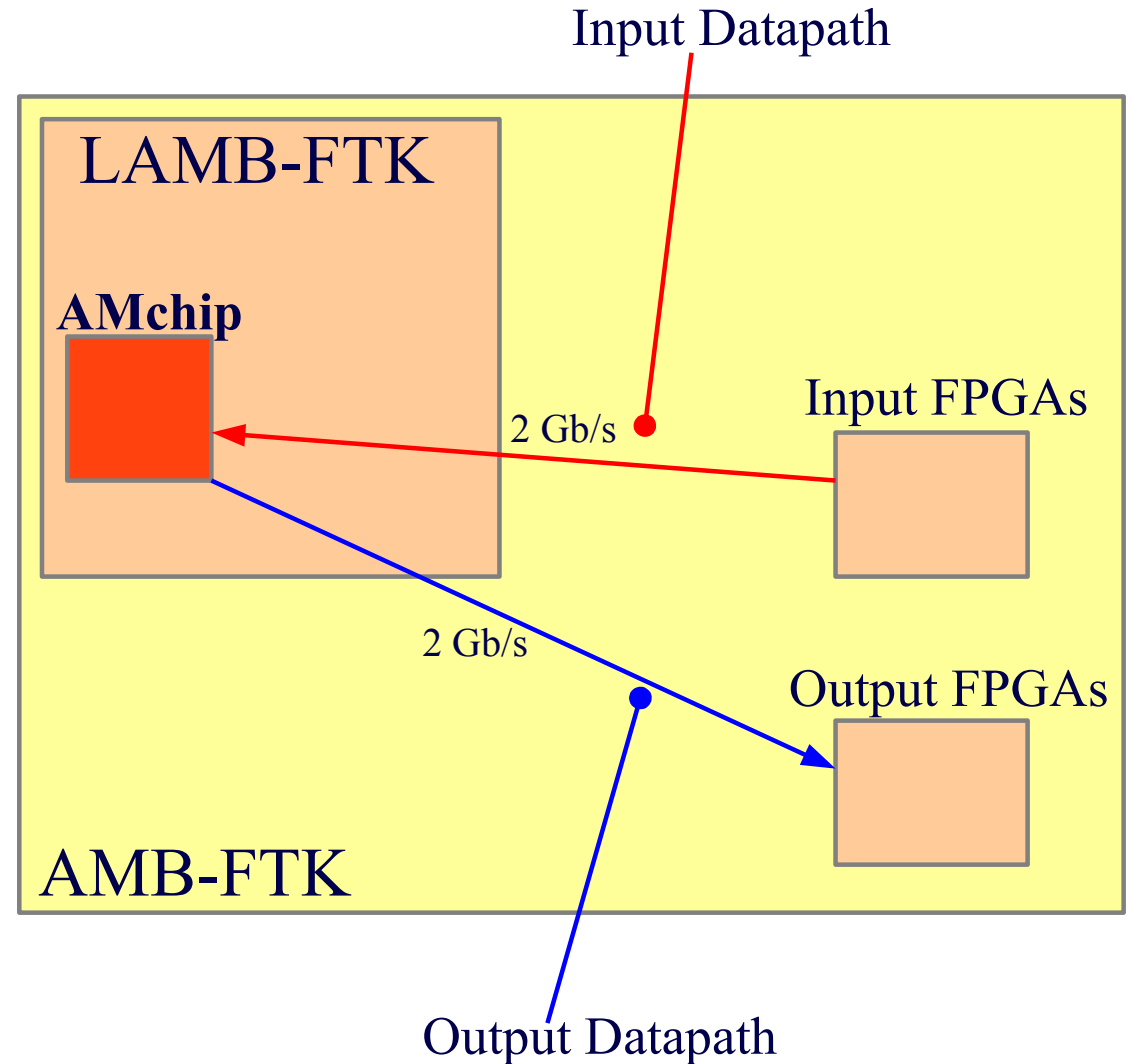
Hits → Data Formatter

Pattern matching

Matched ROADs:

- Collected on the AMB-FTK by 2 Output FPGAs (Blue squares).

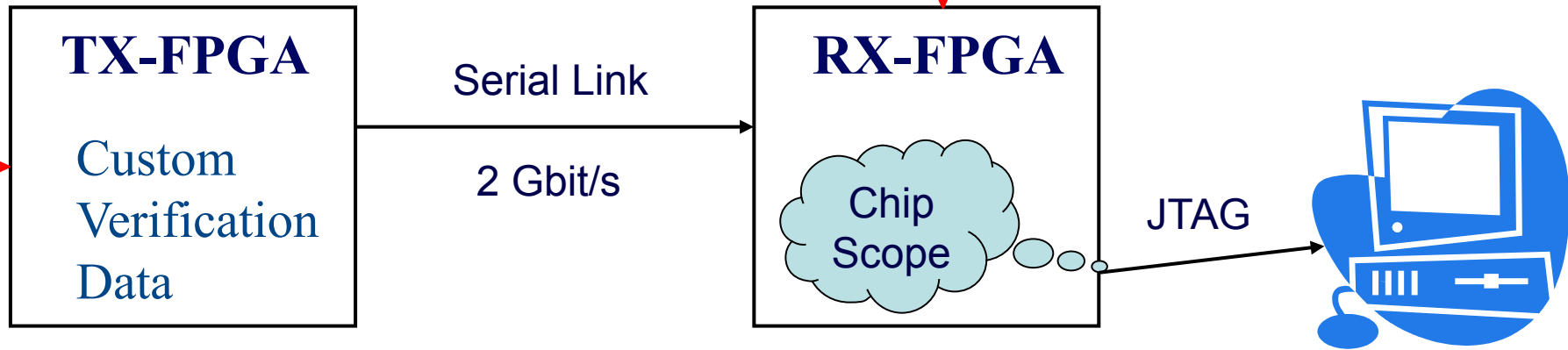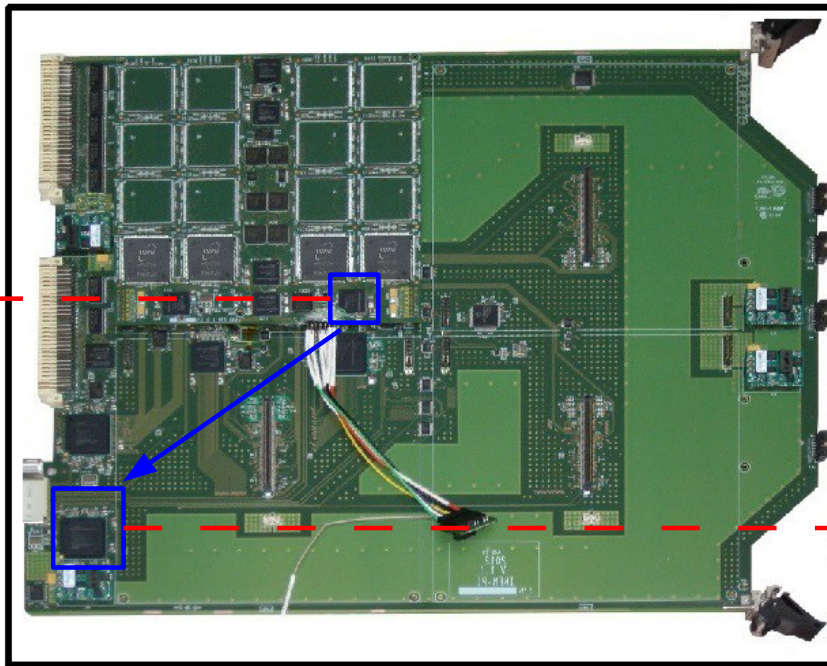- Transmitted to the AUX Board through 16 high-speed links (2Gib/s).

- Test Input Links & FPGAs to correctly send HITs to AM chips.

- Test Output Links & FPGAs to correctly collect the ROADs.
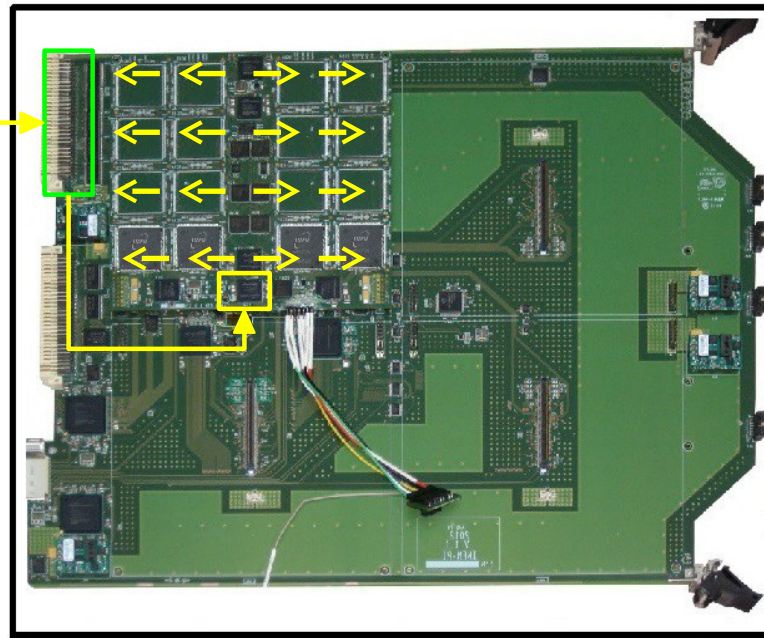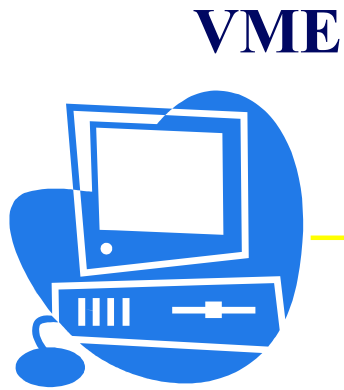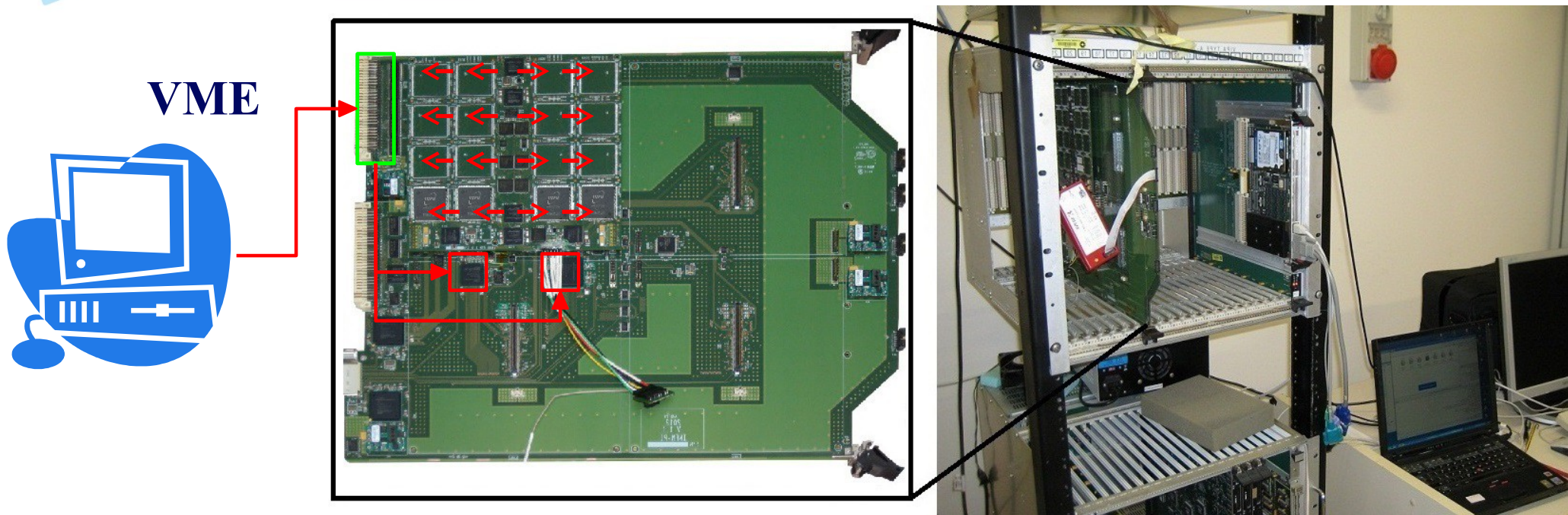
- Test the pattern matching.

Input Datapath

LAMB-FTK

AMchip

Input FPGAs

2 Gb/s

2 Gb/s

Output FPGAs

AMB-FTK

Output Datapath

TX-FPGA

Custom
Verification
Data

Serial Link

2 Gbit/s

RX-FPGA

Chip Scope

JTAG

- Sent a known pattern of data from TX and check it in RX with Logical Analyzer.

VME
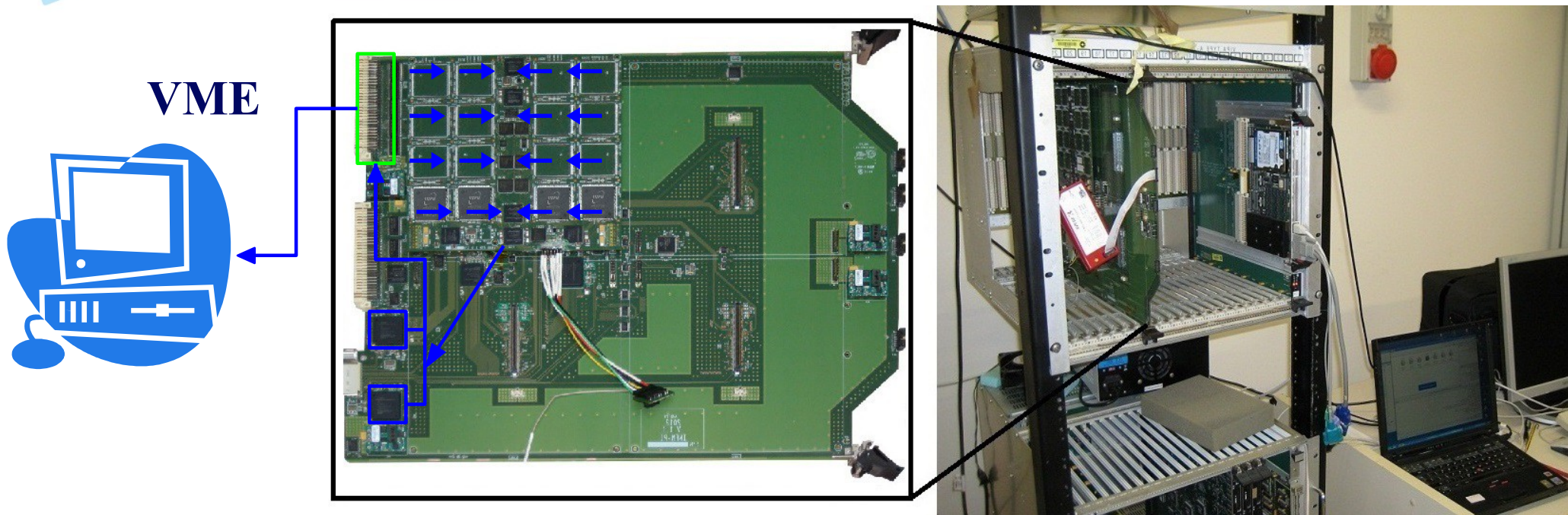

- Step 1: Store precalculated Patterns into Associative memory chips:
 - Through VME the data are stored in the AM by FPGA (yellow arrows)

VME

- Step 1: Store precalculated Patterns into Associative memory chips:
  - Through VME the data are stored in the AM by FPGA (yellow arrows)
- Step 2: Simulate silicon HITS Input:
  - Silicon HITS Input are loaded into the inputs FPGAs memory (red square) through VME.

VME

- Step 1: Store precalculated Patterns into Associative memory chips:
    - Through VME the data are stored in the AM by FPGA (yellow arrows)
- Step 2: Simulate silicon HITS Input:
    - Silicon HITS Input are loaded into the inputs FPGAs memory (red square) through VME.
    - The FPGAs transimits data to he LAMBs at full speed.
- Step 3: Check pattern matching:
    - Collect ROADs in the Output FPGAs (blue squares).
    - Compare Hardware and Simulation output.
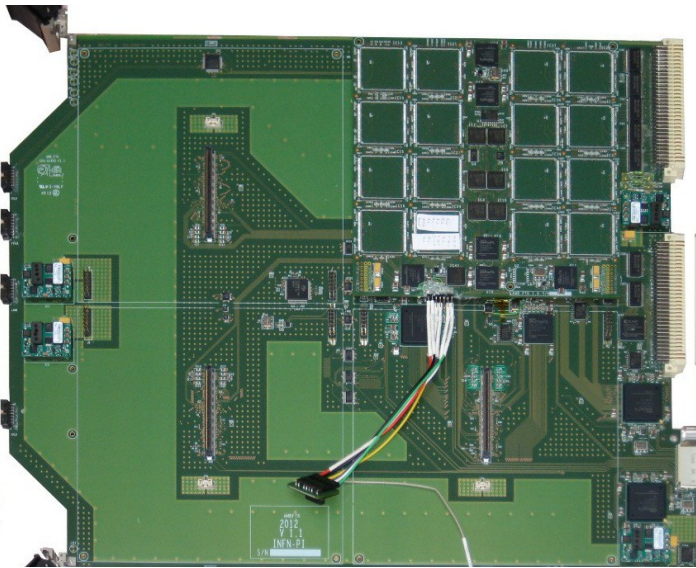
Expected power consumption
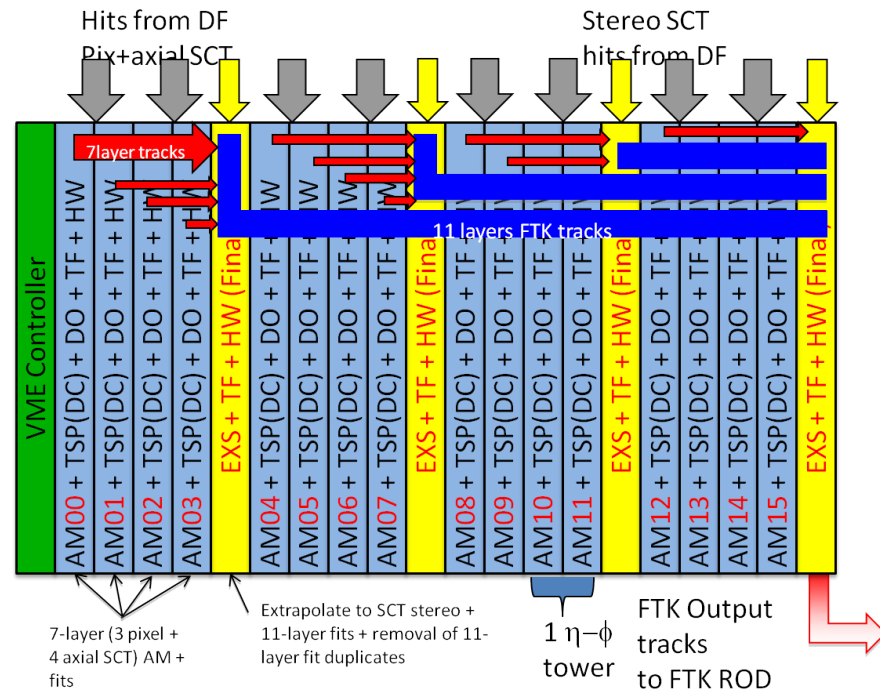1 Processing unit ~ 300 Watt.
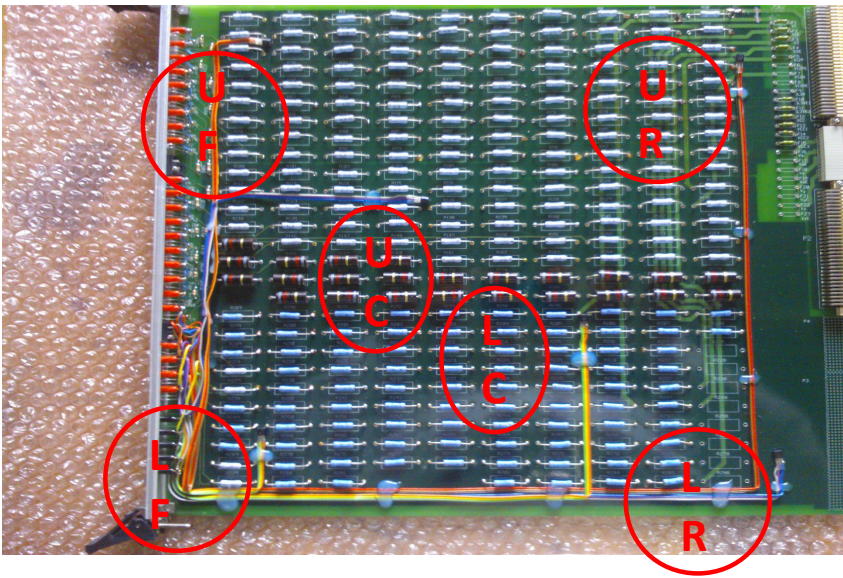
16 PU per crate (plus SSB, CPU)

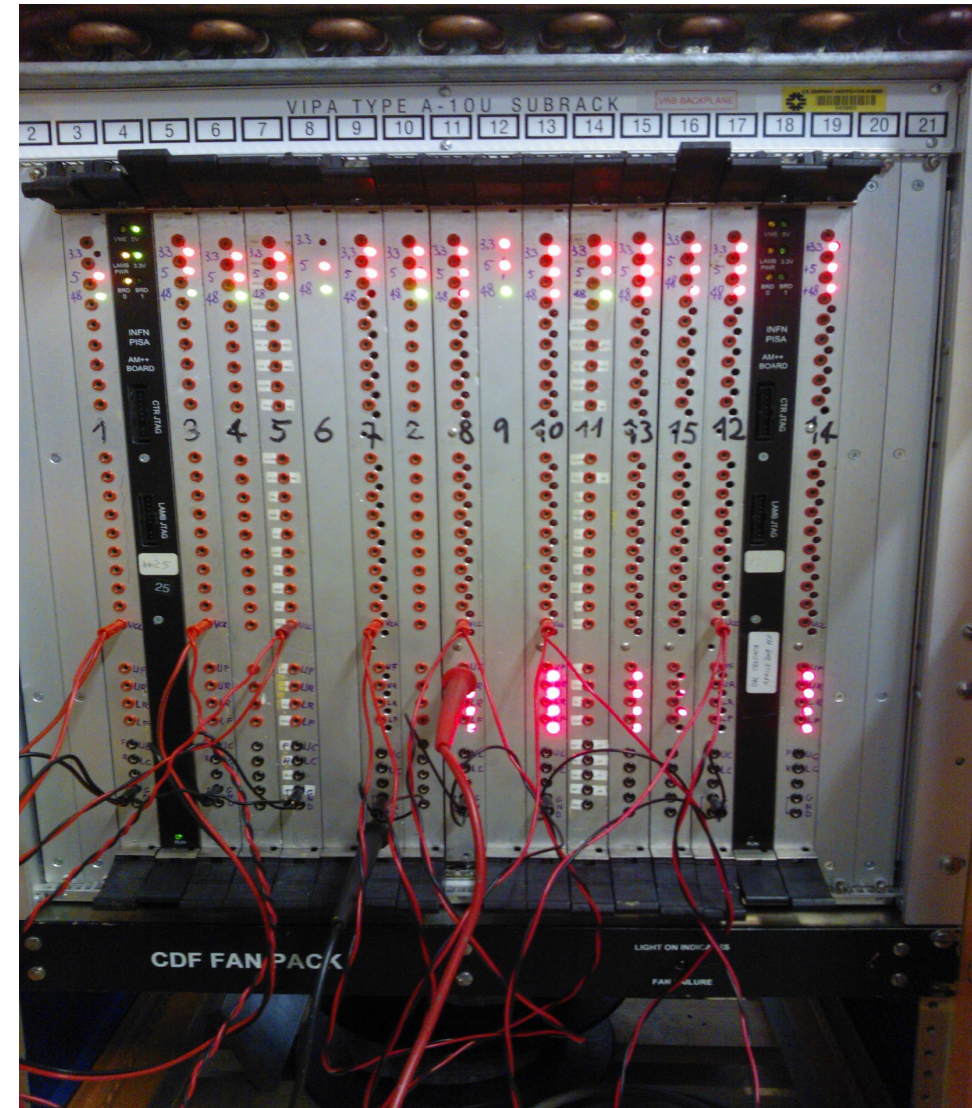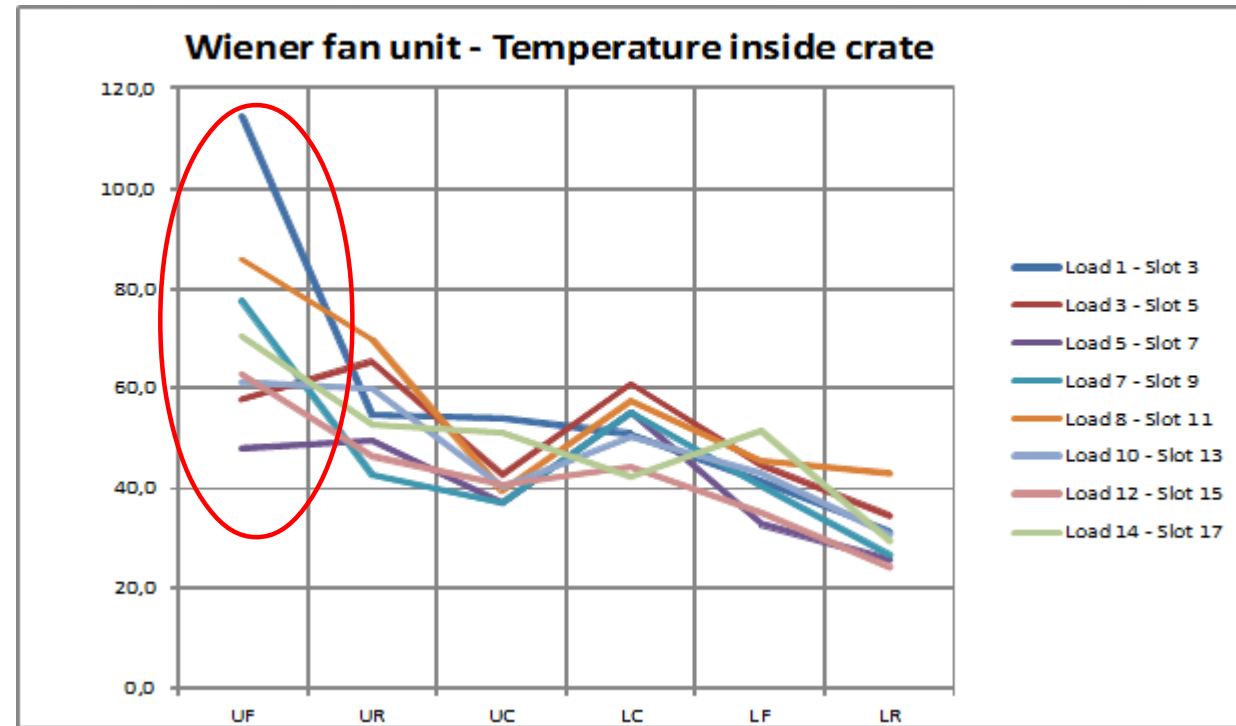5 kW per crate.

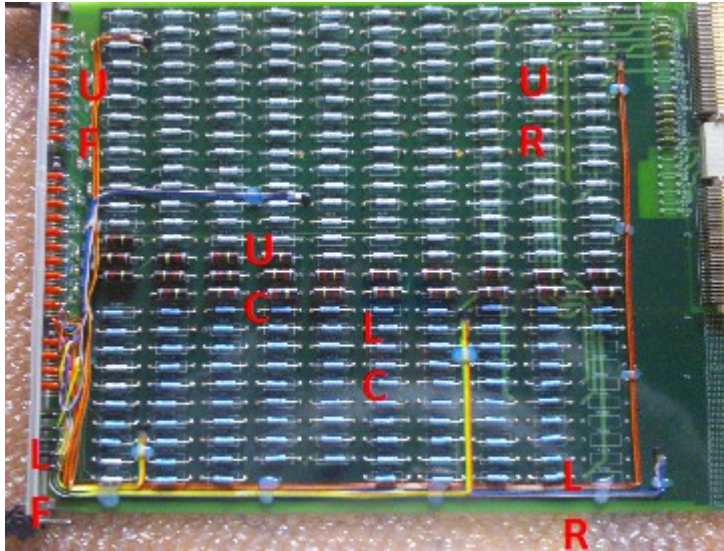Need Cooling test!

Power supply voltages:
- 5V
- 3,3V
- 1,2V

- Cooling test work in progress INFN PAVIA.

- Power consumption simulated with resistors.

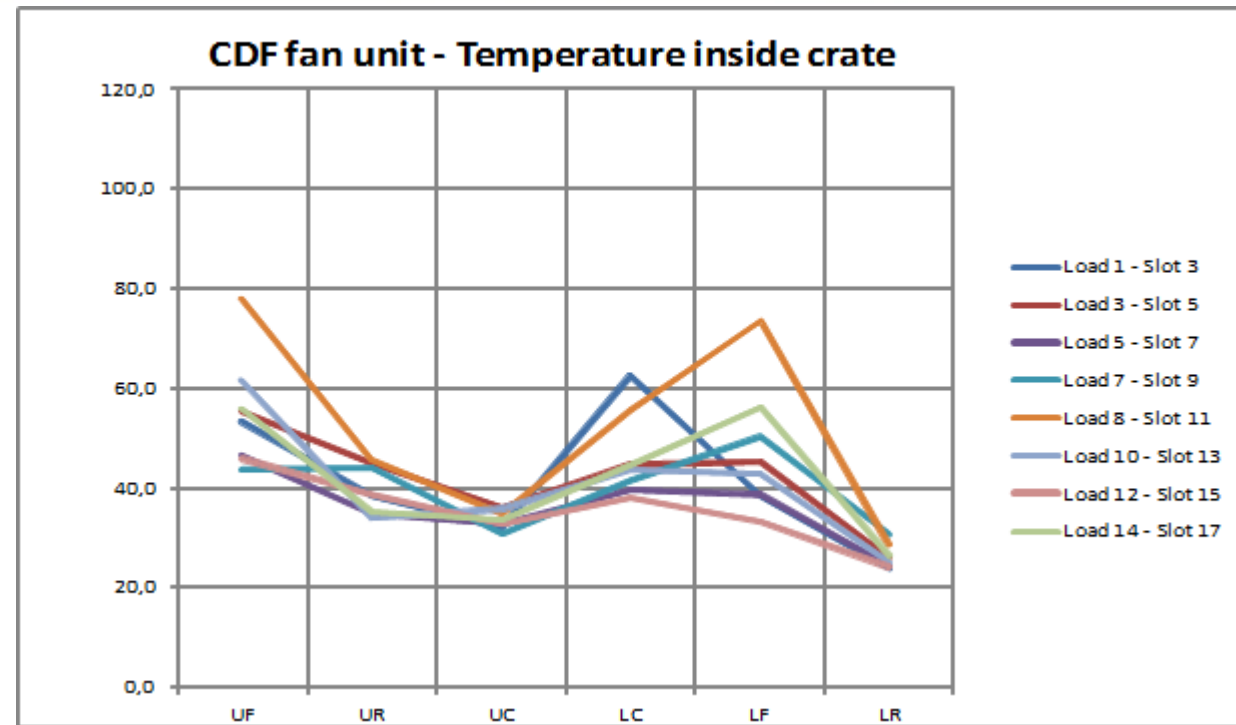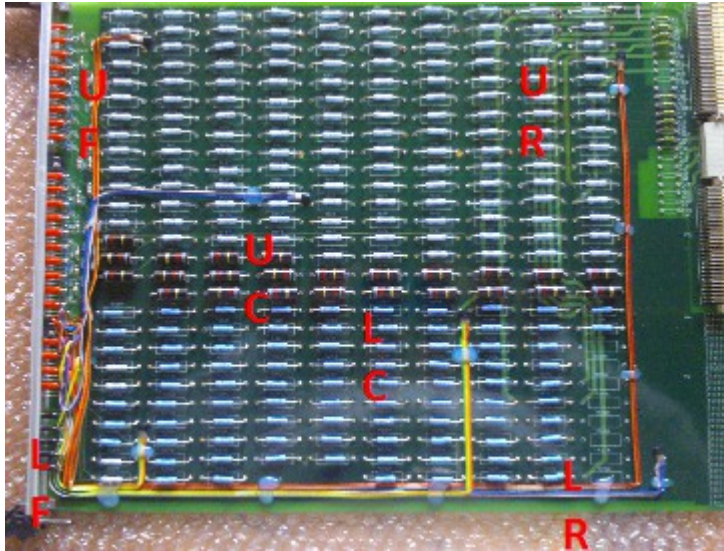- Six sensor used to measure the temperature in the crate (red circles)

Cooling Tests Result without chiller

Wiener fan unit - Temperature inside crate

- With the Wiener Fan we have a peak of temperature in the up side of crate.

- The reason is the power of the fans.

Cooling Tests Result without chiller

- With CDF Fan the temperature is lower but there is a peak in the down front side of crate.

- The reason is the missing fan.

- Cooling test are in progress: next step is to resolve the problem with fans and use the chiller.
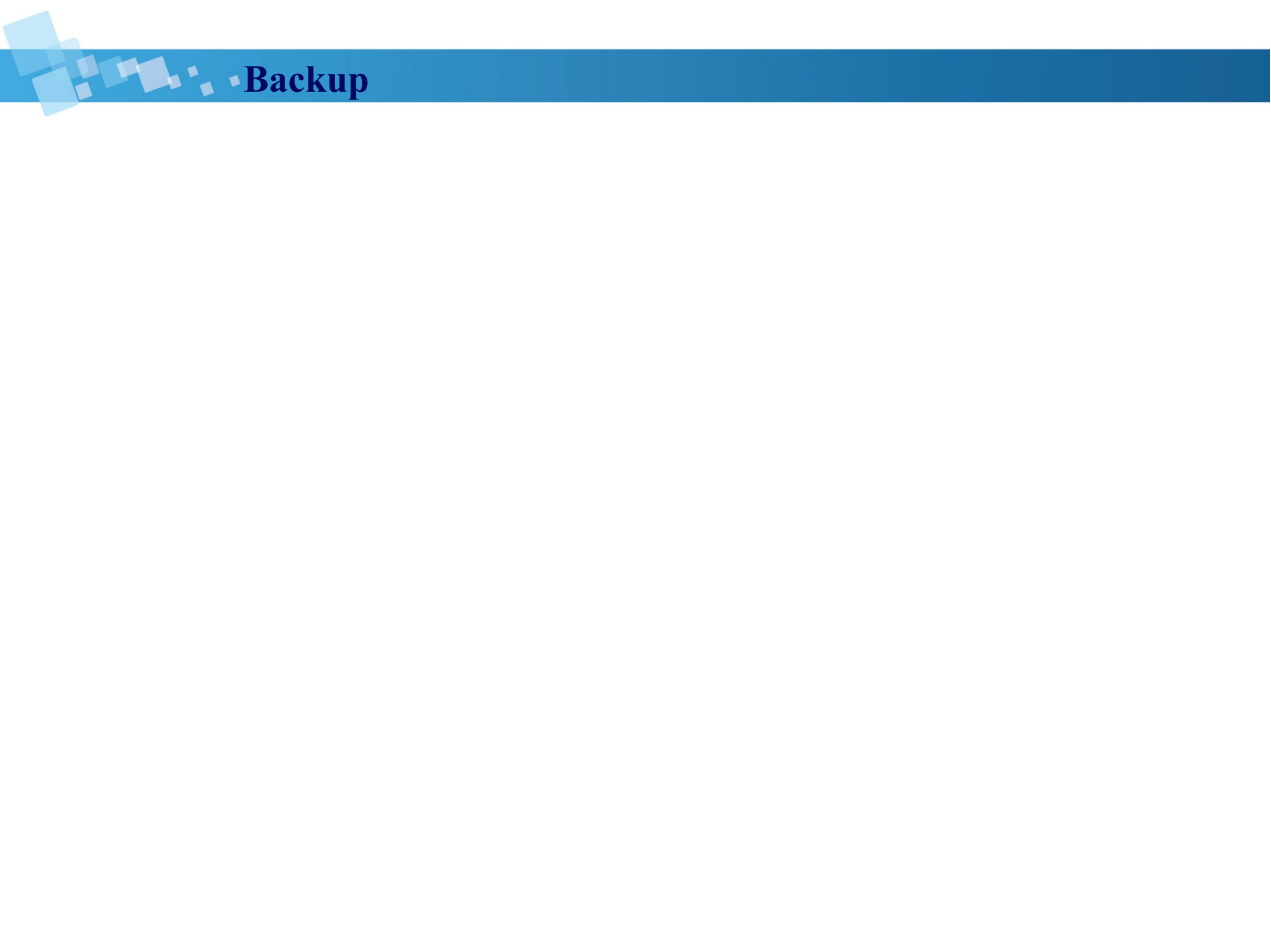
- AM system test results were excellent.

- Cooling test are in progress.

- Now we are improving the system for the final version.

- June 21, 013: ATLAS Collaboration Board approved the FTK Technical Design Report.

- We will install the system for the next LHC power on, in 2015.

Thank You!

Backup