Design of a Portable Test Facility for the ATLAS Tile Calorimeter Front-End Electronics Verification

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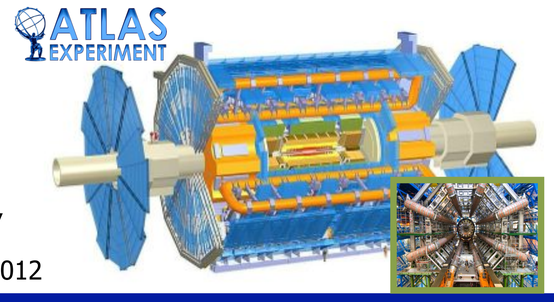
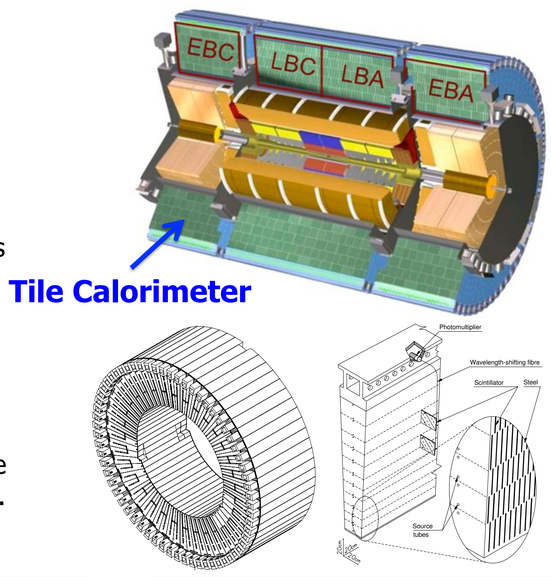
ATLAS

- **LHC (Large Hadron Collider)**
  - A Particle accelerator designed to handle proton-proton collisions at a center of mass energy up to 14 TeV built by CERN and started to run in 2008
  - Lies in a tunnel 27 km in circumference 100m under ground France-Swiss boarder at Geneva, Switzerland
  - Feb. 2013 to end 2014: the first Long Shutdown for Maintenance of LHC and its detectors
- **ATLAS(A Toroidal LHC Apparatus)**
  - One of the general purpose detectors of LHC
  - 45 meters long, 25 meters in diameter and 7,000 tons
  - A collaborative Experiment involving more than 3,000 physicists from 175 institution in 38 countries
  - Main components : Muon spectrometer, Magnet system, Inner Detector and Calorimeters
  - Contribute to the discovery of the Higgs Boson in July 2012



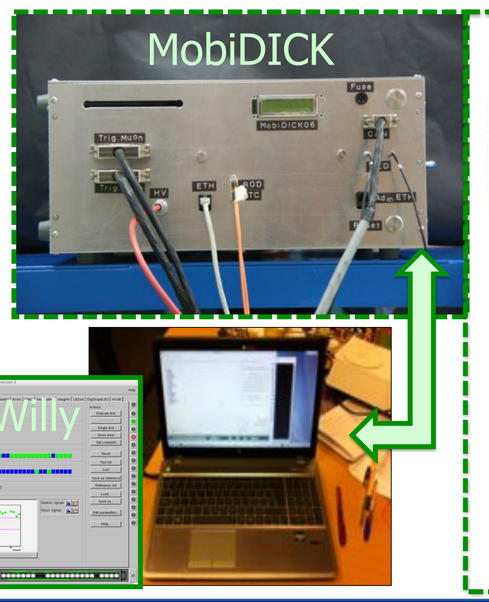
Tile Calorimeter

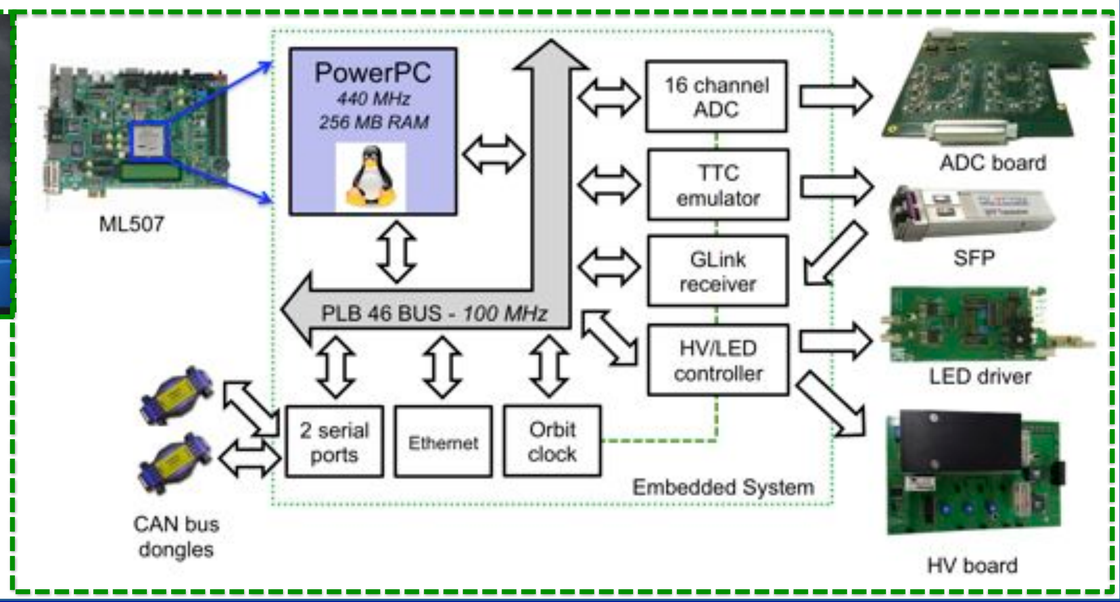
- **Tile Hadronic Calorimeter**
  - The ATLAS calorimeter system is composed of EM calorimeter and Hadronic Tile Calorimeter
  - The Hadronic Tile Calorimeter is a sampling calorimeter where iron plates are interleaved with plastic scintillating tiles.
  - Covers the pseudo-rapidity region of -1.7 to 1.7, and is split into three barrels, two extended barrels and one central long barrel instrumented on both sides.
  - 64 modules covers the entire azimuthal range of each barrel and are radially segmented in three layers.
  - The light produced in the tiles is guided on each side of the module to the outermost region, where the PMTs and the front-end electronics are located.
  - Groups of tiles that define calorimetric cells are read out by the same PMT.



MobiDICK 4

- **A re-designed mobile drawer integrity checking system**
  - the new generation of portable test-bench for the full certification and quality checking of the super-drawers in the Tile Calorimeter during the maintenance periods and beyond
  - Replaces the obsolete VME technology and upgraded with an FPGA
  - Expands fault coverage and can adapt to new front-end electronics : uses an FPGA based embedded system which controls different commercial devices or custom components. These provide the functionality required to certify a super-drawer.
  - Increases the portability and reliability, provides a quicker turnaround time and improves the overall test-bench coverage
- **Hardware**
  - Xilinx ML507 evaluation board : Controlling all the hardware
    - Virtex-5 FX70T with hard core PowerPC @ 440MHz
    - Small Format Pluggable (SFP) module
    - 10/100/1000 Ethernet port
    - Compact Flash slot
  - ADC Board
    - Digitizes analog trigger tower signals from the drawer
    - Two ADS5271 ADCs from Texas Instruments
    - In total 16 ADC channels (8 channels each ADC) and 12-bit x 40 MSPS
    - Serial LVDS output interface
  - HV(High Voltage) Board
    - Feeds PMTs with -830V through TTL input interface
  - LED Driver Board
    - Generates a 20 ns wide pulses to drive two LEDs through TTL output interface
  - CANBUS is used for slow control and ADC-I board readout
- **Software** (Willy : Graphic User Interface)
  - implements a client-server architecture between the ML507 (server) and a laptop (client)
  - the client allows users to manage the different tests needed for certification, while the server controls hardware, extracts and processes data (and sends results to the client)
- **Portable design**
  - A light custom aluminum box
  - Size: 35 cm x 40 cm x 20 cm
  - Weight: ~ 4 kg
  - Forced air cooling system

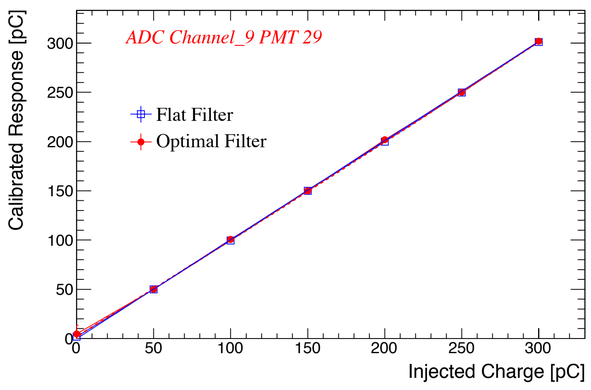




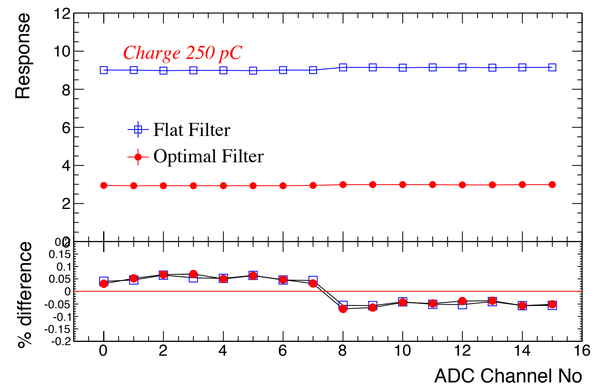
Performance and characterization system tests

MobiDICK is implemented with real-time computing hardware using a FPGA based board for intense maintenance campaign periods, using commercial hardware and out of the shelf components including the FPGA board itself. The implementation of new tests don't require knowledge of VHDL for firmware programming, as they can be implemented in C++ in the client. With this tool we extended the lifetime of the test-bench for 10 years and improved the quality assurance of the maintenance.

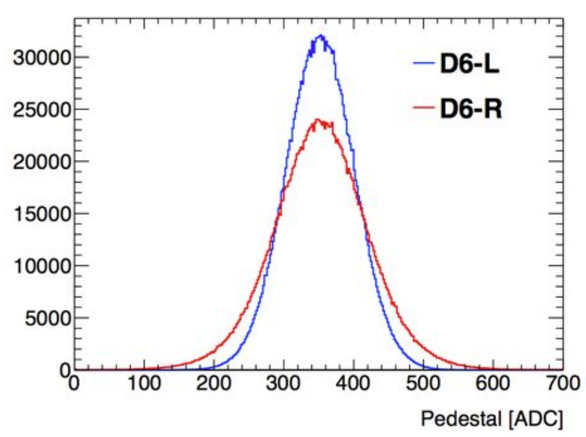
- Improving Real-time processing
  - The New MobiDICK's Power PC embedded motherboard supplies the computing power to handle the data in real-time with a combination of VHDL modules and C++ algorithms
  - The FPGA processes an enormous amount of data and select them at the Level 1 trigger rate of 100 kHz. This data can be read in C++.
  - The results are updated in real time.
- New Functionalities
  - While existing functionality tests are the basis for the certification process, the new MobiDICK system adds new tests.
  - A stuck bit test is implemented to detect upset bits in the samples caused by failures in the front-end-digitizer boards. The test scans the amplitude, phase, and pedestal of each channel and displays the results in the GUI window.

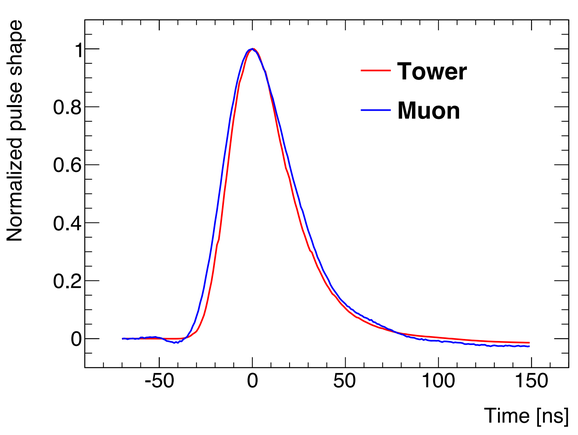


- Characterization of the ADC board(Trigger Signals Read Out)
  - The ADC board plays a key role in data analysis of the MobiDICK system to give a full certification to the performance of the super-drawer front-end.
  - Because of the nature of the newly added test, the new MobiDICK is reconstructing Amplitude, phase and pedestals. A flat Filtering method is implemented in the software to restore the injected charge and its responses. The comparison with an optimal filter is shown in the figure.
  - The Linearity of reconstructed energy as a function of different charges is very good for both flat and optimal filters
  - ADC channels responses at the same charge are overall uniform. Since the ADC system has two ADCs to digitize all the signals, there is an ignorable difference between the two ADCs at the level of 0.1%. The channels from number 0 to 7 are controlled by one ADC while the other ADC monitors the channels from number 8 to 15.
  - Both Flat Filter and Optimal Filter responses agree, where the Flat Filter response is the integral of the signal area while the Optimal Filter is an optimal technique for the pulse amplitude estimation.



  - Based on the Results, the Flat filter is compatible with other sophisticated algorithms like optimal filtering. Therefore, the implemented reconstruction algorithm presented good performance.
  - Difference between the ADCs can be improved by the correct calibration, leading to a better inter calibration.
- Precision test of analog signal from the super-drawer with the ADC board
  - Analog output of the super-drawer can be monitored with the system acting as a digital scope. Up to 128 samples can be stored at a time obtained with a sampling rate of 40 Msps.
  - From the pedestal measurements of the D6 cell, we observe a wider distribution in the D6-R PMT due to a noise pick-up.
  - Pulse shape measurement of the tower and Muon output of the super-drawer were performed by MobiDICK by sampling a charge at different injection times. As expected, the Muon outputs have a slightly wider pulse width, compatible with previous measurements.





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