The Associative Memory Boards for the FTK Processor at ATLAS

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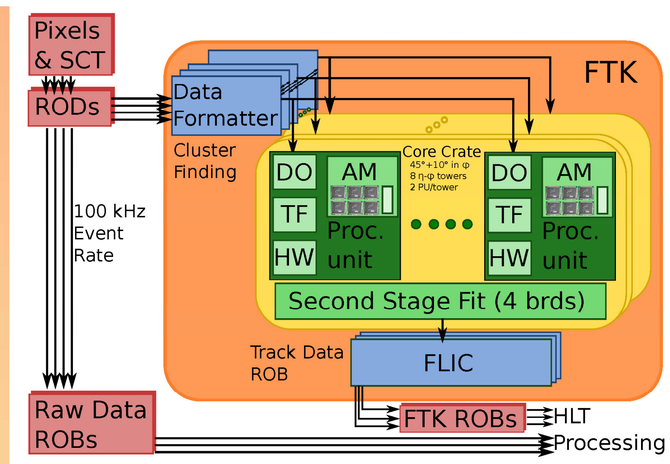
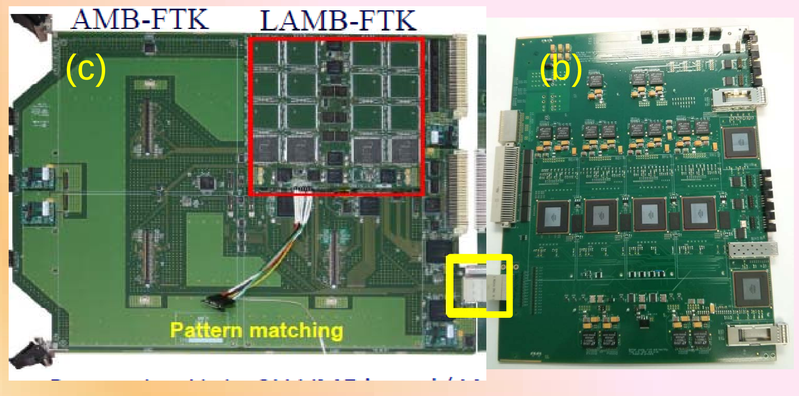
FTK and the Associative Memory (AM) System

FTK is an electronics system that rapidly finds and reconstructs high quality tracks in the inner-detector pixel and SCT layers for every event that passes the level-1 trigger. It operates in two stages: in the first stage, 8 of the 12 ATLAS Pixel and SCT layers are used to perform pattern recognition and do the initial track fitting. Pattern recognition is carried out by a dedicated system called the Associative Memory (AM); tracks from the first stage pass to the second stage where they are extrapolated into the 4 logical Pixel and SCT layers not used in stage 1



AM = Associative Memory System, DO = Data Organizer, FLIC = FTK-to-Level-2 Interface Crate, HW = Hit Warrior, ROB = ATLAS Read Out input Buffer, ROD = silicon detector Read Out Driver, TF = Track Fitter

The AM system consists of the Associative Memory chip, an ASIC designed by INFN and optimized for this particular application, and two types of boards, a 9U VME motherboard on which are mounted four mezzanines (LAMBs) that hold AMchips. Both the boards and the chip are under evolution, and only the two most recent versions will be presented here. The first version of the AMBFTK and LAMBFTK is shown to the right. They were developed and tested with the AMchip04, the first FTK chip provided of parallel I/O.

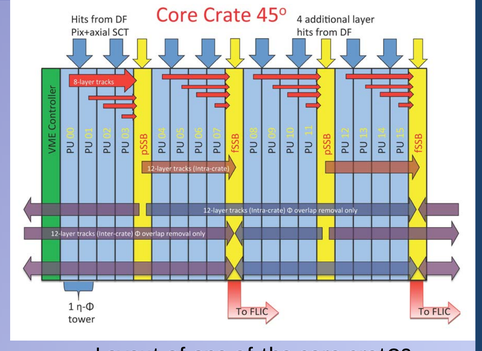


The first associative Memory System, composed of the VME 9U AMBFTK board (A) and four LAMBFTK mezzanines covering almost all the AMBFTK (one is shown in the photo). The picture also shows the the AUX card (B) that sits on the back of the VME crate and communicates with the AM through the high frequency connector P3 (yellow box). In between there is (not shown) the VME backplane

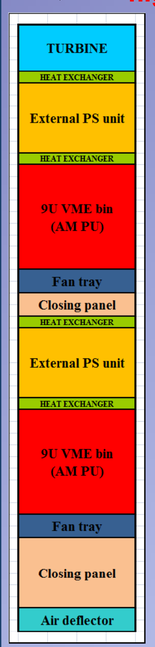
System layout and cooling tests

- Full system composed of:
  - 512 LAMBFTK boards
  - 128 AMBFTK boards
  - 8 VME 9U core crates
  - 4 racks with 2 crates each

16 AMBFTK boards/crate, high power consumption



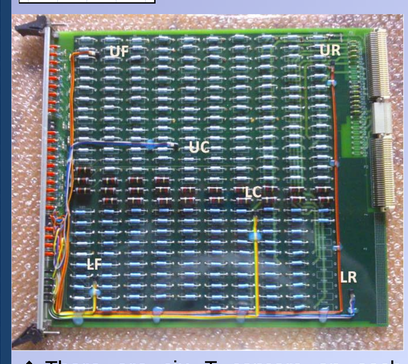
Layout of one of the core crates



✓ Proposed layout of one of the core racks
- Evaluated power consumption for the single core crate is at present about 7k Watts. An R&D effort is in progress in order to reduce the power consumption of the AMchip to 2 Watts and decrease the crate dissipation to 5k Watts
- Present baseline is one power supply for each crate, positioned in the rack outside the crate. Work is in progress to be able to supply two crates with the same power supply, which will be located in the middle of the two crates
- Each crate is equipped with its own fan tray unit to ensure the turbine air flow. More powerful fans are under test to optimize the air pressure inside the crate
- Heat exchangers on top of crates and power supplies are needed in order to avoid a significant increase of the environmental temperature of ATLAS electronics room

Cooling is a critical issue, so system tests were performed with a dedicated setup, and other tests are planned directly in the ATLAS electronics room USA15 in the next weeks

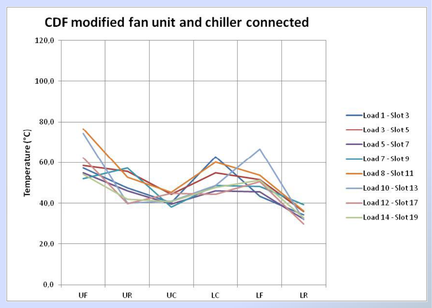
❖ The cooling test setup was installed in a lab outside ATLAS, and is shown in the picture below. It consists of a VME 9U crate, recovered from CDF, and mounted on a rack below a Wiener 6k Watts power supply (PS, with handles in the picture), a fan tray (WIENER or CDF modified), and a chiller (connected to the heat exchanger). The PS load is composed of 15 VME load boards equipped with resistors and T sensors. A measuring system reads both the PS currents and the load temperatures



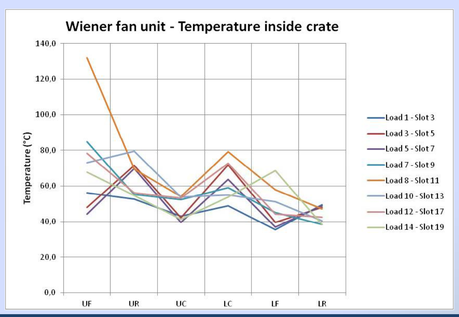
❖ There are six T sensors on each load board (pictured above), which are installed on 8 boards only. Their positions are denoted UF (upper front), UR (upper rear), UC (upper center), LC (lower center), LF (lower front) and LR (lower rear)

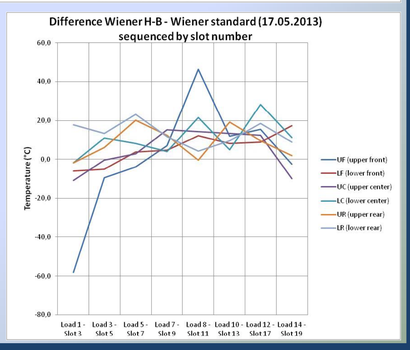
❖ Two different fan trays were used during the system tests outside ATLAS, one CDF and one WIENER standard. Both were modified to improve their cooling performance. One small fan was added to the CDF fan tray, in order to cover the central frontal region. One fan of the WIENER fan tray (the one to the left front) was replaced with a new type, the Hyper-blower, which is much more powerful.

❖ The plot to the right shows the measured performance of the modified CDF fan tray. The result is quite good, apart from the upper frontal region in two boards, on which there is a moderate temperature increase.
The last results of the WIENER modified fan tray are shown on the bottom plots. On average, the temperature is higher than in the CDF case for almost all regions, but where the new Hyper-blower was installed (loads 1 and 3) there is a significant improvement, also evident from the plot showing the difference between the modified fan tray and the standard one.



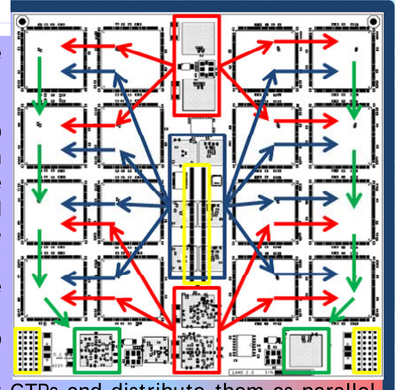
The next tests will use a fully modified WIENER fan tray, containing 9 Hyper-blowers.





LAMBFTK: why a new LAMBSLP is needed

❑ The LAMBFTK was designed to serve the 10 large and parallel I/O buses required by the AMchip04, a small chip (die of 12 mm^2) provided of all the FTK needed functionalities. LAMBFTK receives the buses through an SMD connector placed in the center of the LAMB, (yellow central rectangle in the figure to the right). It contains 32 AMchip04, 16 on the top side and 16 on the bottom side of the board. Their core voltage, 1.2 V, is provided through the large current (up to 25 A per LAMBFTK) connectors (yellow boxes at the bottom), while the I/O voltage, 3.3 V, is provided by the mezzanine central SMD connector. The 32 AM chips outputs are connected as eight 4-chip pipelines (4 on the top side and 4 on the bottom side of the mezzanine), and finally collected by the GLUE FPGAs (green boxes) containing high-speed GigaBit Transceiver (GTP) serial links that are used to transfer the AM outputs to the motherboard through the SMD connector.
❑ Hits for each event, arriving at the LAMBFTKs through the SMD connector, organized into 8 buses, are fed as parallel buses with low fan-out to the 32 AM chips.



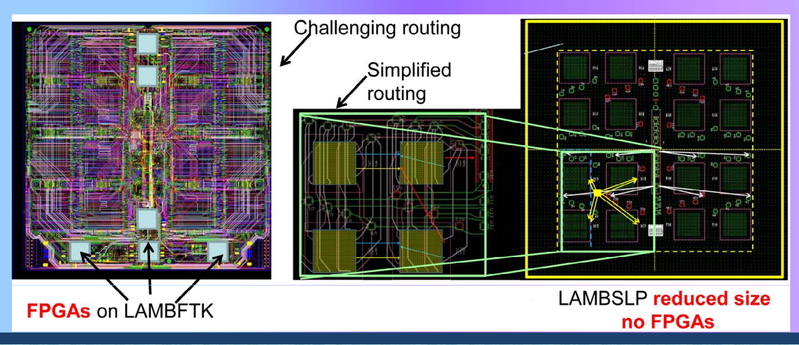
The FPGAs in the red boxes receive the buses serially from the motherboard using their GTPs and distribute them as parallel buses. The red arrows in the figure show how each bus is split four ways and distributed by the FPGAs while the blue arrows show the bus distribution by pairs of smaller CPLDs, able to fit the small remaining space, and receiving parallel buses from AMBFTK.
❑ The LAMBFTK was tested successfully in the lab together with the AMBFTK and the AMchip04, but the system was not adaptable with the following design of a large die AM (180 mm^2) that showed the necessity of a very large number of VCC and GND pads, not compatible with the PQ208 package used for the previous AM chips. To simplify the board design and increase the number of available pads, the new AM chip uses serialized I/O (22 pads instead of 160) and a new BGA package (BGA 23x23).

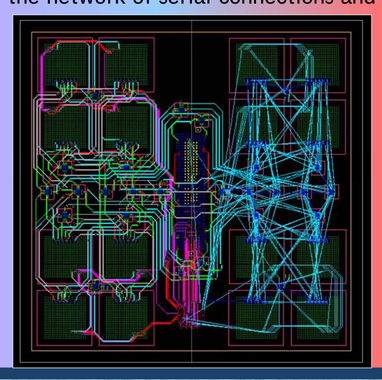
The LAMBSLP

❑ The LAMBFTK had a challenging layout, because of the presence of the parallel buses. Its layout, showing the degree of complexity, is visible in the bottom figure to the left . Moreover, it required many FPGAs for handling the input fan-out and the glue logic. In order to minimize the impact of these weaknesses on the system functionality, a new approach is under development, the LAMBSLP: the FPGAs are replaced by simple low-cost serial-links fan-out chips.

❑ This new mezzanine is designed to match the new AM chip needs. The absence of FPGAs, as shown in the central figure on the bottom, makes the layout design simpler and more compact. The new layout is visible in the bottom figure to the right.

❑ Final prototypes of this new mezzanine will be available in the next months. In the meanwhile we have a mini-asic AM chip provided of serialized I/O and a miniLAMB assembled with 4 mini-asics that we use to test the network of serial connections and the compatibility between the FPGAs, the new fan-out chips and the new AM chip I/Os.

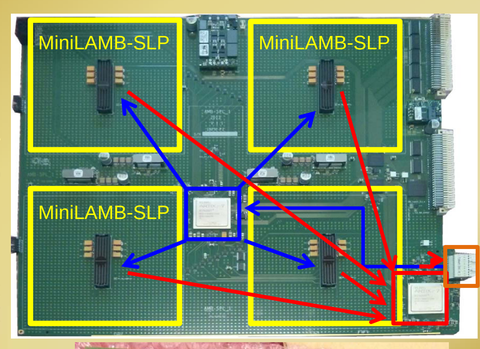




AMBSLP and the MiniLAMB

The AMBSLP design and tests

➢ The AMBSLP is the new 9U VME board on which 4 new LAMBSLPs will be mounted. The figure to the right shows the AMBSLP, highlighting the LAMBs (in yellow). A network of high speed serial links characterizes the bus distribution on the AMBSLP: 12 input serial links (in blue) that carry the ATLAS Pixel and SCT detector hits from the P3 connector (orange square) to the LAMBSLPs, and 16 output serial links (each red arrow represents 4 links) that carry the road numbers from the LAMSLPs to P3.



➢ The data rate is up to 2 Gb/s on each serial link. The control logic is placed inside a group of FPGA chips, visible in the figure. They are two large Xilinx Artix7 for data transfer and some Xilinx Spartan6 FPGAs for control and VME logic. The Artix7 have Low-Power GTPs. This ultra-fast data transmission requires specialized, dedicated on-chip circuitry and differential I/O for coping with the signal integrity issues. Since the LAMBSLP has a reduced size with respect to the LAMBFTK, all the necessary DC-DC converters can be placed in the central region of the motherboard, recovering the standard 9U shape for the AMBFTK, a clear advantage for chip cooling. In addition, a new high-density and high-frequency connector is used to provide both signals and all the necessary voltages to the LAMBSLP.

➢ Prototypes are available and passed the first tests in the lab. An AMBSLP and the MiniLAMB mezzanine are shown in the pictures to the right. On the MiniLAMB, the 4 small mini-asics placed inside QFN64 packages are visible in the lower right corner, since they are too small to use the final BGA package. In the center of this mini-asic group, the low-jitter oscillator and the fan-out chip that distributes the 100 MHz clock to the mini-asics are also visible. Above the group there are the fan-out chips for the hit serialized buses distribution. Two FPGAs are on the board, one to program the AM chips, the other for test purposes.

➢ The Serial links were tested. They are transmitted correctly to the miniLAMB, correctly received by the FPGA on the board and correctly transmitted to the mini-asics through the fan-out. Next step will be the test of the small AM bank (128 patterns) inside the mini-asics.