The Associative Memory Boards for the FTK Processor at ATLAS

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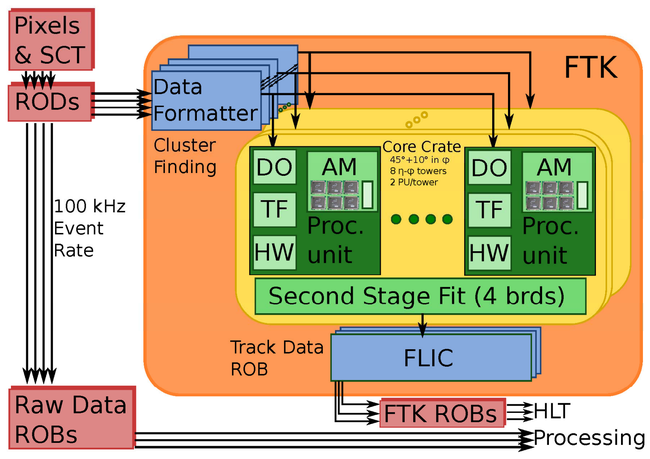
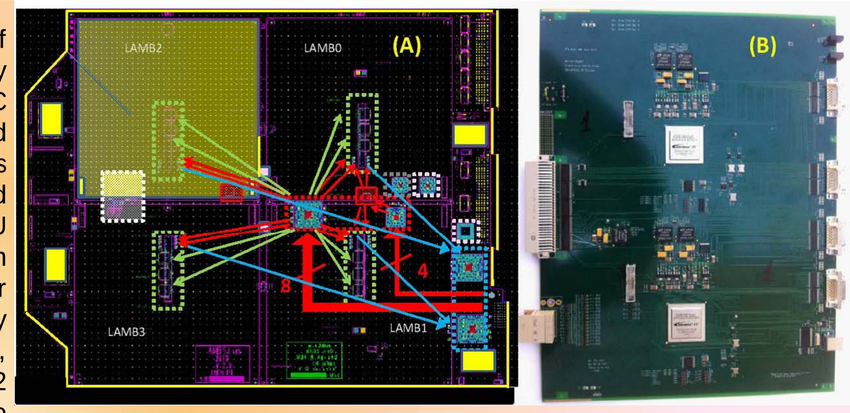
FTK and the Associative Memory (AM) System

FTK is an electronics system that rapidly finds and reconstructs high quality tracks in the inner-detector pixel and SCT layers for every event that passes the level-1 trigger. It operates in two stages: in the first stage, 8 of the 12 ATLAS Pixel and SCT layers are used to perform pattern recognition and do the initial track fitting. Pattern recognition is carried out by a dedicated system called the Associative Memory (AM); tracks from the first stage pass to the second stage where they are extrapolated into the 4 logical Pixel and SCT layers not used in stage 1



AM = Associative Memory System, DO = Data Organizer, FLIC = FTK-to-Level-2 Interface Crate, HW = Hit Warrior, ROB = ATLAS Read Out input Buffer, ROD = silicon detector Read Out Driver, TF = Track Fitter

The AM system consists of the Associative Memory chip (AMchip04), an ASIC designed by INFN and optimized for this particular application, and two types of boards, a 9U VME board (AMBFTK) on which are mounted four local associative memory boards (LAMBFTK), mezzanines that holds 32 AMchips each. Both the boards and the chip are under evolution, and only the two most recent versions will be presented here.

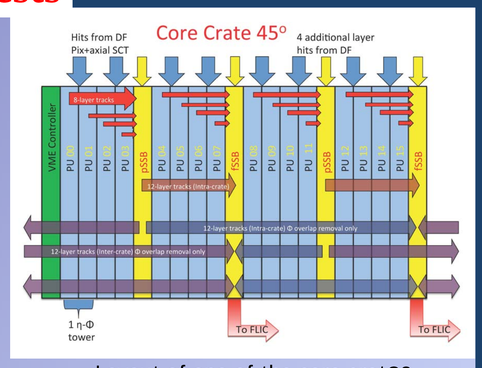


The associative Memory System, composed of the VME 9U AMBFTK board (A), and of four LAMBFTK mezzanines covering almost all the AMBFTK (one is depicted in yellow). The picture also shows the data paths to (blue) and from (red) the AUX card (B) , that sits on the back of the VME crate. In between there is (not shown) the VME backplane

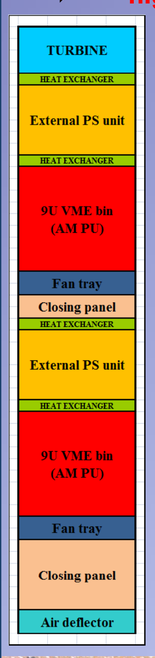
System layout and cooling tests

- Full system composed of:
  - 512 LAMBFTK boards
  - 128 AMBFTK boards
  - 8 VME 9U core crates
  - 4 racks with 2 crates each

16 AMBFTK boards/crate, high power consumption



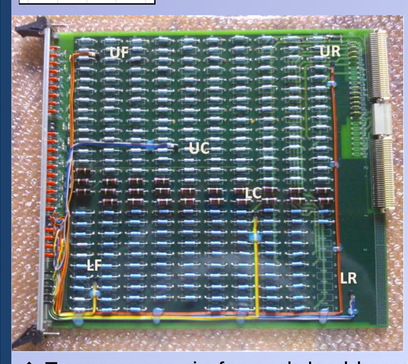
Layout of one of the core crates

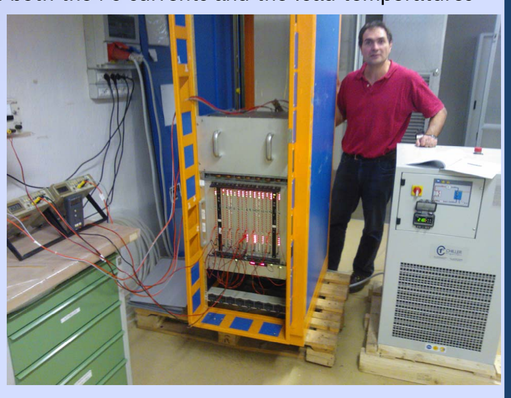


✓ Proposed layout of one of the core racks
- Evaluated power consumption for the single core crate is at present about 5k Watts. An R&D effort is in progress in order to reduce the power consumption of the AMchip to 2 Watts and decrease the crate dissipation to 5k Watts
- Present baseline is one power supply for each crate, positioned on rack outside the crate. Work is in progress to be able to supply two crates with the same power supply, which will be located in the middle of the two crates
- Each crate is equipped with its own fan tray unit to enforce the turbine air flow. More powerful fans are under test to optimize the air pressure inside the crate
- Heat exchangers on top of crates and power supplies are needed in order to avoid a significant increase of the environmental temperature of USA15

Cooling is a critical issue, so system tests were performed with a dedicated setup, and other tests are planned directly in the ATLAS electronics room USA15 in the next weeks

❖ The cooling test setup was installed in a lab outside ATLAS, and is shown in the picture below. It consists of a VME 9U crate, recovered from CDF, and mounted on a rack below a Wiener 5k Watts power supply (PS, with handles in the picture), of a fan tray (WIENER or CDF modified), and of a chiller (connected to the heat exchanger). The PS load is composed of 15 VME load boards equipped with resistors and T sensors. A measuring system reads both the PS currents and the load temperatures

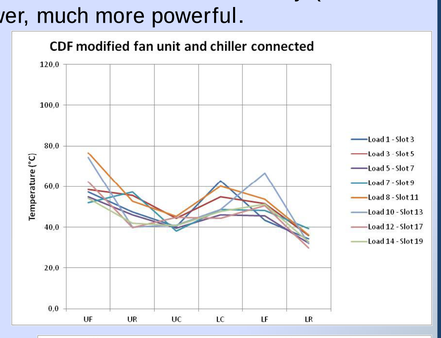




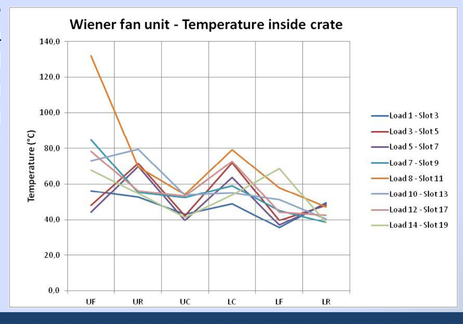
❖ T sensors are six for each load board (picture on top), and are installed on 8 boards only. Their positions are shown in the picture to the right, called UF (upper front), UR (upper rear), UC (upper center), LC (lower center), LF (lower front) and LR (lower rear)

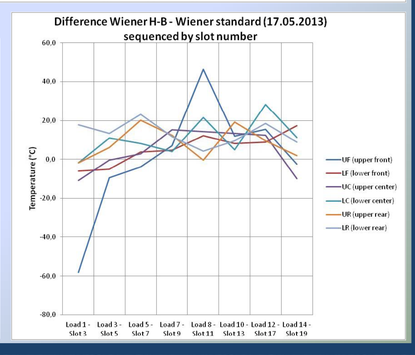
❖ Two different fan trays were used during the system tests outside ATLAS, one CDF ad one WIENER standard. Both were modified to improve their cooling performance. One small fan was added to the CDF fan tray, in order to cover the central frontal region. One fan of the WIENER fan tray (the one to the left front) was replaced with a new type, the Hyper-blower, much more powerful.

❖ The plot to the right shows the measured performance of the modified CDF fan tray. The result is quite good, apart from the upper frontal region in two boards, on which there is a moderate temperature increase.
The last results of the WIENER modified fan tray are shown on the bottom plots. On average, the temperature is higher than in the CDF case for almost all regions, but where the new Hyper-blower was installed (loads 1 and 3) there is a significant improvement, also evident from the plot showing the difference between the modified fan tray and the standard one.



Next tests should use a fully modified WIENER fan tray, containing 9 Hyper-blowers





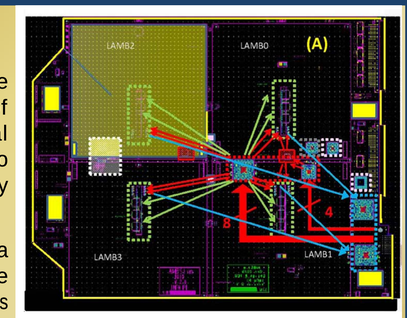
AMBFTK and AMBSLP

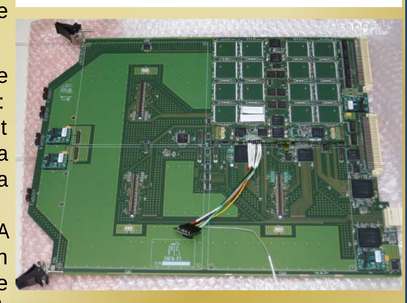
The AMBFTK design and tests

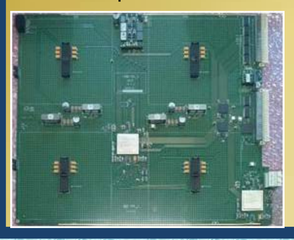
➢ The AMBFTK is a 9U VME board on which 4 LAMBFTKs are mounted. The figure to the right shows the AMBFTK layout, highlighting one of the LAMBs (in yellow). A network of high speed serial links characterizes the bus distribution on the AMBFTK: 12 input serial links (in red) that carry the ATLAS Pixel and SCT detector hits from the P3 connector to the LAMBFTKs, and 16 output serial links (each blue arrow represents 4 links) that carry the road numbers from the LAMBFTKs to P3

➢ The data rate is up to 2 Gb/s on each serial link. The control logic is placed inside a group of FPGA chips, visible in the figure. They are Xilinx Spartan6 FPGAs which have Low-Power Gigabit Transceivers (GTPs). This ultra-fast data transmission requires specialized, dedicated on-chip circuitry and differential I/O capable of coping with the signal integrity issues

➢ Prototypes are available and were extensively tested in lab. An AMBFTK with one LAMBFTK mezzanine is shown in the picture to the right. Two main tests were performed:
- Serial links. The test measured the Bit Error Rate (BER), using Pseudo Random Bit Sequence (PRBS). In the transmitter, a PRBS is selected and the receiver controls a signal that is asserted when there is an error detection in the links incrementing a counter. The measured BER was less than 10^{-10}
- Pattern-matching. This test validates the entire functionality of the AM system. A simulated pattern bank has been generated and loaded into each chip. With an iterative JTAG procedure, each pattern correct writing is checked. Then an input file with random hits is generated and loaded in memories. The simulated pattern bank was compared to the matched output roads generated by the on-board AMs, the result was 1 pattern error over 1k events







The evolution of the AMBFTK: the AMBSLP

➢ Recently, a new approach on the data distribution strategy for the AM system has been adopted, totally based on GTPs. The new system, called Serial Link Processor (SLP), uses a high number of serial link buses at 2Gpbs bandwidth. A Xilinx Artix 7 FPGA receives the 12 input data buses and distributes them to the upper part ad lower part of the board.
The first prototype of this new board is shown to the left. It is currently under test in the lab

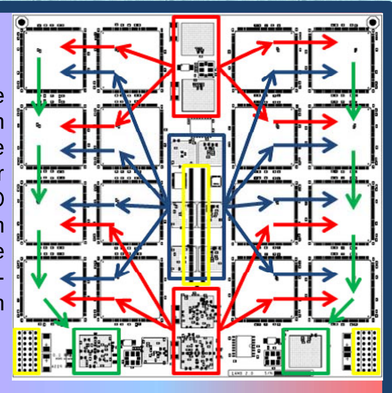
LAMBFTK and LAMBSLP

The LAMBFTK design and tests

❑ The LAMBFTK and the AMBFTK communicate through an SMD connector placed in the center of the LAMB, inside the yellow central rectangle in the figure to the right. Each LAMBFTK contains 32 AMchip04, 16 on the component side and 16 on the solder side of the board. Their core voltage, 1.2 V, is provided through the large current (up to 25 A per LAMBFTK) connectors in the yellow boxes at the bottom of the figure, while the I/O voltage, 3.3 V, is provided by the mezzanine central SMD connector. The 32 AM chips in each LAMBFTK are connected as eight 4-chip pipelines (4 on the top side and 4 on the bottom side of the mezzanine). The GLUE chips are Xilinx Spartan6 FPGAs containing high-speed GTP serial links that are partially used to transfer roads to the motherboard through the SMD connector

❑ The hits for each event, organized into 8 buses, arrive at the LAMBFTKs from the AMBFTK through the SMD connector and are fed partially in parallel, partially serially, using the GTPs. The mixed nature of this data transfer (half serial, half parallel) is due to the AMchip04 not having serial I/O. The red arrows in the figure show how each bus is split four ways and distributed by the Spartan FPGAs while the blue arrows show the bus distribution by a pair of CPLDs

❑ The LAMBFTK, shown in the picture to the right, was tested in lab together with the AMBFTK. See above for the procedures and results of the tests



The LAMBSLP

❑ The LAMBFTK has a critical layout, because of the presence of the parallel buses. Its layout, showing the degree of complexity, is visible in the bottom figure to the left . Moreover, it requires many FPGAs for handling the input fan-out and the glue logic. In order to minimize the impact of these weaknesses on the system functionality, a new approach is under development, the LAMBSLP

❑ This new mezzanine is designed to match the AMBSLP board. The absence of FPGAs, as shown in the central figure on the bottom, makes the layout design simpler and more compact. The new layout is visible in the bottom figure to the right

❑ Prototypes of this new mezzanine will be available in the next months, and tests with the AMBSLP are planned to start just after