Status of the NA62 liquid krypton electromagnetic calorimeter Level 0 trigger processor

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Status of the NA62 liquid krypton electromagnetic calorimeter Level 0 trigger processor

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ABSTRACT: The NA62 experiment at the CERN SPS aims to measure the Branching Ratio of the very rare kaon decay $K^+ \to \pi^+ \nu\bar{\nu}$ collecting $O(100)$ events with a 10% background in two years of data taking. To reject the $K^+ \to \pi^+\pi^0$ background the NA48 liquid krypton calorimeter will be used in the 1-10 mrad angular region. The status of the Liquid Krypton Electromagnetic Calorimeter Level 0 Trigger is presented.

KEYWORDS: Trigger concepts and systems (hardware and software); Digital electronic circuits

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1 The NA62 experiment at CERN SPS

The NA62 experiment [1] aims at measuring the very rare kaon decay $K^+ \to \pi^+ \nu\bar{\nu}$ collecting $O(100)$ events with a 10% background in two years of data taking.

$K^+ \to \pi^+ \nu\bar{\nu}$ is an exceptionally clean decay from the theoretical point of view with a Standard Model branching ratio prediction of $\mathrm{BR}(K^+ \to \pi^+ \nu\bar{\nu}) = (8.5 \pm 0.7) \times 10^{-11}$. A precise measurement of $\mathrm{BR}(K^+ \to \pi^+ \nu\bar{\nu})$ will offer the opportunities of testing the Standard Model and deepening the knowledge of the CKM matrix.

The NA62 detector [2], see figure 1, currently being installed at the SPS North Area High Intensity Facility is composed of: a differential Cerenkov counter (CEDAR), a beam tracker (GTK) and charged particle detector (CHANTI), a straw chambers magnetic spectrometer, a photon veto system composed of different detectors in the various angular decay regions, a RICH, a charged particle hodoscope (CHOD) and a muon detector (MUV).

2 Trigger and data acquisition system

In order to extract few interesting decays from a very intense flux a complex and performing three level trigger and data acquisition system was designed [3].

The Level 0 trigger algorithm is based on few sub-detectors (the charged hodoscope, the muon detector and the liquid krypton electromagnetic calorimeter) and is performed by dedicated custom hardware modules, with a maximum output rate of 1 MHz and a maximum latency of 1 ms.

Level 1 and Level 2 software triggers are executed on dedicated PCs.

The Level 1 trigger is based on information computed independently by each sub-detector, with a maximum output rate of 100 kHz and a maximum latency of 1 s.

The Level 2 trigger is based on assembled and (partially) reconstructed events, in which complex correlations between information from different sub-detectors are possible, with a maximum output rate around 15 kHz and a maximum latency corresponding to the SPS spill period.

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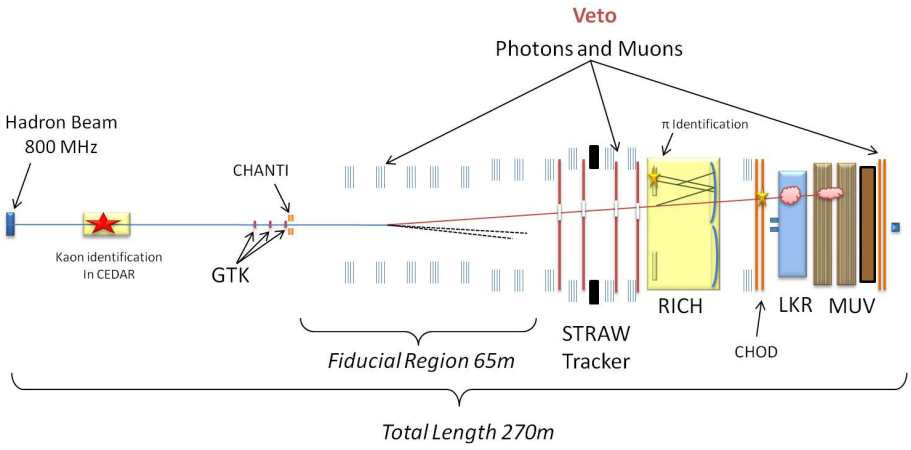

Figure 1. Schematic drawing of the NA62 detector at CERN SPS.

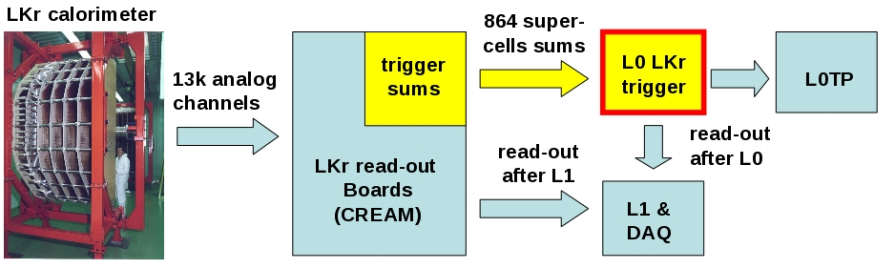

Figure 2. Block diagram of the Liquid Krypton Level 0 trigger inside the Trigger and Data Acquisition system.

3 The liquid krypton electromagnetic calorimeter

In order to suppress the background from $K^+ \to \pi^+\pi^0$ decay an efficient photon veto system is foreseen. In the 1-10 mrad angular region the NA48 electromagnetic calorimeter is used [4].

This calorimeter is a quasi-homogeneous ionization device using liquid krypton as active medium and characterized by excellent time and energy resolution.

The Liquid Krypton calorimeter will be readout by the new Calorimeter REAdout Modules [5] (CREAMs) which will provide 40 MHz 14 bit sampling for all 13248 calorimeter readout channels, data buffering, optional zero suppression and programmable trigger sums for the Level 0 electromagnetic calorimeter trigger processor.

4 The liquid krypton Level 0 trigger

The Level 0 Liquid Krypton electromagnetic calorimeter trigger, see figure 2, identifies electromagnetic clusters in the calorimeter and prepares a time-ordered list of reconstructed clusters together with the arrival time, position, and energy measurements of each cluster. Information on reconstructed clusters is used by the Level 0 Trigger Processor to veto decays with more than one cluster in the Liquid Krypton calorimeter.

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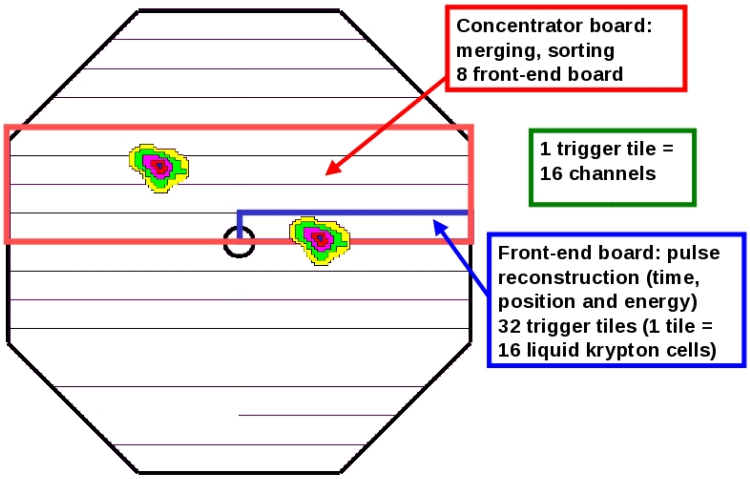

Figure 3. Liquid Krypton electromagnetic calorimeter trigger segmentation.

The trigger processor also provides a coarse-grained readout of the Liquid Krypton calorimeter that can be used in software triggers and off-line as a cross-check for the CREAM high-granularity readout.

4.1 Trigger algorithm

Trigger algorithm is based on energy deposits in tiles of 16 calorimeter cells which are available from the main readout boards.

Electromagnetic cluster search is executed in two steps with two one-dimensional (1D) algorithms, see figure 3.

From the trigger point of view the calorimeter is divided in slices parallel to the horizontal axis. In the first step peaks in space and time are searched independently in each slice with a 1D algorithm. In the second step different peaks which are close in time and space are merged and assigned to the same electromagnetic cluster.

4.2 Trigger processor implementation

The main parameters driving the design of the processor are the high expected instantaneous hit rate (30 MHz), the required single cluster time resolution (1.5 ns) and a maximum allowed latency of 100 μs from detector hit generation to trigger primitives output to the L0 trigger processor.

The processor is a three-layer parallel system, composed of Front-End and Concentrator boards, both based on the 9U TEL62 cards [6] equipped with custom dedicated mezzanines, see figure 4.

The Liquid Krypton Level 0 trigger continuously receives from the Liquid Krypton readout modules 864 trigger sums each one corresponding to a tile of 16 calorimeter cells.

Each **Front-End board** receives 32 trigger sums and performs peak search in space and computes time, position and energy for each detected peak. In order to extract timing information at the ns level a parabolic interpolation in time around sample maximum and a digital constant fraction discrimination are performed after the peak search algorithms. Information on reconstructed peaks is transferred from the Front-End boards to the Concentrator boards on low-latency high-bandwidth

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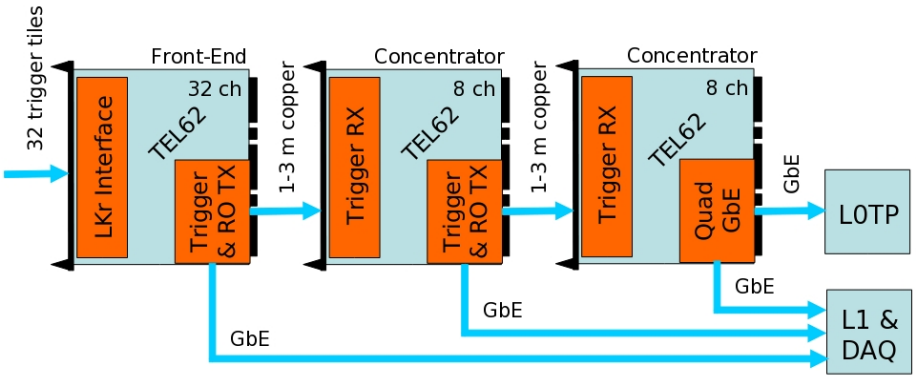

Figure 4. Liquid Krypton trigger processor block diagram. 28 Front-End boards and 8 Concentrator boards are foreseen in the system.

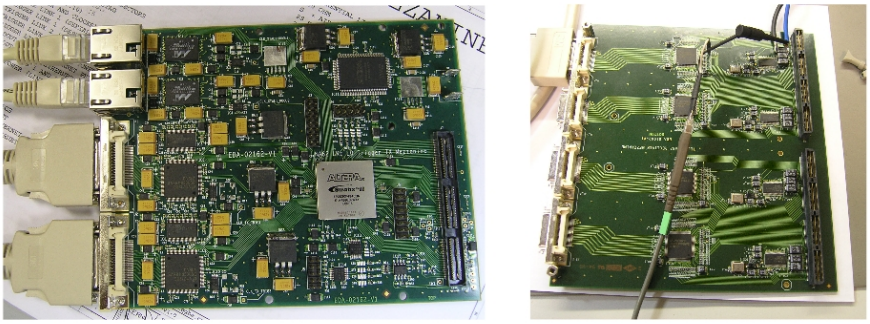

Figure 5. Trigger and Readout TX (left) and Trigger RX (right) mezzanine card prototypes.

dedicated trigger links. Raw data received by the readout modules are also stored in latency memories, to be readout upon request. 28 Front-End boards equipped with 84 custom mezzanines are foreseen in the whole system.

The **Concentrator board** receives trigger data from up to 8 FE boards and combines peaks detected by different front-end boards into a single cluster. Overlap between neighboring Concentrators is foreseen to guarantee that each cluster will be fully contained in at least one Concentrator board with proper logic to avoid double counting. Reconstructed clusters are also stored in latency memories, to be readout upon request. 8 Concentrator boards equipped with 24 custom mezzanines are foreseen in the whole system.

Data transmission from the CREAM main digitizer boards to the trigger processor is performed over standard Ethernet cables (Cat.6, length up to 15 m) with an effective data rate per lane of up to 720 Mbps (640 Mbps payload). Data is transmitted using standard embedded clock serdes chips (e.g. DS92LV16). High-speed differential cable extender buffers (DS15BA101/DS15EA101) optimized for high speed serial transmission over 100 Ohm differential cables will be used.

High speed low latency trigger data transmission from the Front-End to the Concentrator boards is performed by dedicated mezzanines (Trigger and Readout TX mezzanine and Trigger RX mezzanines, see figure 4 and 5).

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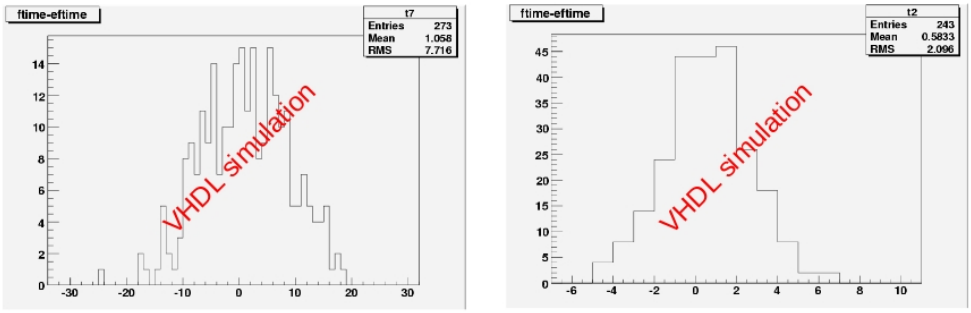

Figure 6. Digital VHDL simulations results. With 40 MHz sampling, 100 ps/bin, 1/40 of a full scale pulse with noise and time jitter added the time resolution is 750 ps RMS.

The Trigger and Readout TX mezzanines transmit up to 4.8 Gbps (48 bits at 100 MHz) over halogen-free individually shielded twisted pairs using the DS90CR485 serializer. The Trigger RX mezzanines receive and deserialize data using the DS90CR486 deserializer.

Readout data is transmitted over two standard gigabit Ethernet cables using an Altera IP MAC core together with an external PHY.

4.3 Simulations and tests

A preliminary version of the peak reconstruction algorithm was simulated and implemented on an ALTERA Stratix I FPGA [7]. With 12-bit pulse height resolution a preliminary version of the algorithm can process one sample at a rate in excess of 80 MHz, corresponding to 62.5 ns to process one peak (5 samples). The maximum acceptable peak rate in a single FPGA is thus 16 MHz for this model of FPGA. Much more powerful devices (ALTERA Stratix III) will be mounted on the TEL62.

Digital VHDL simulations were performed using the following pulse shape

$$f(t) = A[1 + \sin(2\pi t/T - 3\pi/2)]$$

with $T = 175$ ns to check the algorithm, obtaining satisfactory theoretical performances, see figure 6. A more sophisticated algorithm will be implemented for data-taking.

The possibility of using an FPGA embedded processor (Altera Nios II) for the peak reconstruction algorithm is currently under study.

Given the relatively large number of TEL62 used in the trigger processor and the complexity of the board itself (each TEL62 will mount 5 large FPGAs) testing is a very relevant issue. In order to check the TEL62 assembly a JTAG Boundary Scan test was developed, see figure 7, using a commercial JTAG test program [8] and commercial ad hoc JTAG hardware modules [9] for on-board DDR2 testing. With the developed Boundary Scan test program more than 90% of the on-board connections will be tested including the on-board DDR2 lines.

5 Conclusions

A fast parallel processor for cluster reconstruction and counting in the Liquid Krypton electromagnetic calorimeter of the NA62 experiment has been designed.

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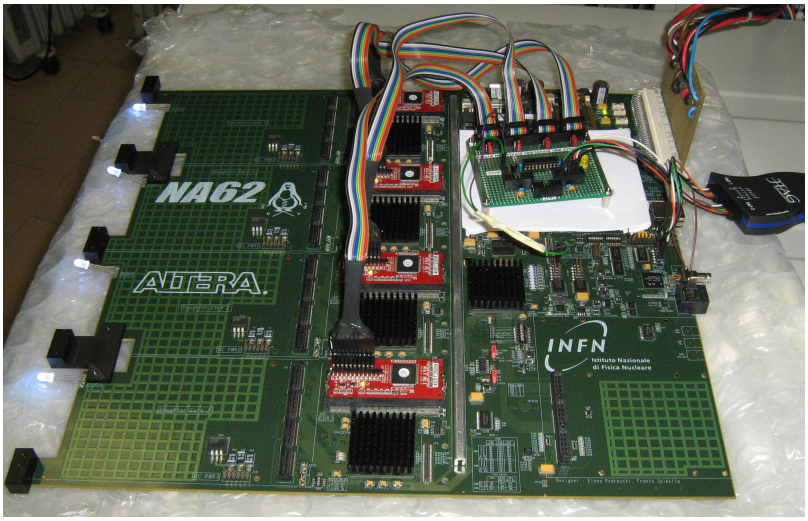

Figure 7. The TEL62 JTAG test stand with the DDR2 JTAG test modules (in red).

In total, the system will be composed of 36 TEL62 boards, 108 mezzanine cards and 215 high-performance FPGAs. The whole system will fit in three 9U crates.

Most of the boards and mezzanines have been designed and are currently being tested. Testing and board production will last for 2013 and part of 2014. The system will be commissioned in the last part of 2014, ready for data taking at the end of 2014, beginning of 2015.

References

[1] NA62 collaboration, *Proposal to Measure the Rare Decay $K^+ \to \pi^+ \nu\bar{\nu}$ at the CERN SPS*, CERN-SPSC-2005-013.

[2] NA62 collaboration, *NA62 Technical Design*, NA62-10-07 (2010).

[3] M. Sozzi, *A concept for the NA62 Trigger and Data Acquisition*, NA62-07-03 (2007).

[4] NA48 collaboration, V. Fanti et al., *The Beam and detector for the NA48 neutral kaon CP-violations experiment at CERN*, *Nucl. Instrum. Meth.* **A 574** (2007) 433.

[5] V. Ryjov et al., *The NA62 Liquid Krypton Calorimeter Readout Module*, in *Proc. of TWEPP 2011*.

[6] E. Pedreschi et al., *Firmware approach for TEL62 trigger and data acquisition board*, 2012 *JINST* **7** C02046.

[7] http://www.altera.com.

[8] http://www.jtag.com.

[9] http://www.start-test.com.

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