Design of a Hardware Track Finder (Fast Tracker) for the ATLAS Trigger

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Marie Curie IOF Project 254410 - ARTLHCFE

INFN Frascati

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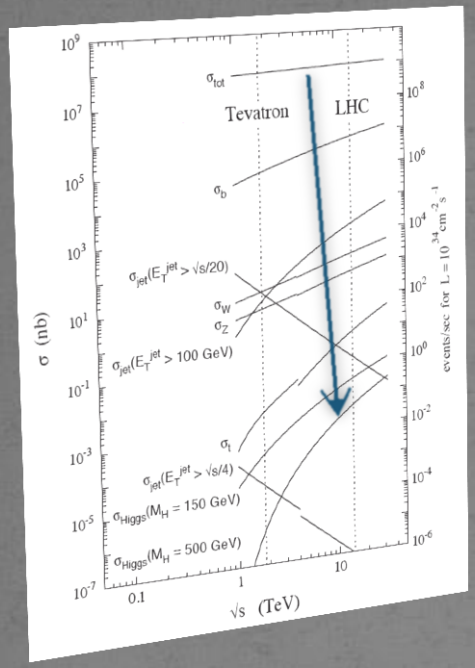
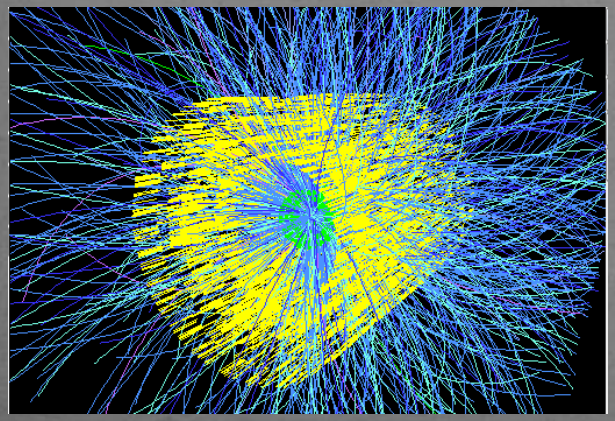
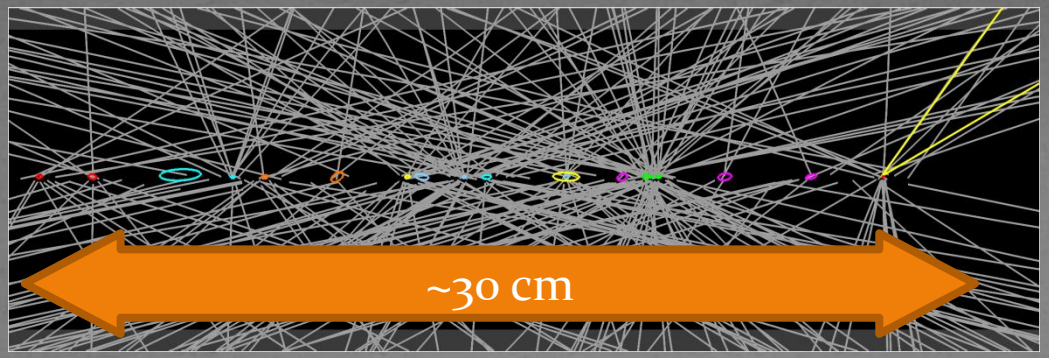
The Motivation and the Challenge



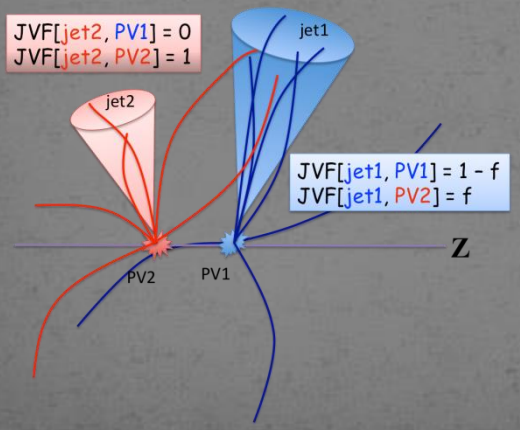


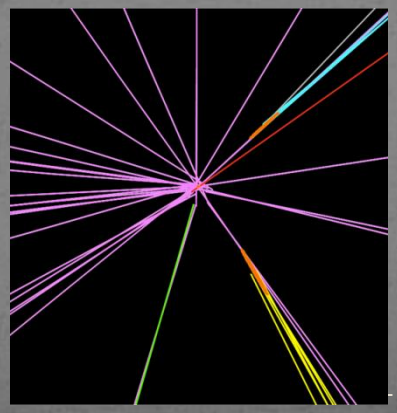
- Higgs discovery confirmed the SM model once more
- The picture is still incomplete and more measurements will challenge it
  - New precision tests require much higher luminosity
  - Energy increase to 13 TeV may open new scenarios
- Focus on very rare and energetic channels
- Maintain high trigger efficiency on challenging final states is crucial
- Selections complicated by the presence of a large number of pileup events
  - LHC expects between 40-80 multiple interactions (pileup) 2015-2018
  - Full tracking is a powerful tool to limit its effect

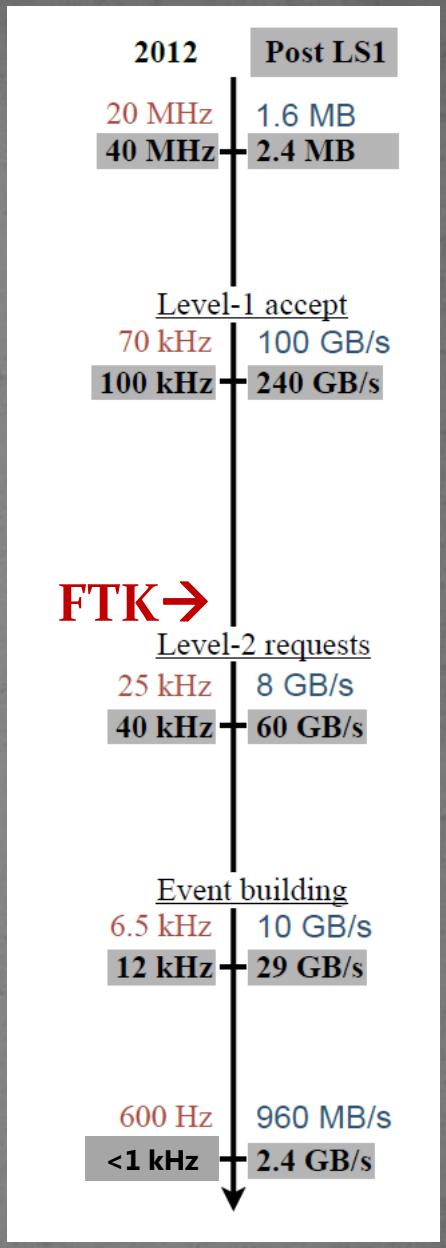


Tracking detector can provide powerful information like the number of primary vertexes.
Can help in correcting the calorimetric measurements or be fundamental to identify specific topologies, as b- or τ-jets.

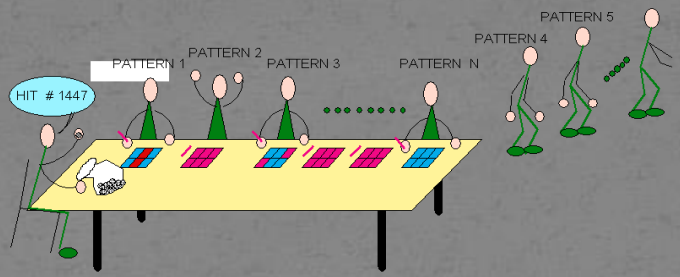
The Fast TracKer (**FTK**) will perform a complete tracking in time for the level-2: 100 KHz with a latency <100 μs.

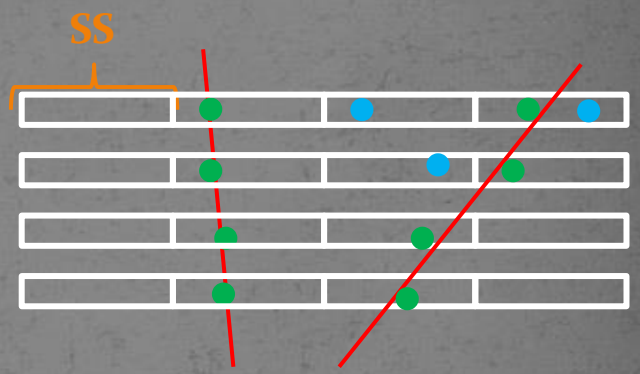




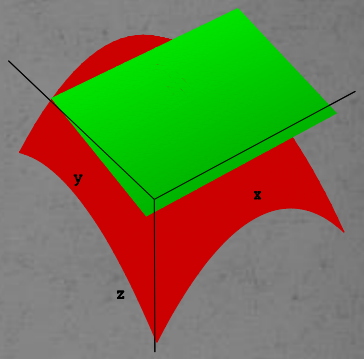


The FTK basic ideas



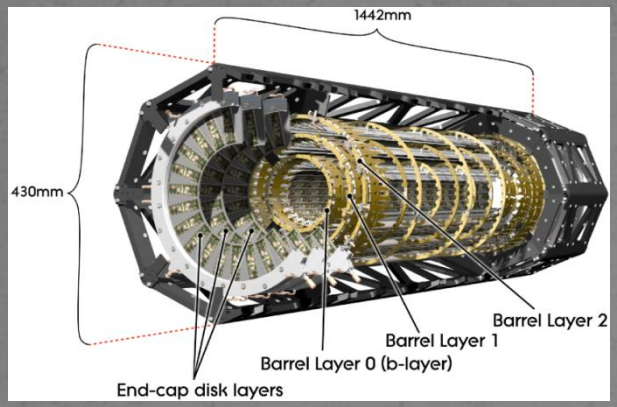


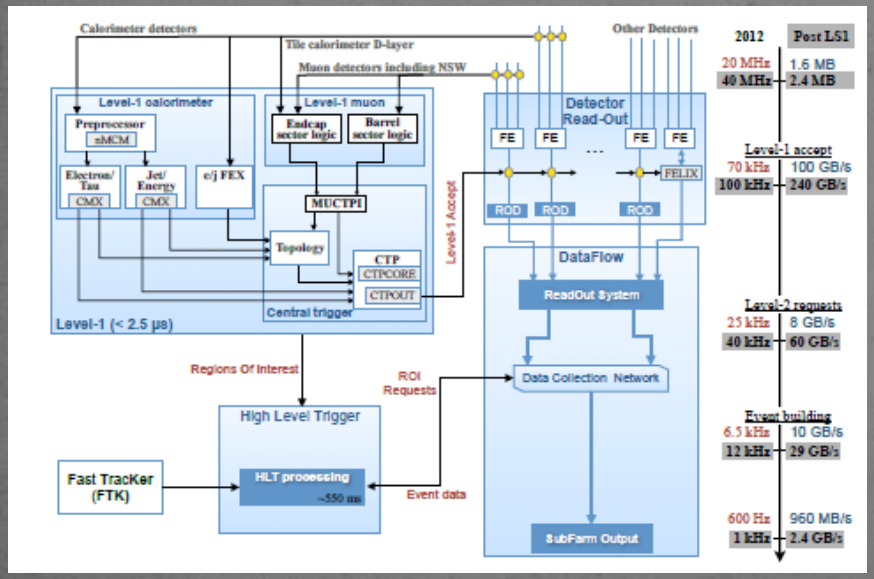
- FTK algorithms designed to be simple and highly parallel
- Tracking divided into two sequential steps
- The pattern matching comparing the hits with calculated patterns at course resolution and special hardware
  - Hits are grouped in super-strips (SS) with coarse resolution
  - Limited resolution reduces the number of pre-computed patterns
- The track's parameters are evaluated from the full resolution hits using a linear Principal Component Analysis algorithm (j.nima.2003.11.078)



$$p_i = \sum_j C_{ij} \cdot x_j + q_i$$

Integrating FTK in ATLAS

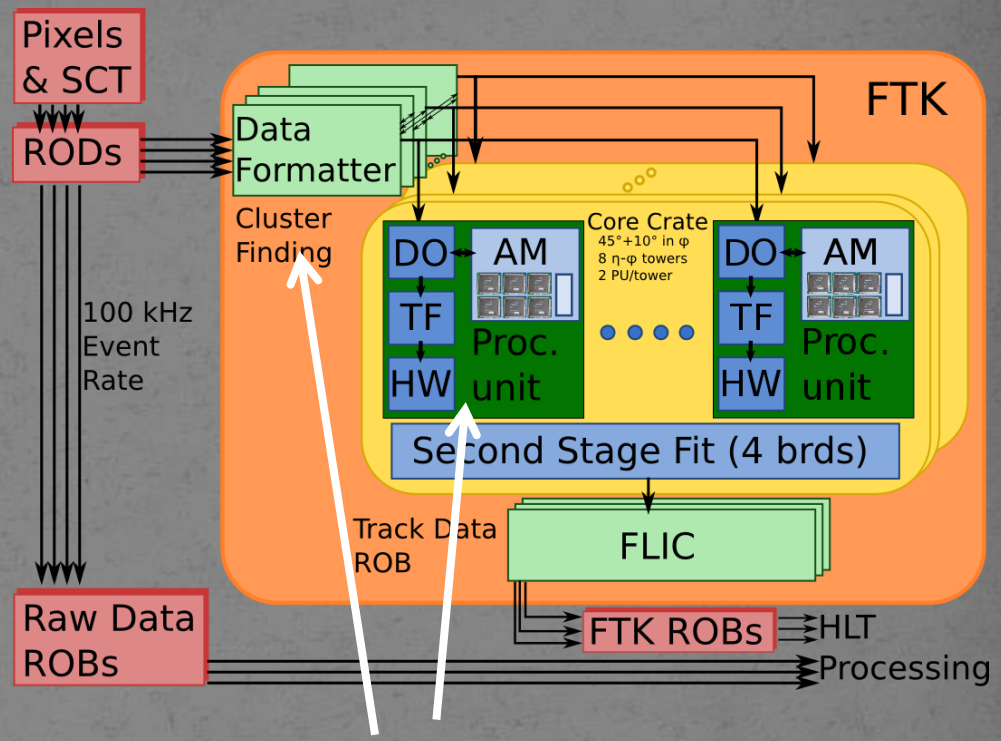




- The ATLAS inner detector is composed by 4 pixel layers and 4 strip pairs (12 layers)
  - Not originally designed for real-time tracking
- FTK will receive data from the whole ATLAS inner detector after each Level-1 trigger
- Pattern matching performed looking for segments with hits in 8 layers
- Track fitting performed in 2 stages
  - 1st stage confirms the road
  - 2nd stage extends the track to improve the quality and reduce the fakes

FTK architecture overview

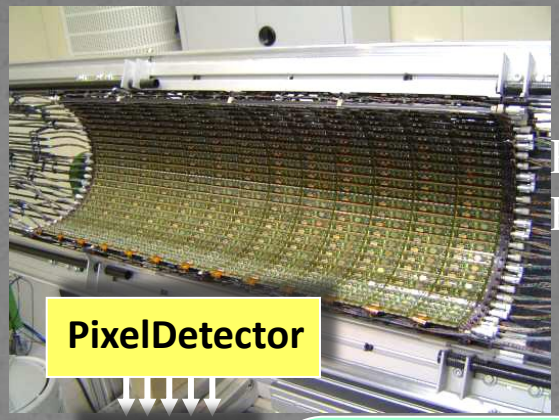
- The system receives a copy the data from the RODs
- The Data Formatter (DF) performs a first data reduction and organizes the data in 64 overlapping η-ϕ towers
- DF provides data for pattern matching to the Processing Units (PU)
  - 1st track fitting stage removes random coincidences
- The 2nd stage board (SSB) combines 1st candidates with additional hits
  - Refines the fit: improve quality and reduce fakes
- Final candidates using up to 12 layers are filtered and reformatted by the "FTK Level-2 Interface Crate" (FLIC)



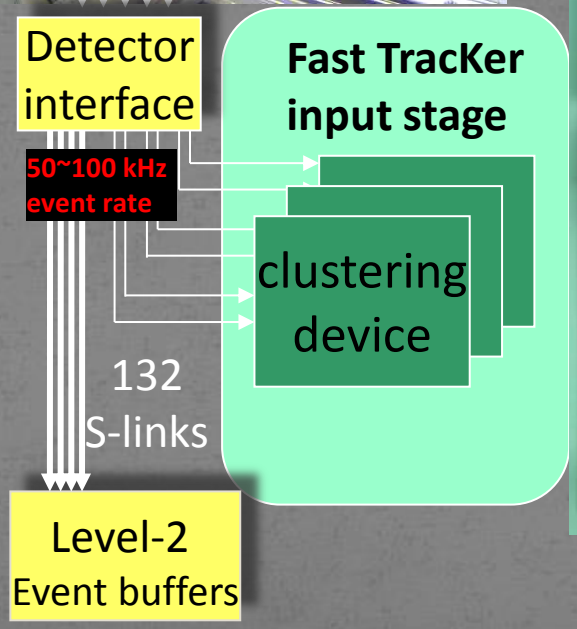
This talk will focus on the clustering "input mezzanine" (FTK_IM) in the DF and the processing unit (PU)

2D-Clustering for the ATLAS FastTracKer Processor

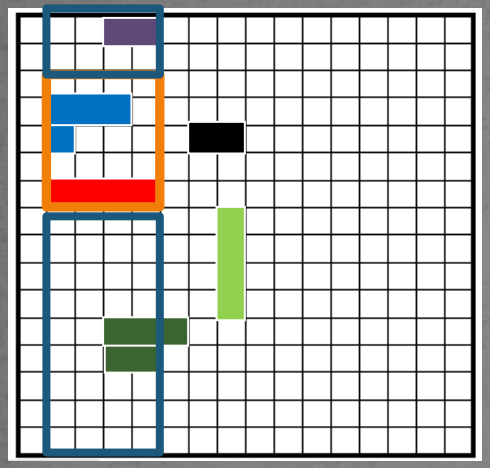
- The is installed on the "data formatter" (DF) boards
- Performs a fundamental data reduction for the system
- Main challenge: input rate 308 Gbits
  - 256 S-link fibers from all pixel RODs
    - Running at 1.2 Gbits
    - 32bit words at 40MHz, 1 hit/word
- SCT data partially clustered by the font-end



FTK Input Mezzanine Board

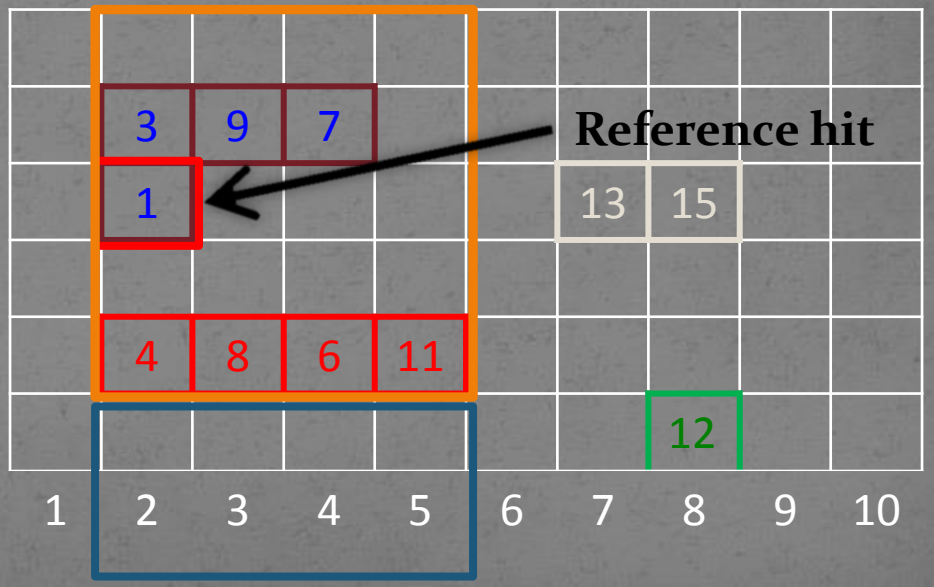


Grid Clustering – Generate Window



- Generate a cluster window (e.g. 4x5 pixels) around a reference hit
- The reference hit is located on the **middle row** of the window and
  - **Column 1** of the window if it belongs to an **odd** column
  - **Column 0** of the window if it belongs to an **even** column

- Pixel hits are read from the front-end in columns
- Hits are read from the input until a hit which belongs to a column beyond the cluster window is identified
- The hits that belong to the same columns as the cluster window are stored in a separate circular buffer



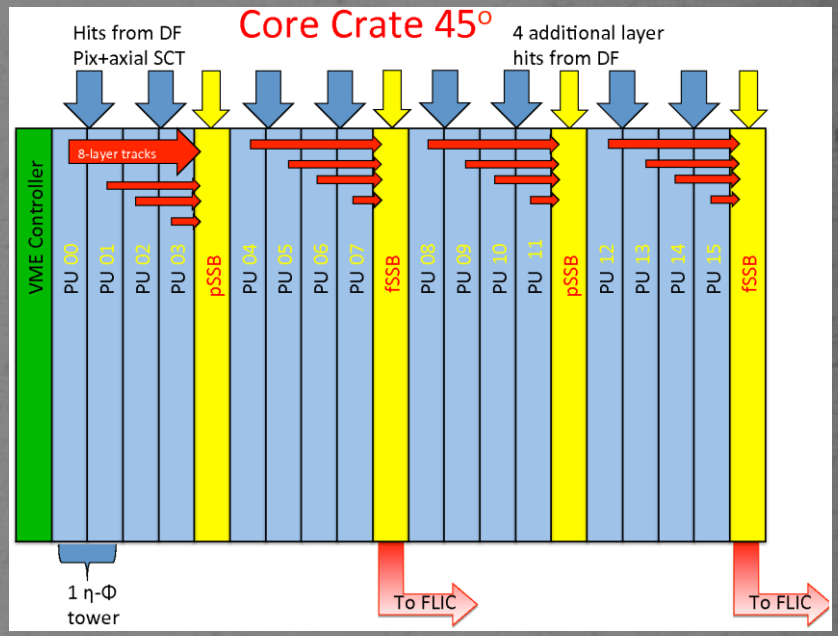
The Clustering Implementation

- The current implementation is an evolution of a linear algorithm with a high cost in terms of FPGA resources
- In the previous algorithm grids of 168x4 or 328x8 pixels were used. For these grid sizes the extrapolated area and clock results (for the Spartan 6-LX150T) would be:

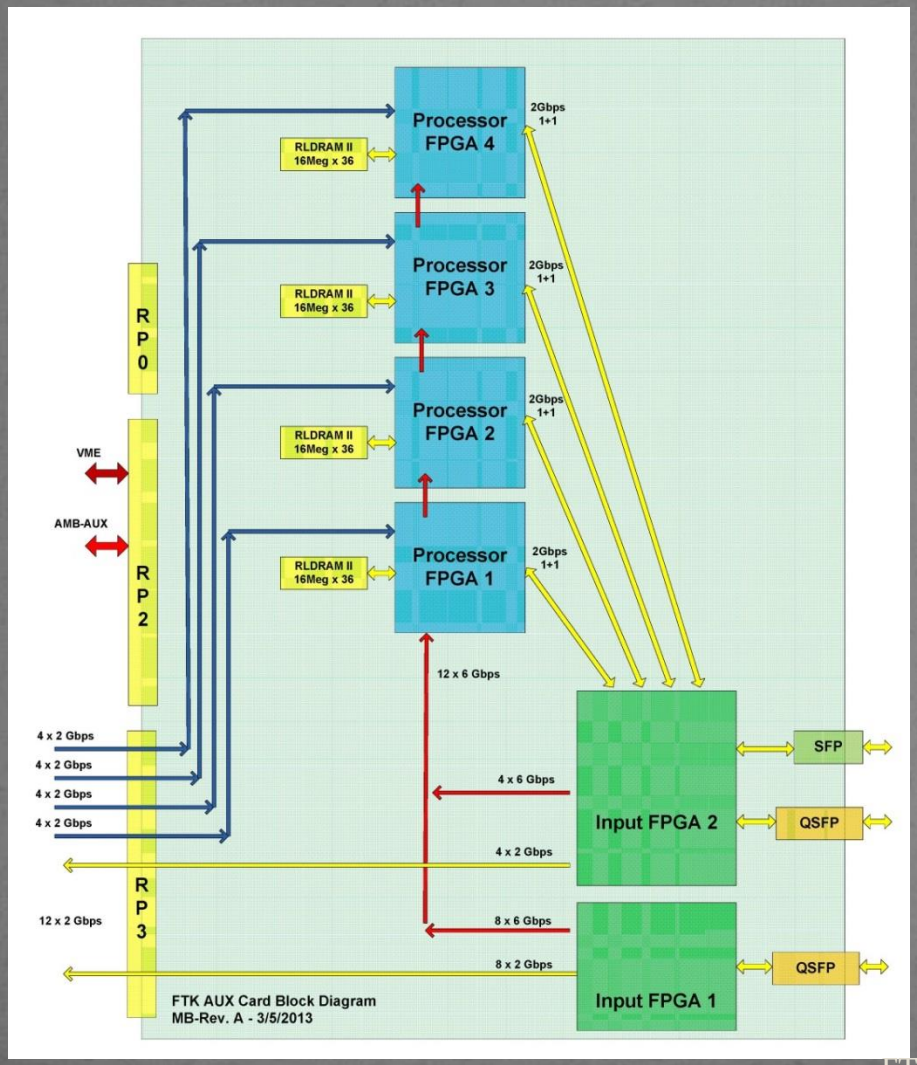
Grid Size	Slice Registers	Slice LUTs	Clock	Frequency
21x8 (current)	696 (1%)	1950 (2%)	12ns	83Mhz
168x4	2784 (1.5%)	7800 (8.2%)	68ns	14.8Mhz
328x8	10510 (5.7%)	30457 (33%)	265ns	3.8Mhz

The FTK processing unit

- The core of the system is composed of the AM board and the AUX card
  - The AUX card interfaces with the DF (input) and Second-stage board (output)
    - Prepare the input for the AM and do the 1st stage of the fit to remove low quality candidates
  - The AM board performs the pattern matching
- The final system will have 2 boards for each tower
  - Each tower has 4 independent engines
  - The system will contain 512 independent engines



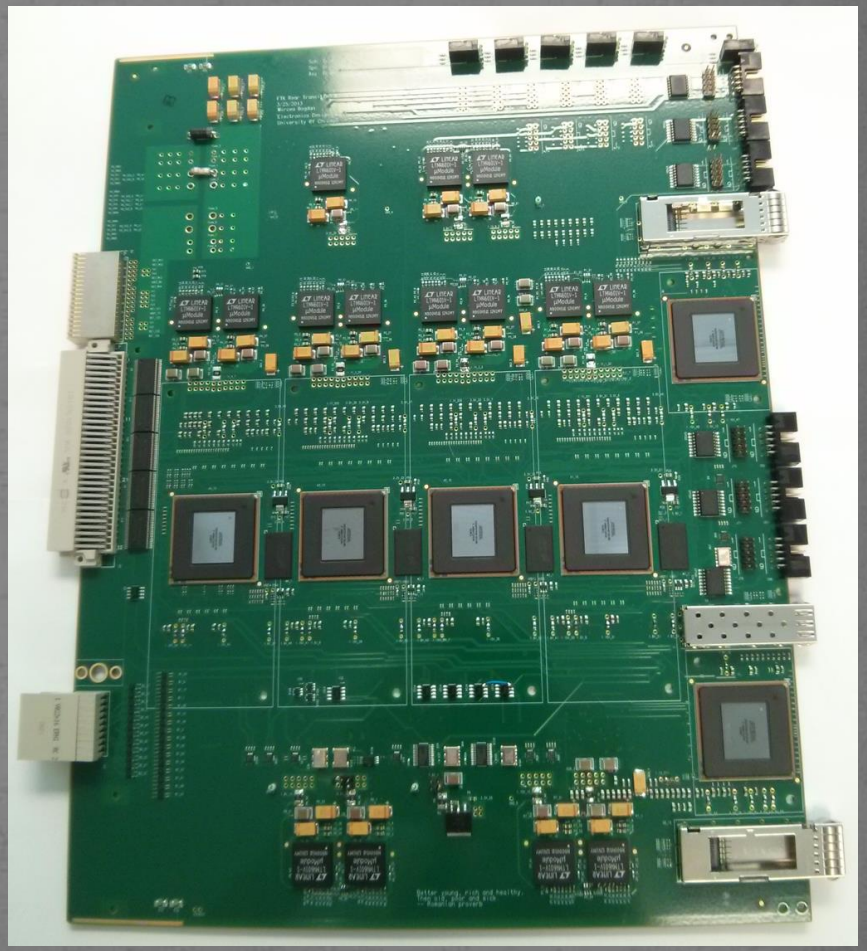
AUX Card (1/2)



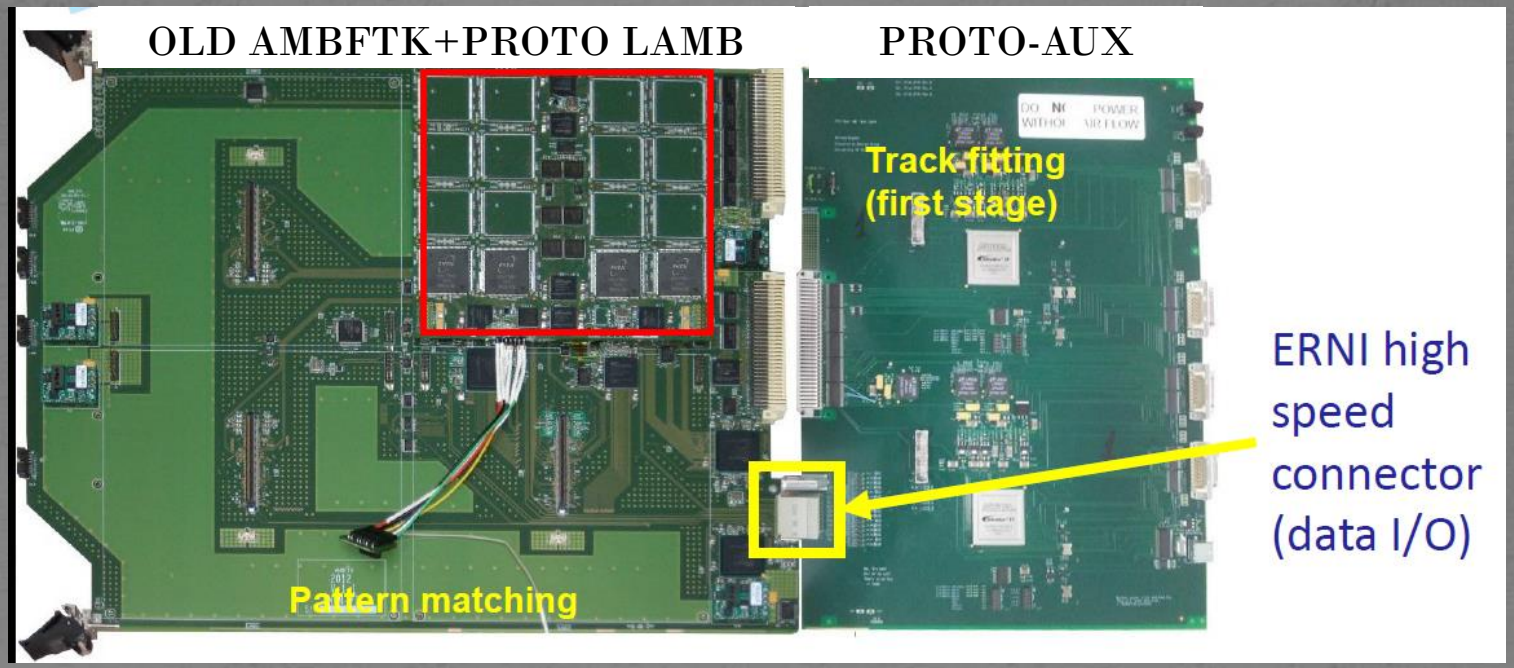
- Receives full precision clusters from the DF
- 9U VME Rear Transition Card
  - 280mm deep!
- I/Os:
  - Fibers: to DF, SSB
    - 2 x QSFP (8 x RxTx @ 6Gbps)
    - 1 x SFP (1 x RxTx @ 2Gbps)
  - P3 Connector: Data to AMB
    - 12 x Out @ 2Gbps
    - 16 x In @ 2Gbps
  - P2 Connector: VME control, power
- Processing power: 6 Arria V FPGAs
  - 20 Mb RAM, ~1000 DSPs each

AUX Card (2/2)

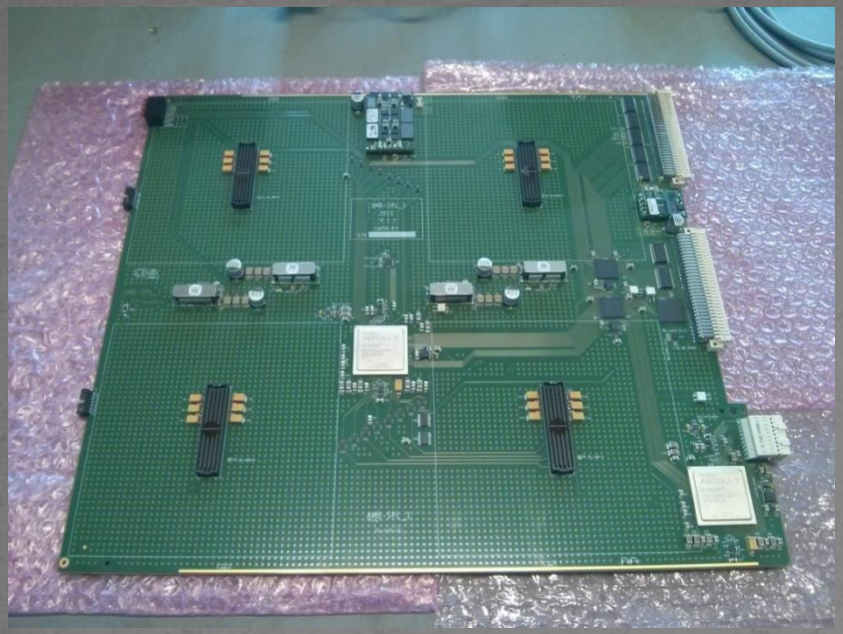
- Convert 32 (16) bit pixel (sct) hits into 12 bit coarse resolution superstrips to send to AM, store full resolution hits for later use
- Received matched roads from AM and fetch full resolution hits
- up to 8kHz road rate
- Do 8-layer track fitting using full precision hits to reject fake roads
- up to 1 fit per ns average
- Send tracks passing chi2 cut to Second Stage
- 20 MHz single track output rate

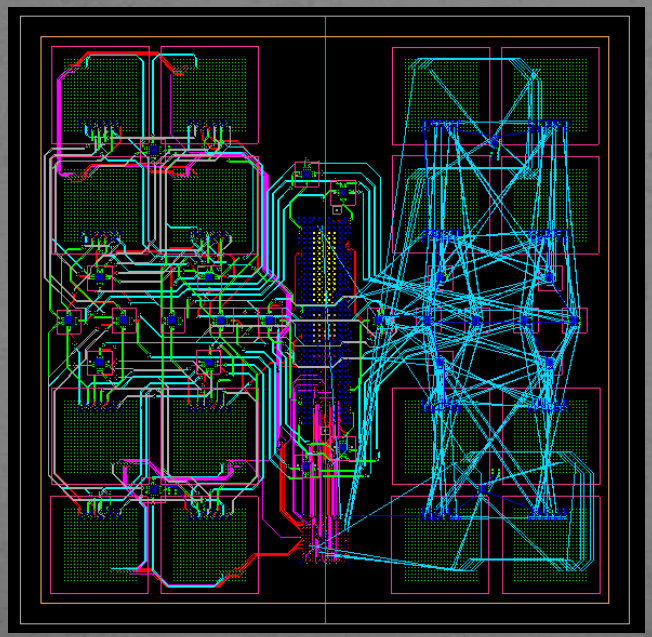


Associative memory board (AMBFTK) and Large Area Mezzanine board (LAMB)



- Associative memory board receives coarse resolution hits from the AUX using high speed connector
- Each board is composed of 4 LAMBs with AM chips
  - Each LAMB-FTK will contain 16 chips, ~10^6 patterns/LAMB

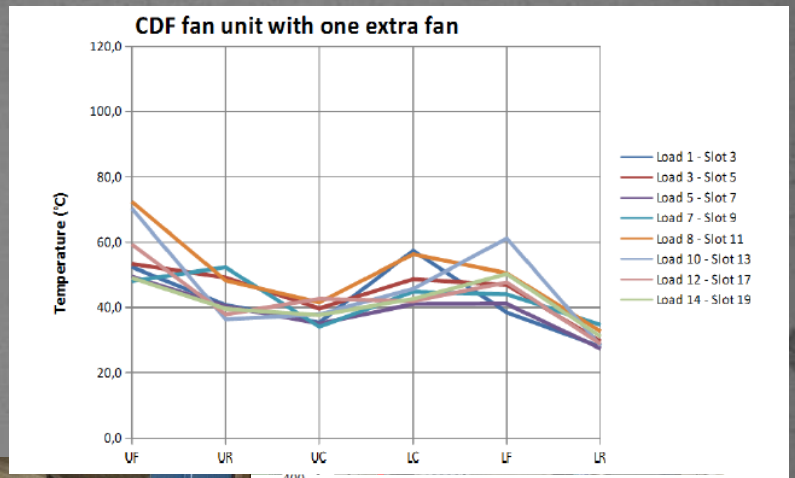


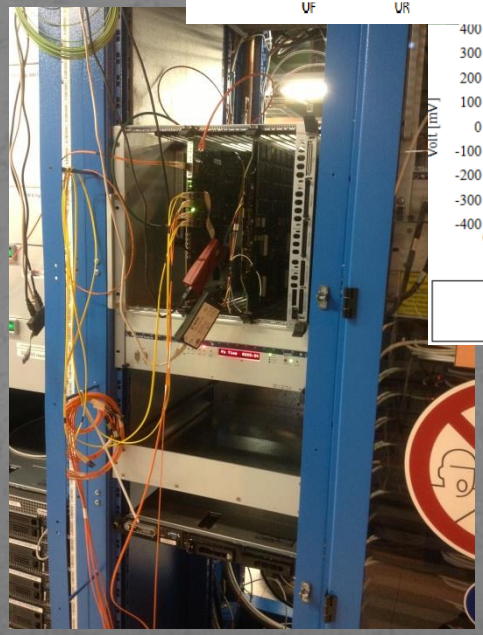


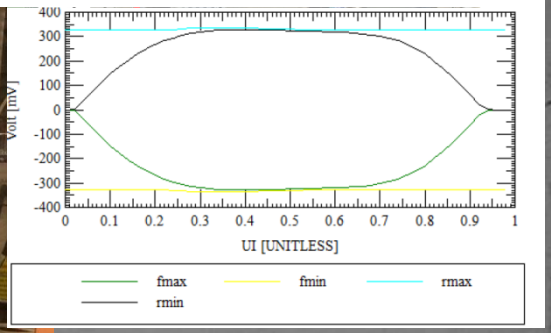
- AMBFTK is EURCARD 9U format
- Massive serial I/O
  - 2 Artix 7 FPGAs
  - Only serial communication busses
- Additional FPGAs for VME control
  - Slave for VME communication in the AUX-card
- LAMB redesigned for the newer AM-chip
  - Serial communication replaced the parallel busses
  - See M. Beretta talk on 24/09
    - https://indico.cern.ch/contributionDisplay.py?contribId=50&confId=228972
- Different voltages to be distributed
  - 3.3V for the I/O
  - 1.2V AM-chip
- High power consumption, about 200 W

Processing unit tests

- Existing prototypes of the PU were tested
- Cooling tests for the crates were performed
- High-speed links between AMBFTK and the AUX successfully tested
- A limited integration test with the ATLAS DAQ was also successfully performed before the LHC shutdown
  - Previous generation AM-board and LAMB
- Additional tests are expected to start in the winter

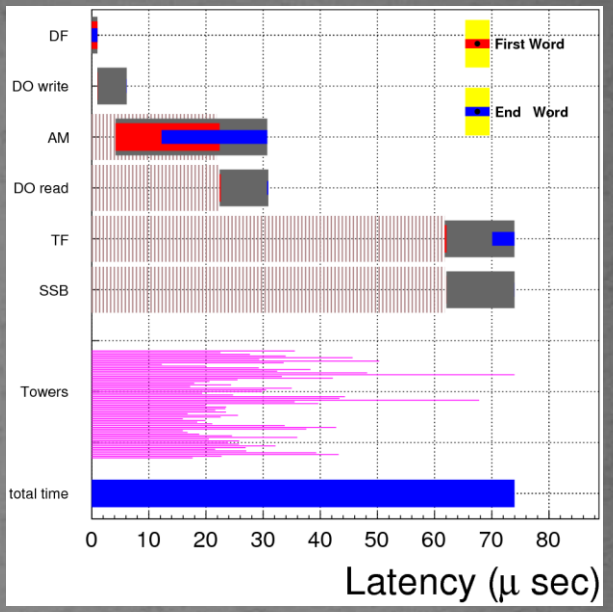


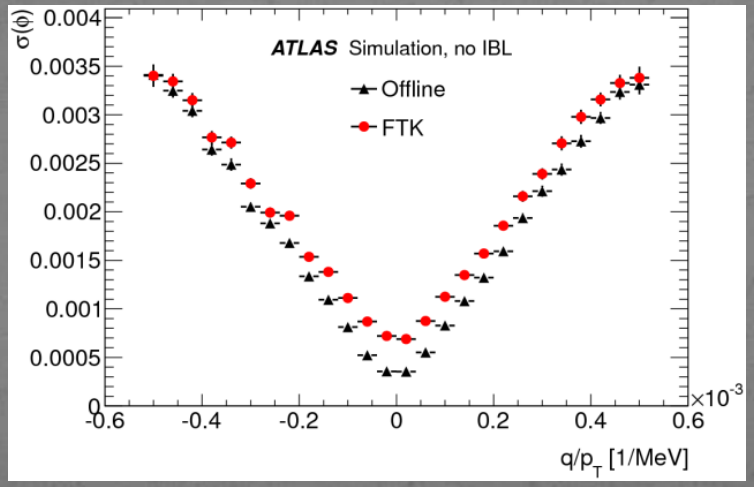


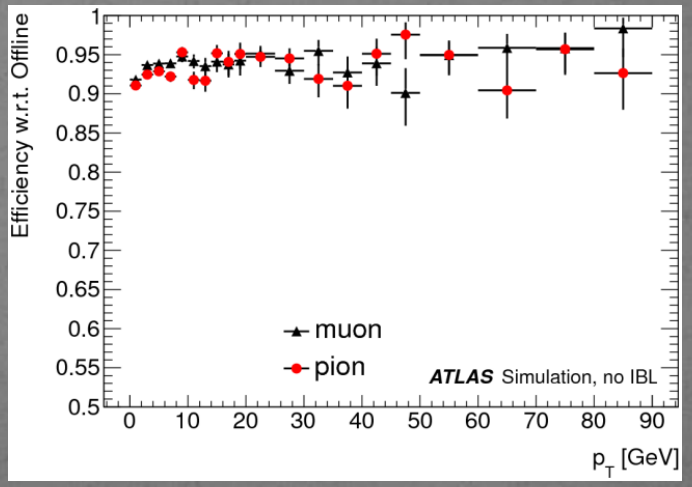


Simulation results

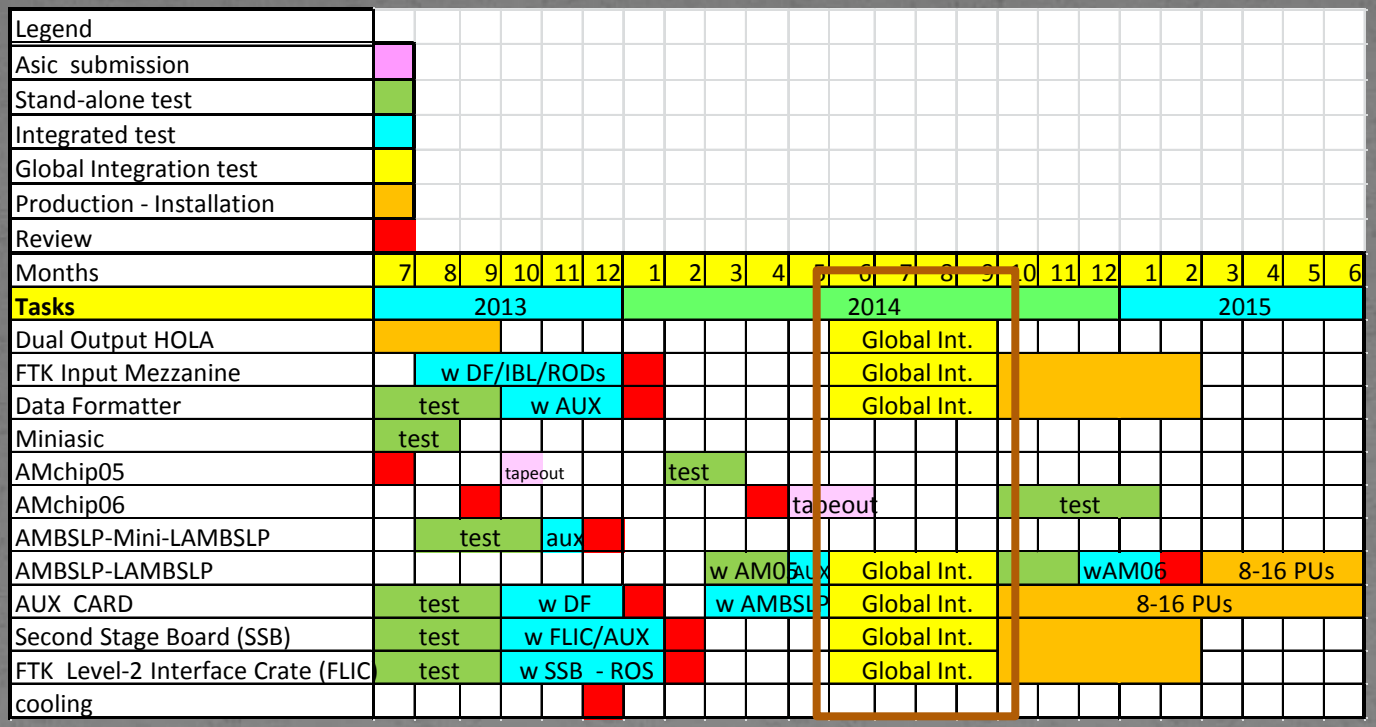
- FTK detailed simulation has been performed
- The load ho the system is compatible with allowed latency
- FTK tracks show a near to offline result in many quantities key quantities
  - HLT CPUs can use the tracks to make a preliminary identification of the events
  - Allowing to use the existing resources for more complex selections







Schedule



- Tests in are already started in the single institutions
  - Some tests already performed, no issues found
- Integration tests at CERN are expected starting next year
- First collected data expected during summer 2015

Conclusions

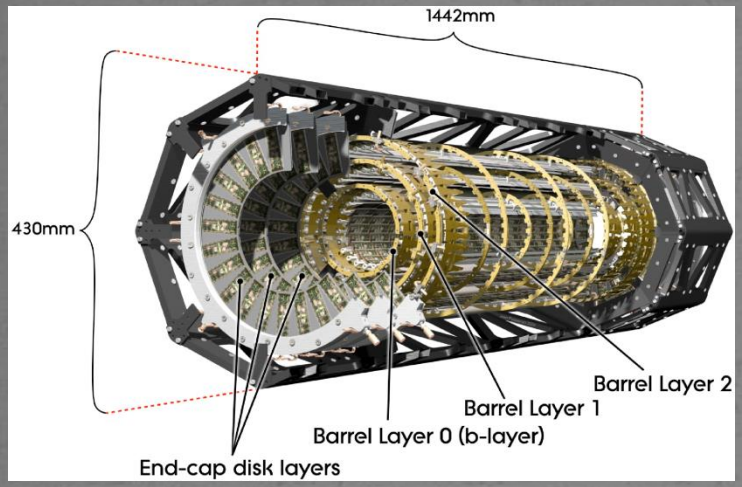
- FTK TDR has been published in May
  - https://cds.cern.ch/record/1552953/?ln=it
- FTK is able to improve the ATLAS trigger performance
  - FTK tracks can be used to identify interesting objects
  - The tracks can be used as by the HLT algorithms
    - More detailed integration studies are ongoing
- Prototypes of the main components are under construction or final design
  - The processing unit boards are in advanced state
    - Preliminary integration tests done
- FTK is expected to collected data from 2015

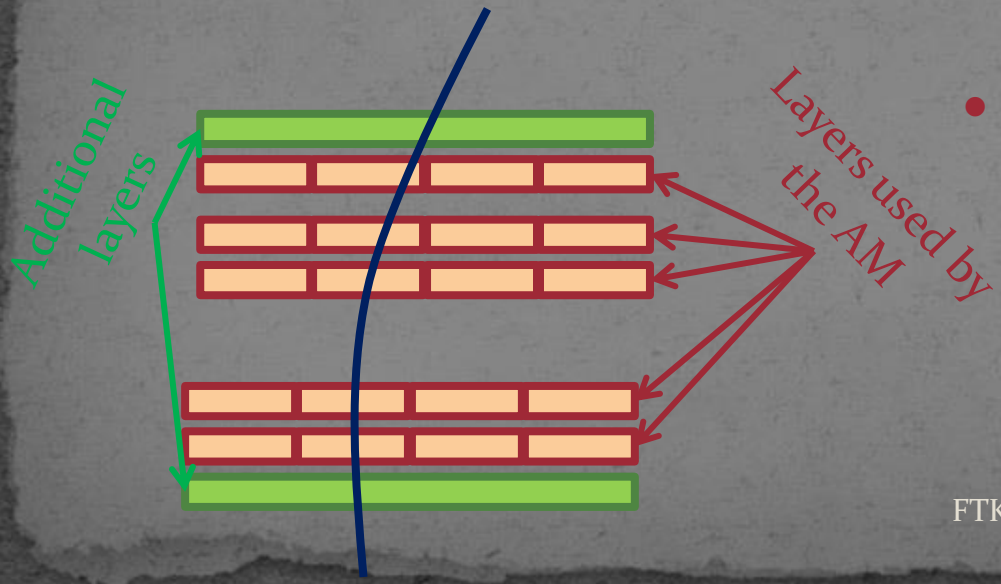
Acknowledgements

- The Fast Tracker project receives support from Istituto Nazionale di Fisica Nucleare; the US National Science Foundation and Department of Energy; Grant-in-Aid for Scientific Research from the Japan Society for the Promotion of Science and MEXT, Japan; the Bundesministerium für Bildung und Forschung, FRG; the Swiss National Science Foundation; and the European community FP7 Marie Curie OIF and IAPP programs.

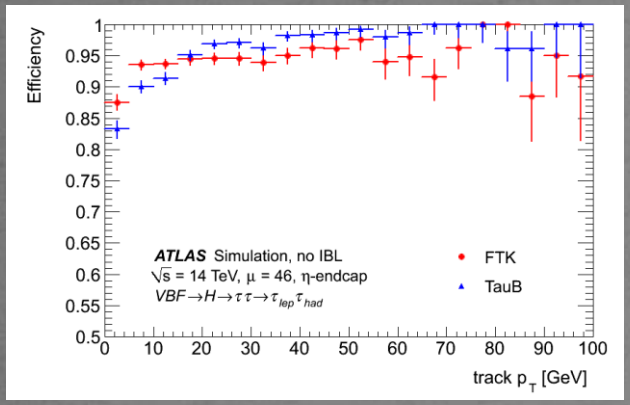
Backup

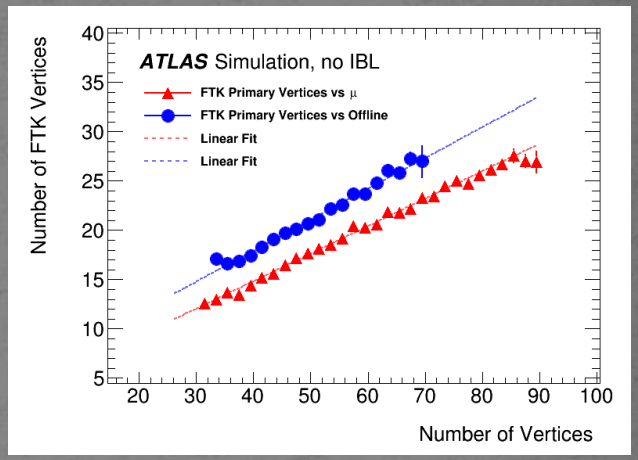
Tracking with AM at ATLAS

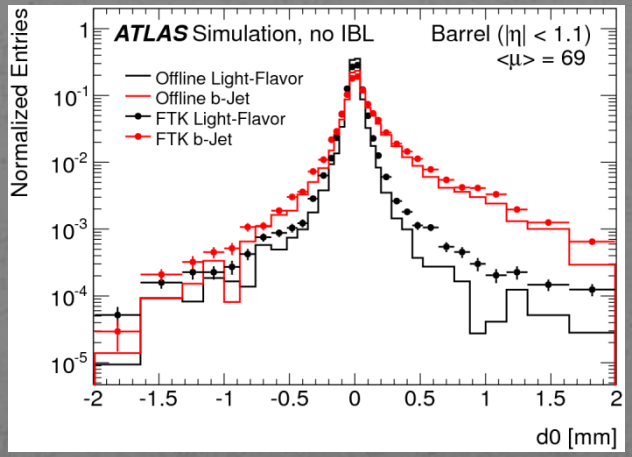




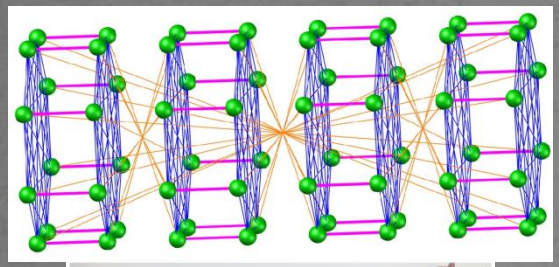
- The ATLAS inner detector was not originally designed for HW trigger
  - Study required to find the best compromise between HW complexity and performance
- Pattern recognition based on 8 silicon layers
  - 3 Pxl +5 SCT sensors
- Track fitting performed in 2 stages
  - 1st stage confirm the road
  - 2nd stage extend the track to improve the quality and reduce the fakes


Efficiency
ATLAS Simulation, no IBL
√s = 14 TeV, μ = 46, η-endcap
VBF→H→ττ→τ_lep τ_had
FTK
TauB
track p_T [GeV]


ATLAS Simulation, no IBL
FTK Primary Vertices vs μ
FTK Primary Vertices vs Offline
Linear Fit
Linear Fit
Number of FTK Vertices
Number of Vertices

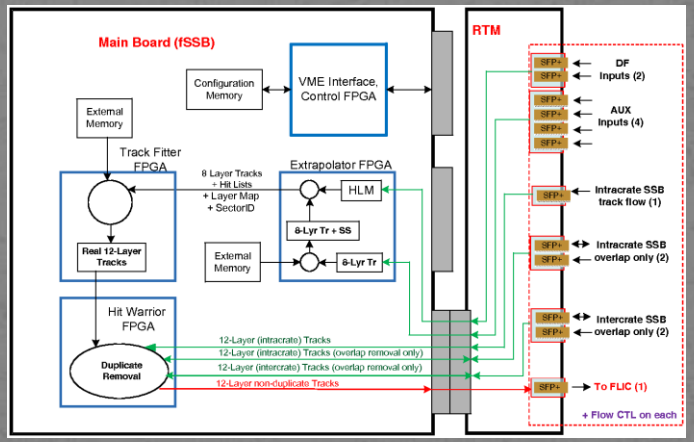

ATLAS Simulation, no IBL
Barrel (|η| < 1.1)
<μ> = 69
Offline Light-Flavor
Offline b-Jet
FTK Light-Flavor
FTK b-Jet
Normalized Entries
d0 [mm]

Status of the other main components



DATA FORMATER

- Handles the input of the system, distributing the data to the processing units
- Large data exchange between the boards
- Uses ATCA technology with full mesh backplane



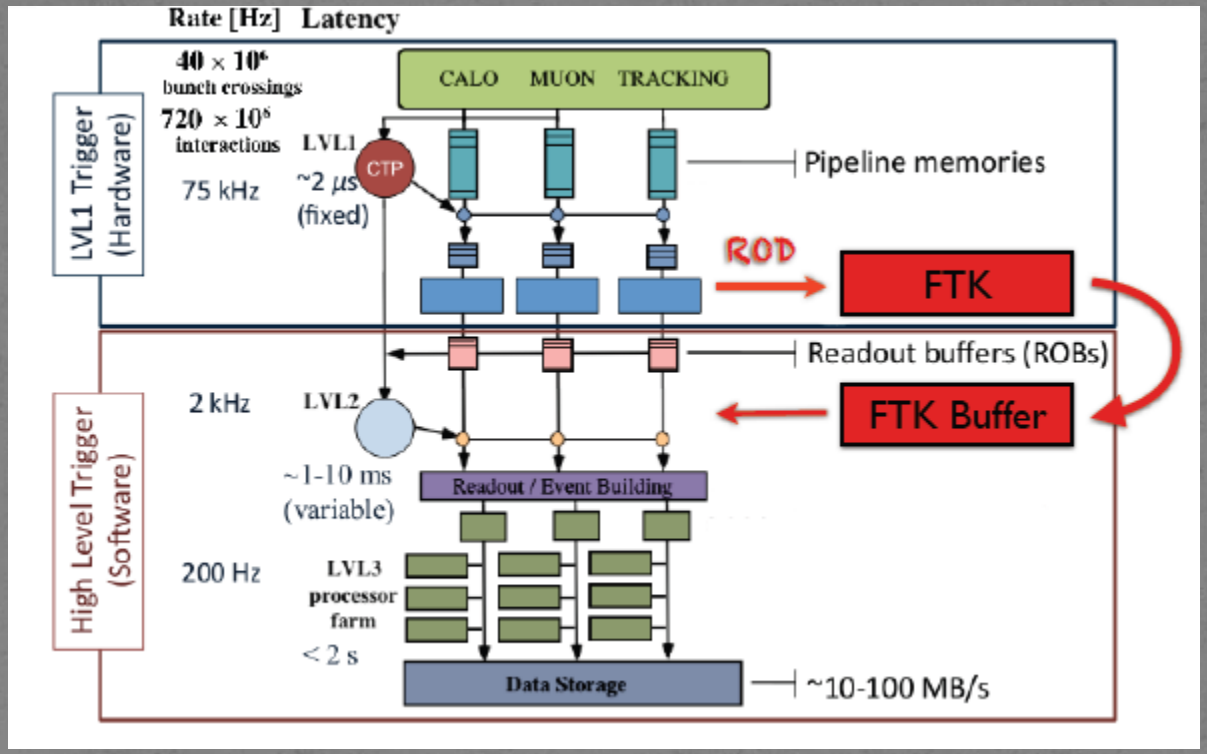
SECOND STAGE BOARD

Improves the track candidates calculated by the PUs
Responsible for duplicate suppression

FLIC

Interfaces the FTK processor with the ATLAS HLT

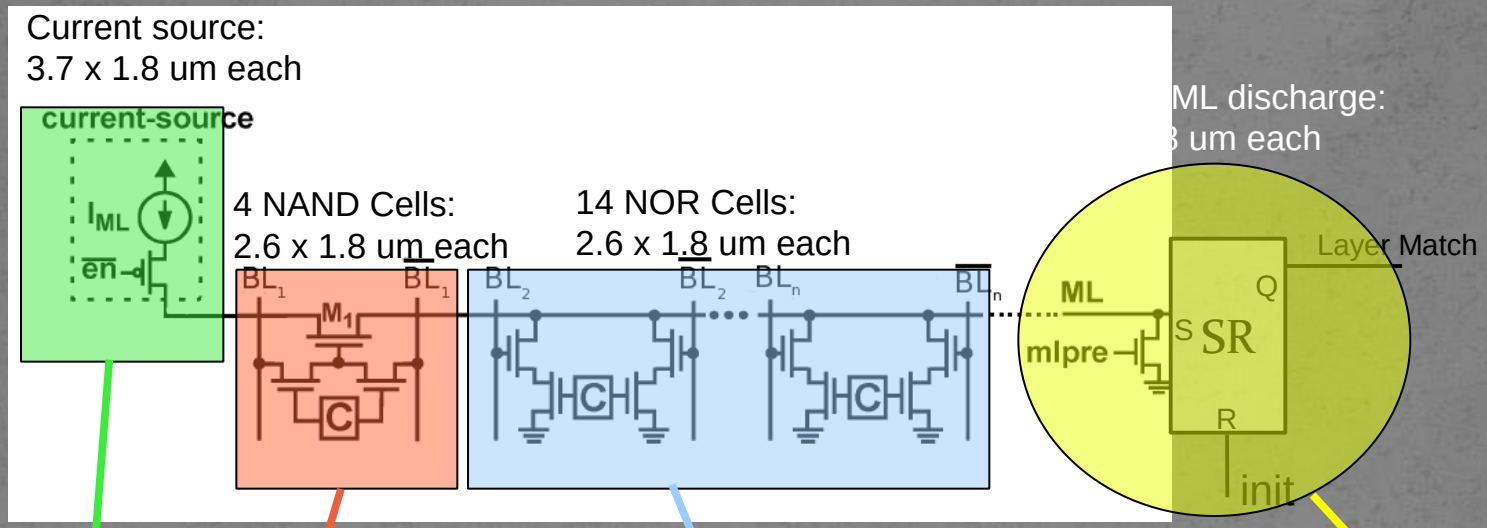
FTK within the ATLAS DAQ



Associative Memory Layer

To save power we have used two different match line driving scheme:

- *Current race scheme (dummy layer timing)*
- *Selective precharge scheme*



Full Layer layout : w=~53µm X h=1.8 µm