Design of an FPGA-based embedded system for the ATLAS Tile Calorimeter front-end electronics test-bench

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on behalf of the ATLAS Tile Calorimeter System

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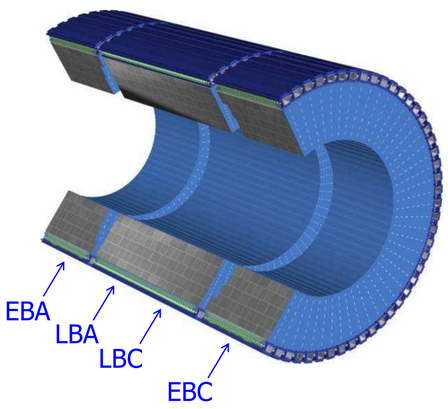
Tile Calorimeter

The Tile Calorimeter (TileCal) is a hadronic sampling calorimeter made out of steel plates and plastic scintillator tiles which covers the central region of the ATLAS experiment. It is divided in 3 sections along the beam direction, each of which is segmented azimuthally into 64 modules.

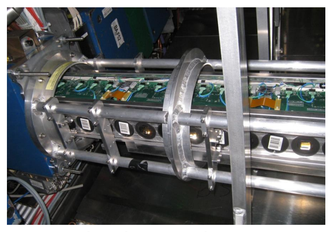
The light produced by a charged particle passing through the plastic scintillating tile is guided by wavelength shifting fibers to photomultiplier tubes (PMTs). The number of channels needed to digitize and read-out all the calorimeter signals is about 10,000. When the front-end electronics receives a Level 1 trigger accept (L1A), data from that bunch crossing is transmitted through optical fibers to the Read Out Driver (ROD) modules in the counting room.



Tile Calorimeter

Front-End Electronics

All the electronics required for the readout of the PMTs are hosted inside super-drawers in the outmost part of the detector.
The front-end electronics (3-in-1 cards) provide shaped PMT signals to the digitizer boards, analog trigger outputs to the adder boards and integrated PMT currents for channel calibrations (ADC-I board).
The digitizers convert the analog signals and store them in pipeline memories, while the adder boards send a tower trigger analog sum to the L1 Calo system. Once the digitizer receives a L1A signal via a Trigger and Timing Control receiver (TTCrx), the interface card collects the corresponding data from the digitizers and sends it to the back-end using optical fibers.
In addition, two separate CAN bus lines are used to control and monitor the high voltage applied to the PMTs and to readout the ADC-I board. TTC commands are used to configure and control calibration circuitry of 3-in-1 cards and digitizers.



Tilecal super-drawer

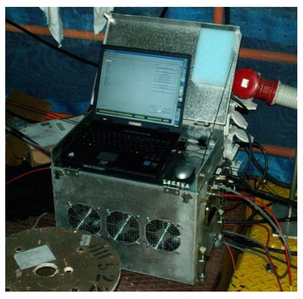
MobiDICK 4

Introduction

The MobiDICK 4 system is the new generation of portable test-bench used for the full certification and quality checking of the super-drawers in the TileCal detector during the maintenance periods.

This system performs a variety of tests on the front-end electronics, guaranteeing the correct operation before and after the insertion of the super-drawers in the detector modules.

This new version of MobiDICK, compared to the previous VME based system, enhances mobility and improves the accuracy of tests.



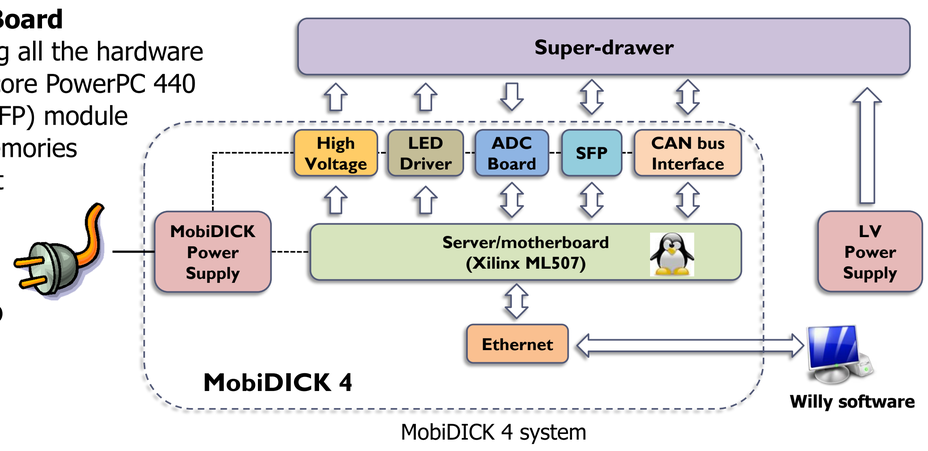
Previous version of MobiDICK based on a VME system

Hardware

Xilinx ML507 Evaluation Board
- Works as server, controlling all the hardware
- Virtex 5 FX70T with hard core PowerPC 440
- Small Format Pluggable (SFP) module
- SODIMM slot for DDR2 memories
- 10/100/1000 Ethernet port
- Compact Flash slot

LED Driver board
- Generates a 20 V, 20 ns wide pulse to drive an LED
- TTL input interface

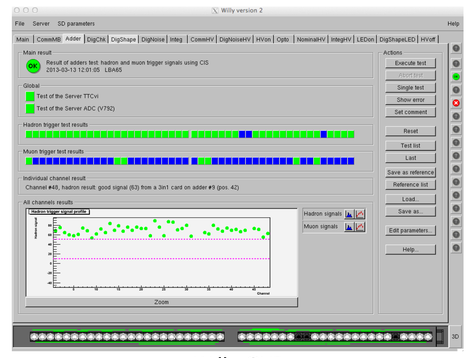
High Voltage board
- Feeds PMTs with -830V
- TTL input interface



MobiDICK 4 system

ADC board
- Digitizes analog trigger tower signals coming from adder boards
- Two Texas instruments ADS5271 ADCs
- 16 ADC channels
- 12-bit x 40 MSPS
- Serialized LVDS output interface

CAN bus dongles
- Commercial devices
- Serial port to CAN Bus interface
- Slow control and ADC-I board readout



Willy GUI

Software

MobiDICK4 implements a client-server architecture between the ML507(server) and a laptop (client). On the laptop a Graphical User Interface (GUI) called Willy, allows users to manage the different tests needed for certification, while the server controls hardware, extracts and processes data and sends results to the client.

Mechanics

- Custom aluminum box
- Size 35 cm x 40 cm x 20 cm
- Weight : 4 kg
- Forced air cooling system

MobiDICK 4

Embedded System Architecture

Backbone architecture

The core of the embedded system is a PowerPC 440 processor connected to different custom and vendor IP cores implemented on logic resources of the Virtex 5. These IP cores perform the communication with the PowerPC processor through the Processor Local Bus (PLB) as slave devices.

Several hardware devices of the previous version have been replaced by firmware and implemented on the ML507, as a TTCvi card and an ODIN card, obtaining an appreciable improvement in size, weight and portability.

G-LINK receiver IP core

The G-Link receiver IP core emulates the Agilent HDMP-1034 chip receiving and decoding the G-Link data stream from the interface card through the SFP module at a data rate of 800 Mbps. This IP core includes a CRC module which detects data integrity errors in the received data and errors in the format on-the-fly.

TTCvi emulator IP core

The TTCvi emulator IP core emulates most of the TTCvi functionalities and is easily controlled from Linux:
- Short-format asynchronous and synchronous broadcast commands
- Long-format asynchronous individually-addressed and broadcast commands
- Different fixed L1A trigger rates: 1 Hz, 100 Hz, 1 kHz, 5 kHz, 10 kHz, 25 kHz, 50 kHz, 100 kHz
- Single L1A signals

Synchronous operation is achieved via a FIFO memory which is capable of storing up to 8 commands/L1A and the corresponding Bunch Crossing (BC) at which they should be executed. This IP core manages a VHDL module which Time Division Multiplexes (TDM) L1A signals and commands using BiPhase Mark (BPM) encoding and sends the encoded data to the super-drawer through the SFP module.

Orbit Clock IP core

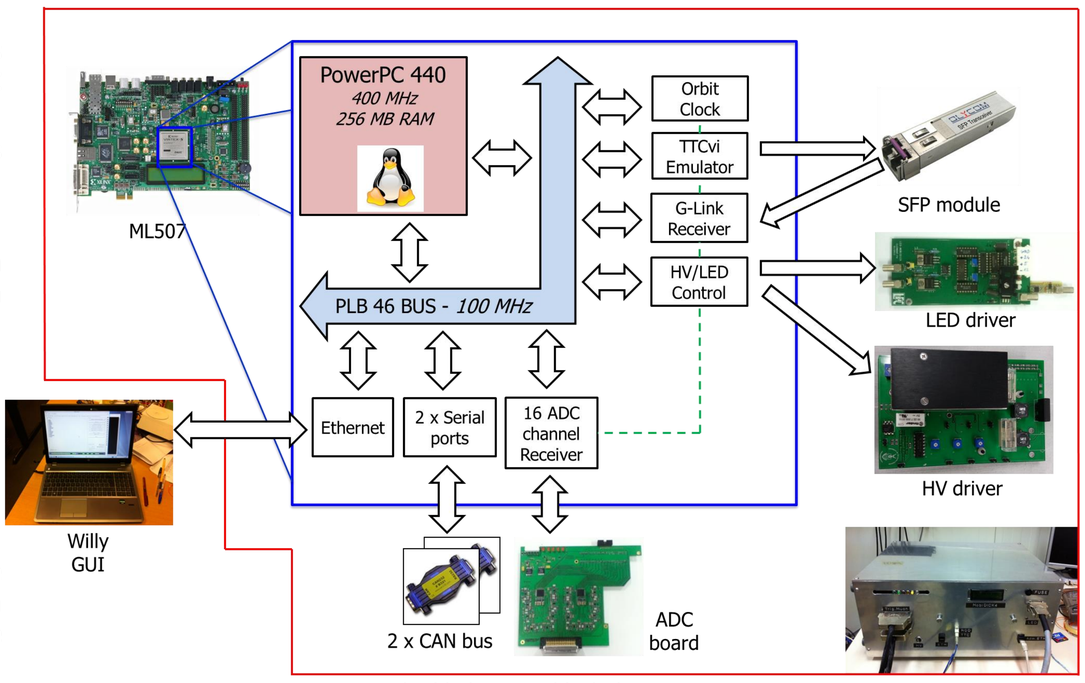
The Orbit Clock IP core generates a pulse train of period 89.1 μs (corresponding to 3564 BC using a 40 MHz clock) which allows the synchronization of commands and L1A signals with the generated clock. This clock is used to fire the train of stored commands in the FIFO memory at every tick.

ADC IP core

The ADC IP core receives and deserializes 16 ADC channels at a data rate of 480 Mbps each using the ISERDES resources in the Virtex 5. It also includes 24 kB RAM memories which store the digitized data when a special command is executed by the TTCvi emulator IP core.

High Voltage and LED driver IP core

The High Voltage and LED driver IP core implements a very simple remote control interface to the different devices. It allows switching on/off the High Voltage module and controlling the pulse generation of the LED driver which is synchronized with the FIFO memories in the ADC IP core.



Embedded system block diagram

Software libraries

A set of drivers and libraries written in C++ allows the embedded Linux to manage the hardware through the IP core registers.

Operating system

A custom lightweight version of embedded Linux runs on the PowerPC, where the root file system is loaded into the RAM memory.
This Linux version has been built using the Embedded Linux Development Kit 4.2 from DENX and includes the BusyBox package.

Booting system

The embedded system boots from a System ACE file stored in the compact flash when the ML507 is powered on. This file contains all the data needed to configure the Virtex 5, initialize the internal block RAM, initialize the external RAM memory with the Linux image and boot up the PowerPC.

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