AIDA

Advanced European Infrastructures for Detectors at Accelerators

Deliverable Report

WAFER POSTPROCESSING (THINNING, TSV)

Moser, Hans-Gunther (MPG-MPP)

27 May 2013

The research leading to these results has received funding from the European Commission under the FP7 Research Infrastructures project AIDA, grant agreement no. 262025.

This work is part of AIDA Work Package **3: Microelectronics and interconnection technology**.

The electronic version of this AIDA Publication is available via the AIDA web site <http://cern.ch/aida> or on the CERN Document Server at the following URL: <http://cds.cern.ch/search?p=AIDA-D3.5>

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Advanced European Infrastructures for Detectors at Accelerators

Seventh Framework Programme, Capacities Specific Programme, Research Infrastructures,
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Abstract:

Wafer post processing (thinning, TSV): This deliverable reports on the qualification of post processing for wafers to be prepared for the 3D interconnection process. This may include wafer thinning, addition of special metal layers (UBM), planarization and etching of vias. Post-processed wafers to be used for 3D interconnection are available. This report gives a short description of the wafers and the post-processing that was performed on them.

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Delivery Slip

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Executive summary

In AIDA WP 3 several subprojects have been defined, each using a different approach to 3D technology and working with different industrial partners.

The subprojects sample technological approaches which range from 'mature' (available for production at low risk without important R&D, however with moderate performance) to 'challenging' (need of R&D with high risk, but having the potential to reach superior performance). Thus a knowledge pool of different technologies and their respective usefulness and potential for HEP applications will be created.

Most of the sub-projects use the mature via-last technology for TSV, which requires post-processing.

Two of the 5 sub-projects which need post-processing have post-processed wafers in hand. In two sub-projects the post processing started or is about to start, one sub-project needs to wait for the availability of the CERN access to 65 nm technology.

1. INTRODUCTION

The main objective of AIDA WP3 is the demonstration of the feasibility of 3D interconnection for applications in Particle Physics. This is the basic goal of task WP3.2, and will be achieved by the fabrication of pixel detectors and readout electronics, interconnected by advanced 3D integration technologies. The knowledge gained with the construction of these demonstrators can be used to design and fabricate detectors for specific applications in particle physics. There are in principle two different technological approaches to 3D integration, depending at what stage the TSVs (Through Silicon Vias) are fabricated:

1) Via First (or Via Middle): in this approach the vias are etched and filled during the CMOS processing. Via first is basically a first step in the production chain, before any processing of transistors and metal layers. In the via middle approach the vias are etched and filled after the transistor processing but before the deposition of the metal layers. In both cases the via processing is integrated in the CMOS process. Hence this can only be done by the fab processing the CMOS wafers. This technology usually allows for very small (few µm) vias with large aspect ratios. The vias can be connected directly and even covered by the standard metal layers of the CMOS process allowing a very efficient use of the wafer area. This is the technology for more advanced application of 3D integration, requiring highest via density. On the other hand only few vendors offer this process and none allows for interconnection of different wafers types.
2) Via Last: in this approach the vias are processed after the completion of the CMOS processing. In principle wafers from any fab and any technology can be processed by a third party. Hence via last is extremely flexible in the choice of technology and allow easy 3D interconnection of heterogeneous technologies. Disadvantages are the larger space requirements for the vias since the area needed for them cannot be used for CMOS circuitry, which has to be designed accordingly. The vias offered to date have a rather large diameter and a low aspect ratio, hence the process cannot be used for high density pixel-to-pixel interconnect. Post processing can only be done on complete wafers, which excludes ASICs from

MPW. Nevertheless via last is offered by several vendors and can be considered as rather mature.

This document discusses the status of the post-processing of the ASIC wafers that some WP3 subprojects will use for the construction of demonstrators. As discussed in the following, full wafers with 3D-compatible ASICs are already available to some subprojects, as they were developed in the frame of other large experiments or collaborations. These chips are based on 130nm CMOS processes, or even on technologies with larger feature sizes. Some sub-projects pursue post processing of the more advanced 65nm technology, which has to wait till those wafers become available.
For the sub-projects looking in the more advances via-first technology no post-processing is needed.

2. POST-PROCESSING IN WP3 SUBPROJECTS

2.1. PLANS OF SUB-PROJECTS FOR POSTPROCESSING

- **Bonn/CPPM:** Interconnection of the ATLAS FEI4 chips to sensors using bump bonding and TSVs from IZM (large diameter TSV, large interconnection pitch): The FEI4 wafers need to be post-processed (thinning, etching of vias and addition of a redistribution layer),
- **CERN:** Interconnection of MEDIPIX3 chips using the CEA-LETI process: The MEDIPIX3 wafers need to be post-processed (thinning, etching of vias and addition of a redistribution layer),
- **INFN/IPHC-IRFU:** Interconnection of chips from Tezzaron/Chartered to edgeless sensors and/or CMOS sensors using an advanced interconnection process (T-MICRO or others). Tezzaron/Chartered offers a via-first technology. Hence no post processing is needed in the first stage of this project. Post processing may become necessary in a later stage preparing the wafers for interconnection (UBM).
- **LAL/LAPP/LPNHE/MPP:** Readout ASICs in 65nm technology interconnected using the CEA-LETI or EMFT process. The wafers need to be post-processed (thinning, etching of vias and addition of a redistribution layer).
- **MPP/GLA/LAL/LIV/LPNHE:** Interconnection of ATLAS FEI4 chips to sensors using SLID interconnection and ICV (high density TSVs) from EMFT. The FEI4 wafers need to be post-processed (thinning, etching of vias and addition of a redistribution layer),
- **UB**: 3D interconnection of 2 layers of Geiger-Mode APD arrays with integrated readout in Tezzaron Chartered technology. This via first approach does not need post-processing.
- **RAL/UPPSALA**
  Integration of a 2-Tier readout ASIC for a CZT pixel sensor using EMFT SLID technology and TSV including redistribution of I/O connections to the backside for a

4-side buttable device. The ASIC tiers need to be post-processed (thinning, etching of vias, adding UBM and redistribution layers)

For a more details description of these WP3 subprojects, the report for Deliverable 3.1 can be used as a reference.

2.1.1. Bonn/CPPM

The goal of this activity is to develop a 3D integration technology applicable to the innermost pixel layer of the detector at High Luminosity LHC. Within the AIDA R&D framework WP3, we propose to produce real chip/sensor assemblies to test an interconnection technique allowing the access to the wire bond pads of the 3D structures after bonding.

For these prototypes, we propose to use planar ATLAS pixel sensor wafers and the ATLAS pixel FE-I4 electronic chip wafers. The FE-I4 chip [1] contains readout circuitry of 26880 hybrid pixels in 80 columns by 336 rows and it is produced in the 0.13 µm feature size bulk CMOS process by IBM. The pixel pitch in FE-I4 is 50x250 µm. The dimensions, 20x19 mm^2, are the biggest among HEP chips and close to the maximum size allowed by most of the vendors. The backside wire bond pad access by means of via will allow mounting two (or four) chip modules with the sensor side on the mechanical-cooling carbon structure.

Three wafers of the FE-I4A chip are available and will be used for a first run of TSV fabrication.

First wafers of FE-I4B are available and were sent to Fraunhofer IZM in Berlin for post processing. IZM will thin them to 150 µm and etch tapered vias of about 40 µm (inner) and 100µm (outer) diameter. The vias connect the I/O contacts on the periphery of the FEI4 chip. The chip has been designed for this process by connecting metal 1 pads to the I/O. Thus the vias need only to be etched up to metal 1 and there is no need to traverse all metal layers. A redistribution layer will be added for the backside connection of the vias to wirebond pads. Results are expected in the last quarter of 2013.

2.1.2. CERN

The proposed project uses Medipix3 read out chips [2] as the platform for 3D integration development. The aim of the project is to utilize an existing mature TSV technology made available by CEA-LETI as a part of their open 3D initiative. The LETI via-last process offers vias of about 40µm diameter and 3:1 aspect ratio.

The post-processing at CEA-LETI has already been performed successfully. 10 wafers were processed in three batches. While the first two batches showed bad or marginal yield (TSV insulation), after process optimization the third batch showed very good yield (Fig. 1). The wafers are back at CERN and under test. A first test of the noise performance showed no difference between chips with and without TSVs (Fig. 2).

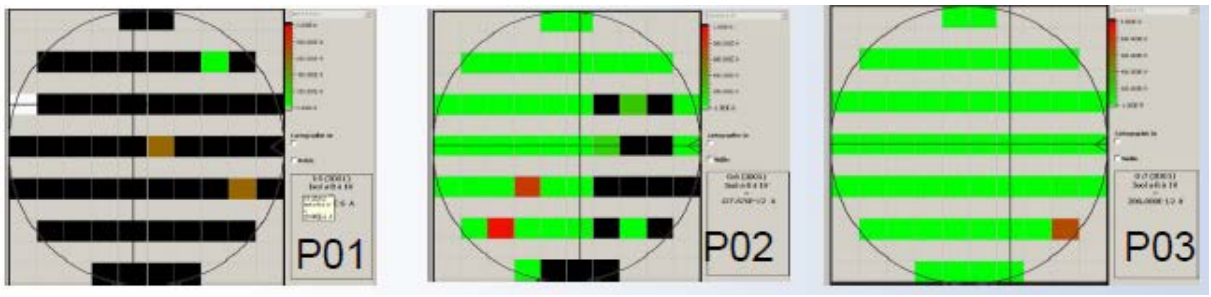

Fig. 1: Insulation between TSVs and bulk of the various sub-batches. While the first batch showed very low yield (chip marked black) the consecutive batches showed large improvements up to almost no defects.

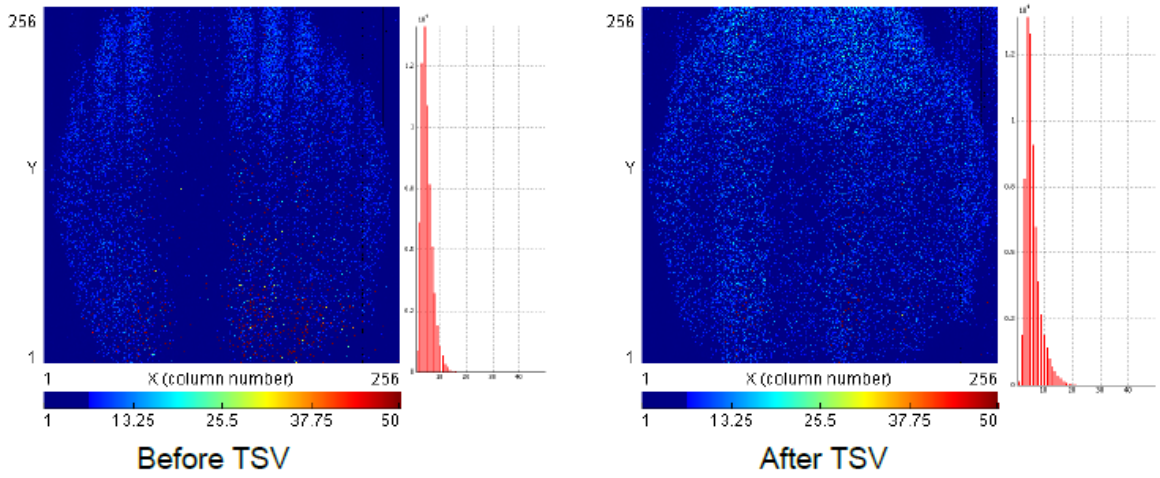

Fig. 2: Noise distribution of the MEDIPIX with and without TSV processing. No significant noise increase is visible.

2.1.3. INFN/IPHC-IRFU

The goal of the INFN/IPHC-IRFU proposal in the framework of the AIDA WP3 is the design and fabrication of a multi-tier pixel sensor resulting from the vertical interconnection of a CMOS readout circuit to a separate CMOS layer optimized for particle sensing and to a fully depleted edgeless or 3D detector. The project relies on CMOS sensors designed by IPHC-IRFU, fully depleted detectors provided by FBK Trento and a mixed signal readout chip designed by INFN.

The readout chip is foreseen to consist of a dual-tier mixed signal circuit fabricated in the Tezzaron/Globalfoundries vertical integration CMOS technology, where each tier is based on a 130 nm process. Since this is a via-first technology no further post processing is needed.

In a later stage the interconnection of these chips to the sensors may require post-processing (addition of UBM and microbumps). First studies with the Japanese vendor T-MICRO have been done.

2.1.4. LAL/LAPP/LPNHE/MPP

This subproject plans to exploit the challenging 65 nm CMOS technology to build a single electronic layer that houses both analogue and digital parts, interconnected to a sensor layer using via last and SLID innovative technology. This approach is similar to another proposed

subproject using ATLAS FEI4 readout circuit and some synergy will be achieved in terms of SLID evaluation and electrical tests. The availability of 65nm design tools for use in our laboratories for our application in high energy physics combined to novel 3D interconnect technology will create a new generation of advanced devices to increase the density, and minimize the space and power consumption.

For the time being the final design and production of the ASIC wafer has to wait for CERN to conclude a contract with IMEC for the access to the TSMC 65nm technology. The contract is already in a final stage and it is planned that the process becomes available in a few months.
A first 65nm demonstrator ASIC pixel readout circuit is scheduled for the end of 2013.

2.1.5. MPP/GLA/LAL/LIV/LPNHE

This activity regards the interconnection of the new FE-I4 ATLAS chip, designed for the upgrades of the ATLAS pixel system, to a compatible sensor by using 3D technologies developed by the Fraunhofer Institute EMFT. The post-processing for this vertical integration technology has to be performed at wafer level. EMFT offers an advanced TSV etching process which allows a large aspect ratio (10:1) and small diameter vias (5 µm). The SLID technology is bumpless and allows in principle for a high density of interconnections, limited only by the pick and place accuracy. Post-processing includes via etching, thinning, addition of a redistribution layer and adding the copper/tin layers needed for SLID. FEI3 wafers have already been processed with this technology and successfully interconnected (interconnection only without vias). The different architecture of the FEI4 chip with respect of the FEI3 (no free area for vias in the wire bond area, connection directly to metal 1) requires a modification of EMFT's TSV technology. Instead of etching the vias from the front side through the metal layers into the bulk and consecutive back etching, the vias need to be etched in already thinned wafers from the backside. The need of passivation of the via walls and contact opening to metal 1 is more challenging especially for large aspect ratio vias. This may require larger via diameters than in the old FEI3 project, but it is planned to maintain diameters below 25 µm, which is still substantially smaller than vias from other via last processes. EMFT is still working on detailed process planning and it is planned to start the post-processing in the next months. Wafers are available.

2.1.6. UB

Barcelona plans for 3D interconnection of two layers of Geiger mode APD arrays in order to increase the fill factor of such devices. The APD arrays are made in a CMOS process and include circuitry for quenching, recharge and readout. Single layer arrays have a rather low fill factor, a large limitation for tracking devices. By stacking two layers the APDs can be arranged in a way that one layer covers the dead areas of the other. Thus a fill factor up to 92% can be obtained. The most efficient layout requires pixel by pixel interconnect and therefore a high interconnection density. Hence Barcelona is looking in via-first technologies as offered by the Tezzaron/Chartered process. Hence no post-processing is necessary. The project will be submitted with the next Tezzaron MPW run (not yet announced).

2.1.7. RAL/Uppsala

These partners will look at two activities: one is for the construction of a full 3DIC stacked pixel ASIC with pixels interconnected between 2 layers, and the second is for an activity to redistribute I/O connections to the back of an ASIC to enable 4-side butted pixel detectors.

A 40 x 40 pixel readout ASIC has been built based on an existing 80 x 80 pixel Hexitec CZT readout circuitry [4]. The Analogue pixel circuitry is exactly the same as the Hexitec ASICs which are successfully being used. The second digital layer contains a run-down ADC in each pixel and the digital readout circuitry necessary from this layer. There is one TSV interconnect from the analogue pixel on the top layer to the digital on the bottom layer and one for each I/O connection as all readout is from the top layer. Both devices have been built and tested in previous years and the 8 wafers of devices have been supplied to EMFT Munich for integration. This post processing is expected to be finished by end of May.
Furthermore Hexitec single layer wafers have been post-processed at T-Micro. TSVs have been etched to reach the I/O pads from the backside and a redistribution layers was added (Fig. 3).

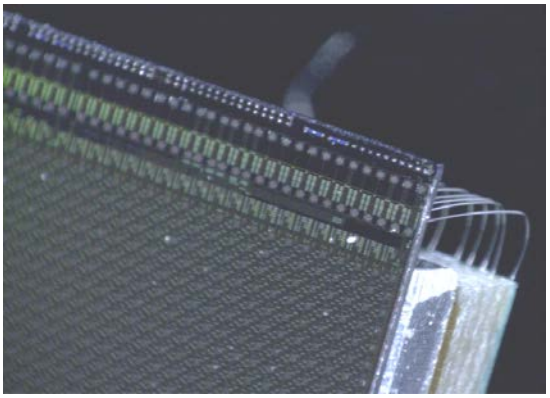

Fig. 3: ASIC after postprocessing: thinning to 120µm, etching of vias with 70µm diameter to contact I/O pads and addition of a redistribution layer.

3. CONCLUSION

This document presents a summary (see also Table 1) of the wafer post-processing steps that AIDA WP3 will pursue with the goal of preparing CMOS wafers for 3D integration. Two projects (CERN & RAL/Uppsala) have successfully post-processed wafers, that is thinning, via etching and adding of a redistribution layer. In two projects (Bonn, CPPM & RAL/Uppsala) the post-processing has already started and is expected to be finished soon. In another project (MPP/GLA/LAL/LIV/LPNHE) the post-processing is about to start. Two other projects concentrate on via-first technology and do not need post-processing at this stage of the project.

Since the sub-projects sample different technologies with different challenges it cannot be expected that all of them progress at the same pace. The projects using the more mature technologies (large diameter vias in existing wafers) have already achieved the deliverable. Projects aiming for small diameter vias or using advanced CMOS technology are a bit behind but expected to achieve similar goals by the end of 2013.

Project name	wafer	Via technology	Post-processing	status
Bonn/CPPM	FE-I4 (CMOS 130nm)	Via last	IZM	4Q 2013
CERN	MEDIPIX3 (CMOS 130nm)	Via last	CEA-LETI	available
INFN/IPHC-IRFU	Superpix1 (3D CMOS 130nm)	Via first	-	-
LAL/LAPP/LPNHE/MPP	Omegapix (CMOS 65 nm)	Via last	EMFT/CEA-LETI	4Q 2013
MPP/GLA/LAL/LIV/LPNHE	FE-I4 (CMOS 130 nm)	Via last	EMFT	About to start
UB	Tezzaron	Via last	-	-
RAL/Uppsala	Hexitec (CMOS 350 nm)	Via last Via last	EMFT T-MICRO	2Q 2013 available

Table 1. Status of wafer post-processing within the sub-projects

4. REFERENCES

[1] M. Garcia-Sciveres et al., NIM A, 636 (2011), 155-159

[2] M. Ballabriga et al., NIM A, 636 (2011), 15-18

[3] A. Manazza et al., "Vertical integration approach to the readout of pixel detectors for vertexing applications", *2011 IEEE Nuclear Science Symposium Conference Record*, Valencia (Spain), October 23 – 29, 2011, pp. 641-647.

[4] L. Jones et al., NIM A, 604 (2009), 34-37.