The Associative Memory system for the FTK processor at ATLAS

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Radiation Hardness of Semiconductor Detectors
3-5 July 2013, Florence

Introduction

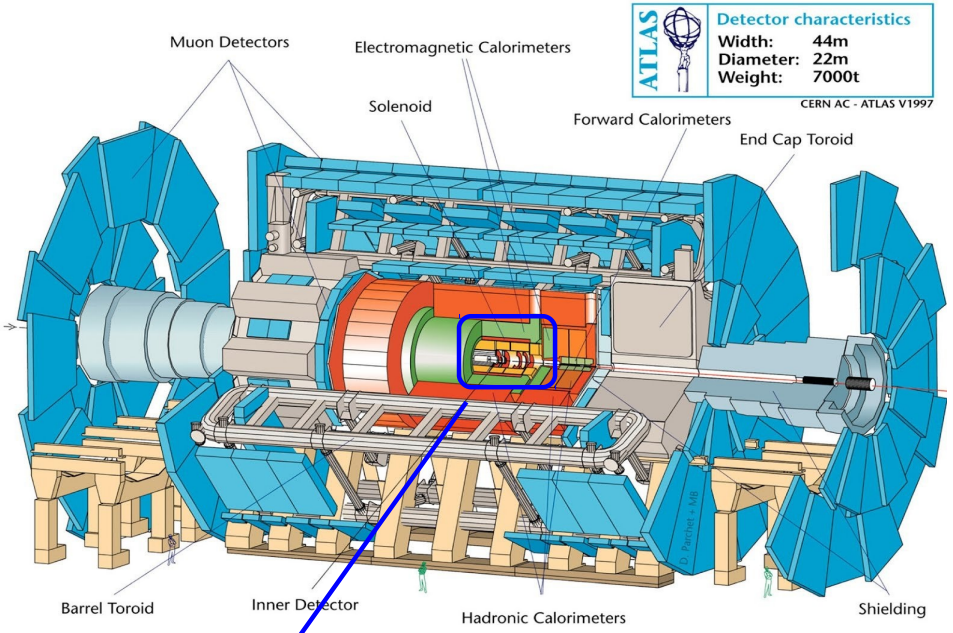
- Fast TracKer (FTK): New on-line tracker for Atlas upgrade based on Associative Memory technique
- FTK working principles
- FTK architecture, with a detailed description of the Associative Memory system
- Test of the prototypes
  - High speed links
  - Pattern Matching in the AM chip
  - Crate cooling

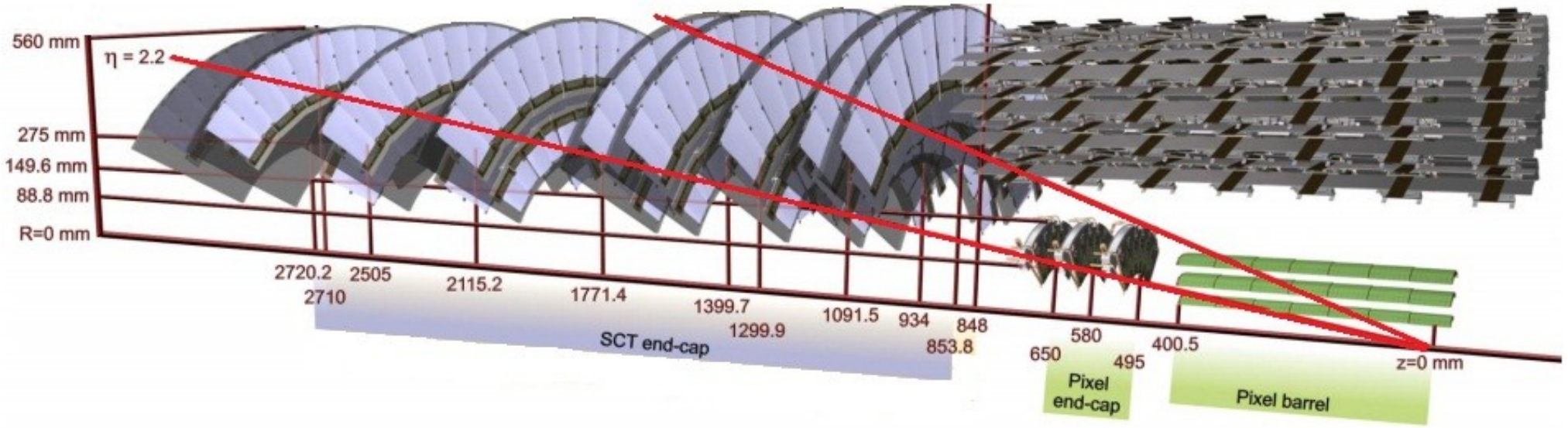
An online silicon detector tracker for the ATLAS upgrade

- FTK reconstructs charged particles trajectories in the silicon detectors (Pixel & SCT) at “1.5” trigger level.
- Extremely difficult task

  25 ns inter-bunch time

  ~70 overlapping events (pile-up) at highest luminosity.





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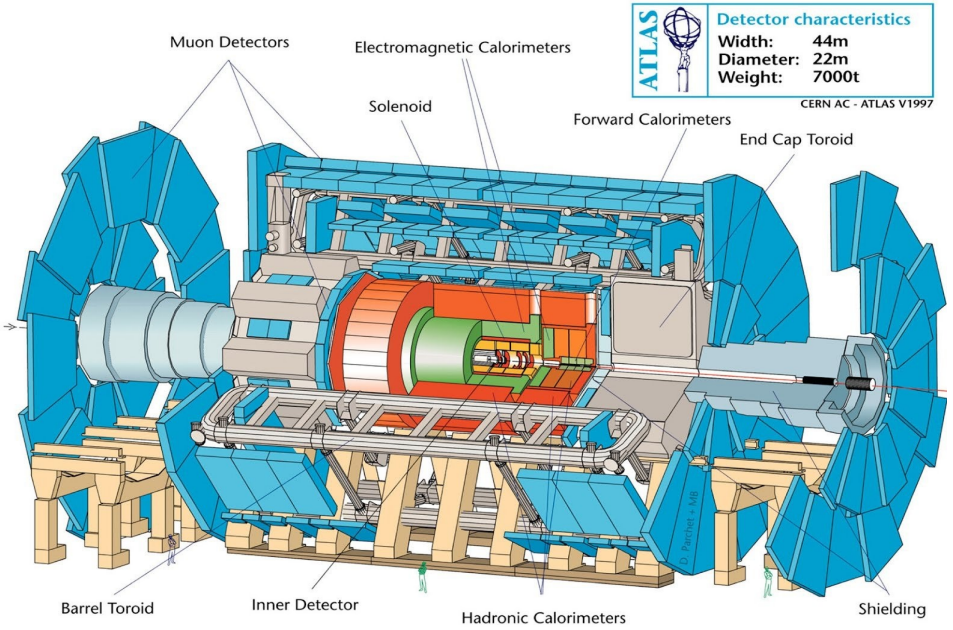
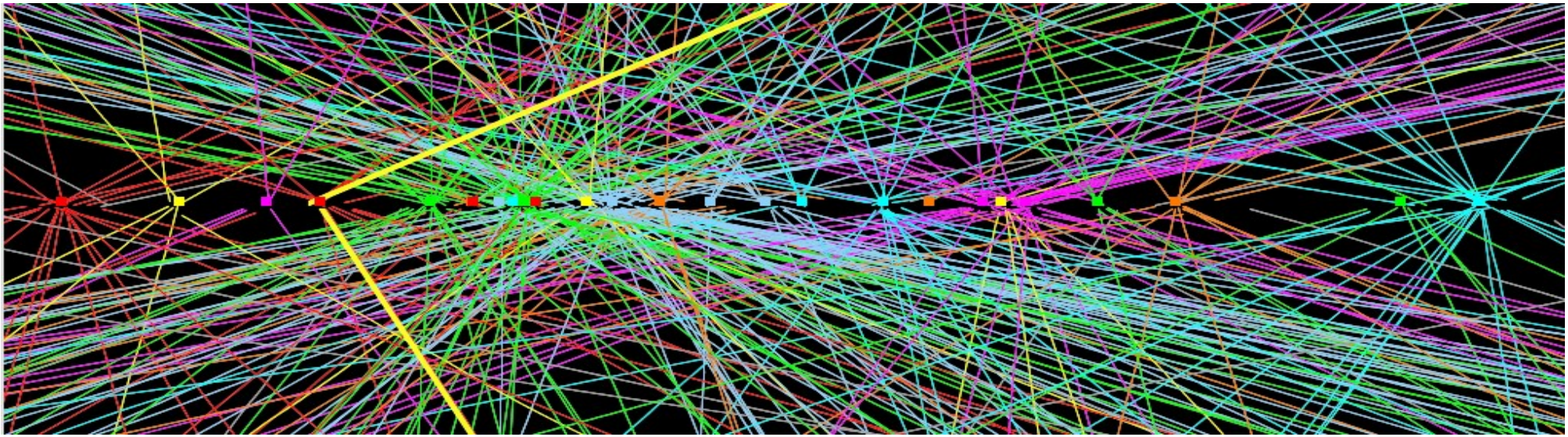
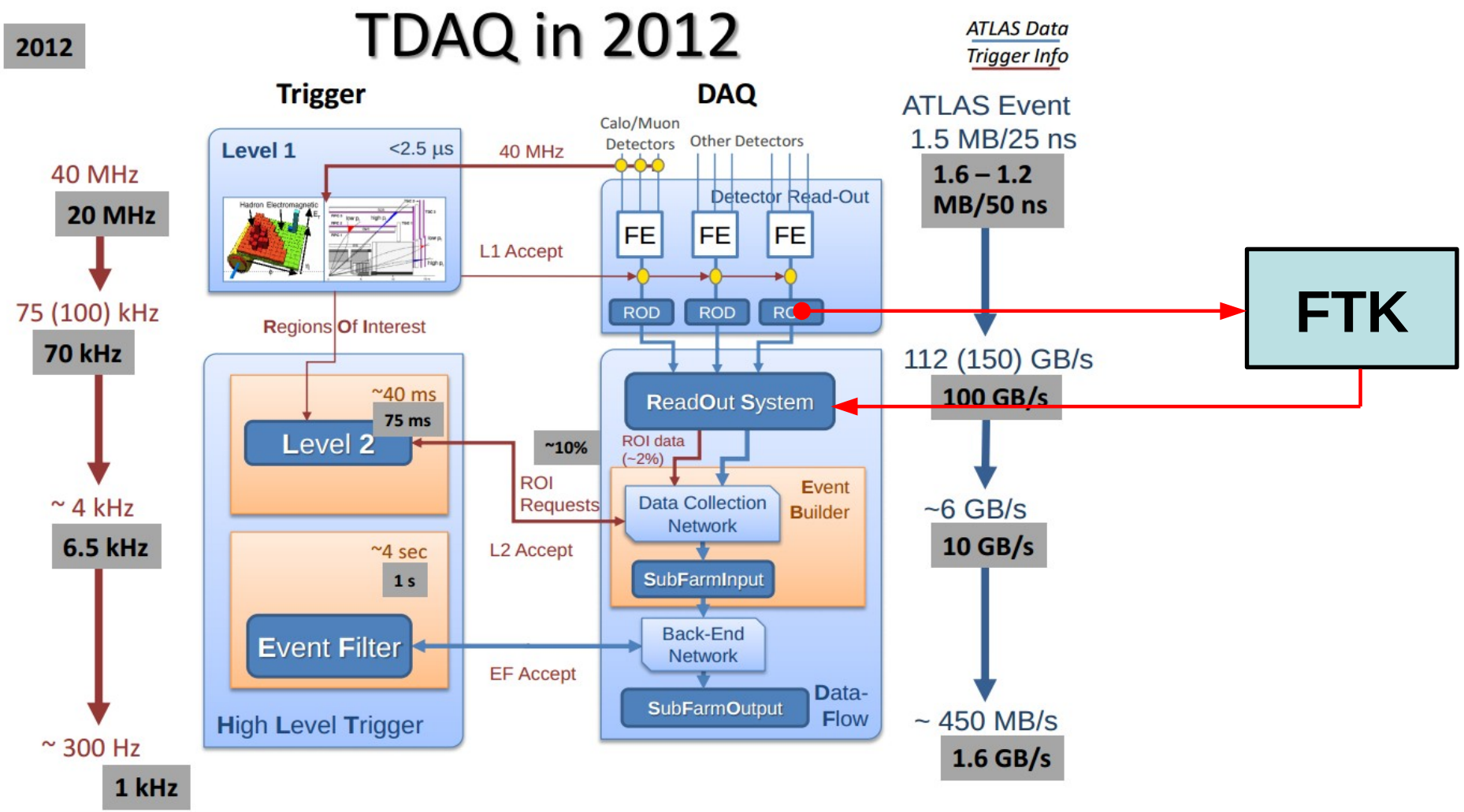


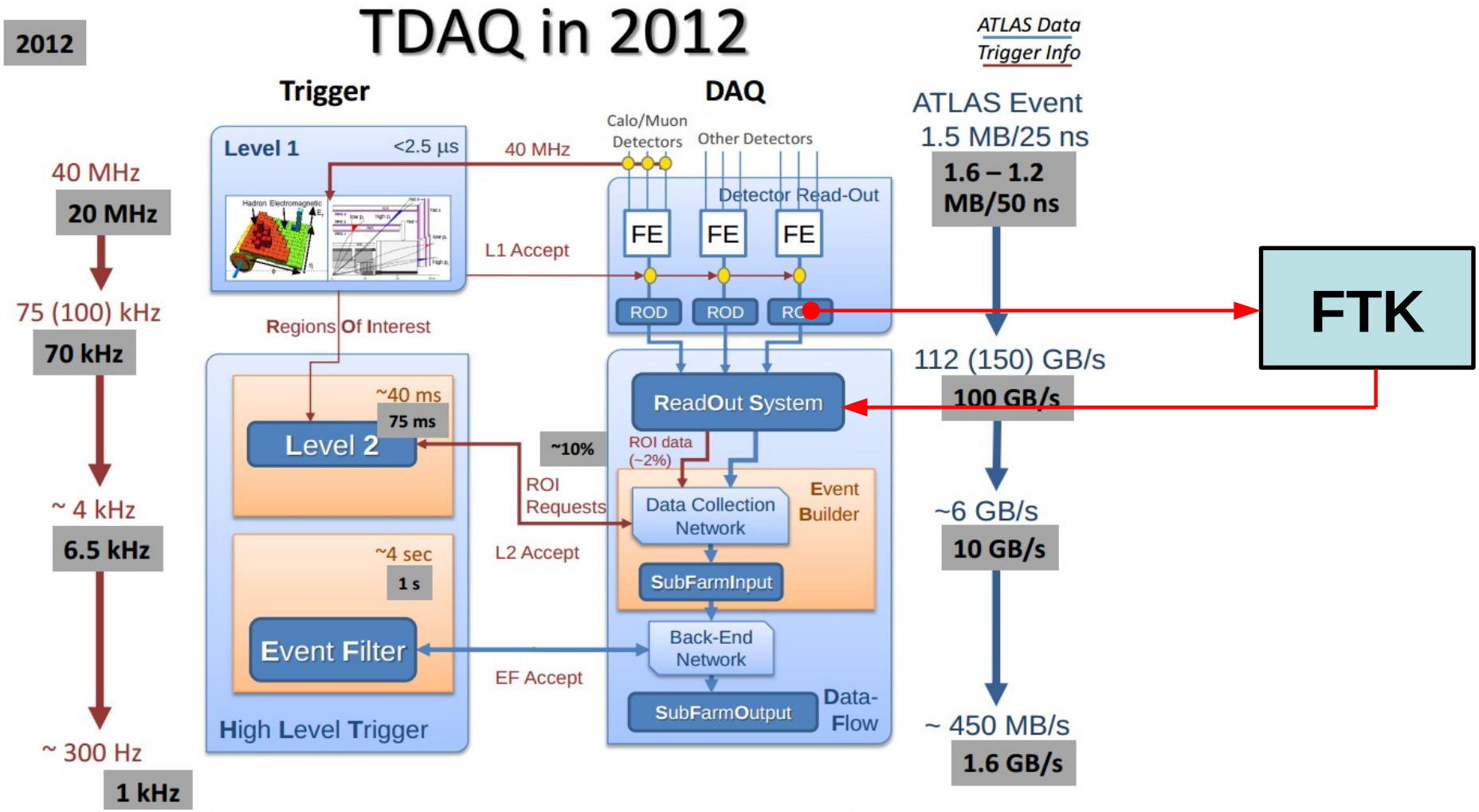


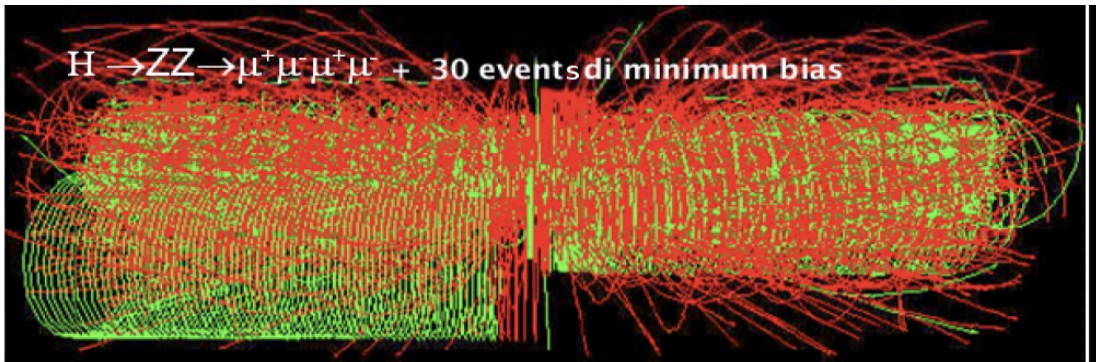
“1.5” Level Trigger processor

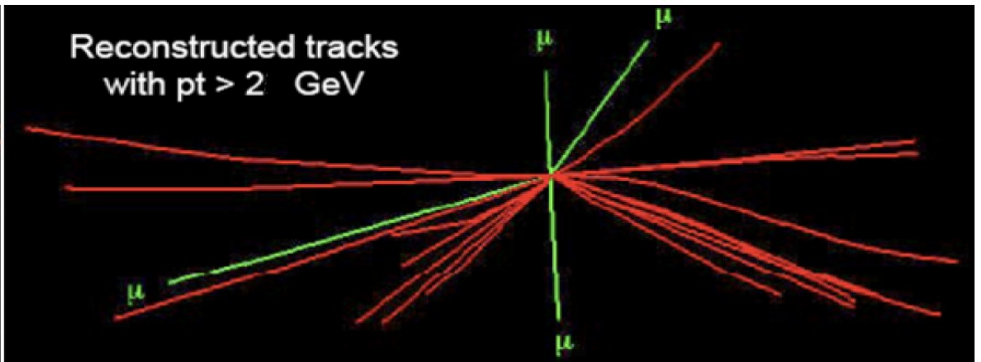


- Silicon data currently used only locally (ROI) and late in Level 2.
- FTK reconstructs all tracks with PT>1 GeV/c in time for Level 2.
- Track parameters are computed with full detector resolution.

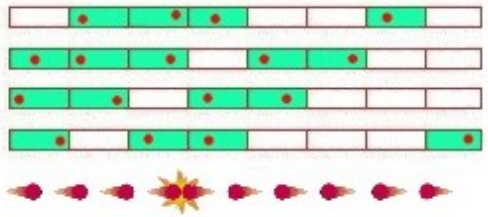
“1.5” Level Trigger processor

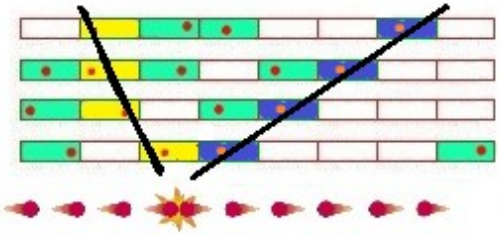






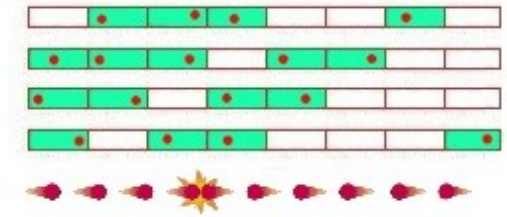
Pattern matching & track fitting

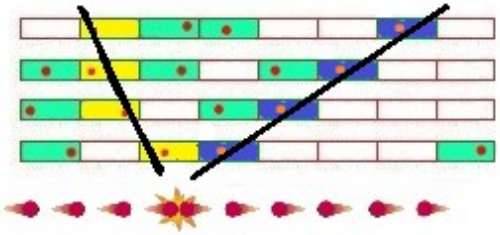


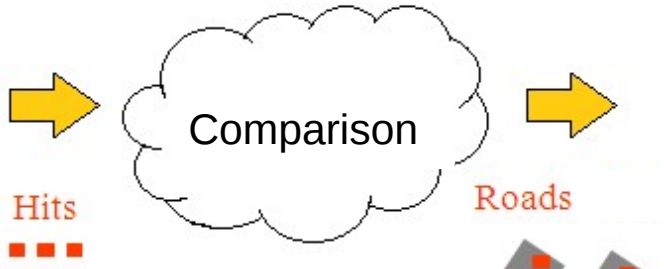


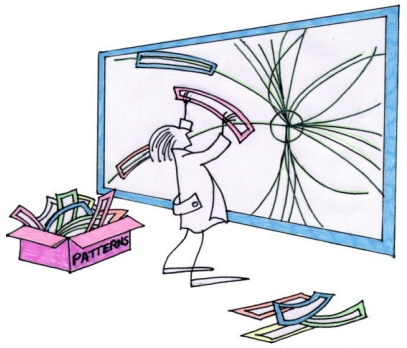
- Pattern Bank: All the possible patterns (low resolution real track candidates) are precalculated and stored in the Pattern Bank.

Pattern matching









Road = Low resolution Track

- Pattern Bank: All the possible patterns (low resolution real track candidates) are precalculated and stored in the Pattern Bank.
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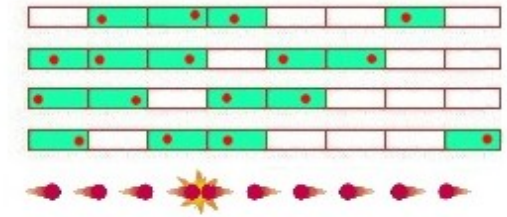
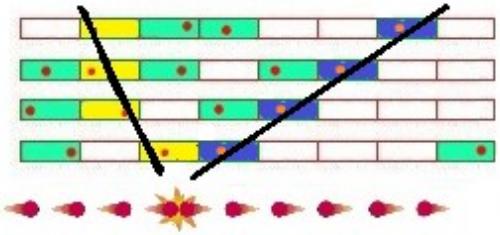
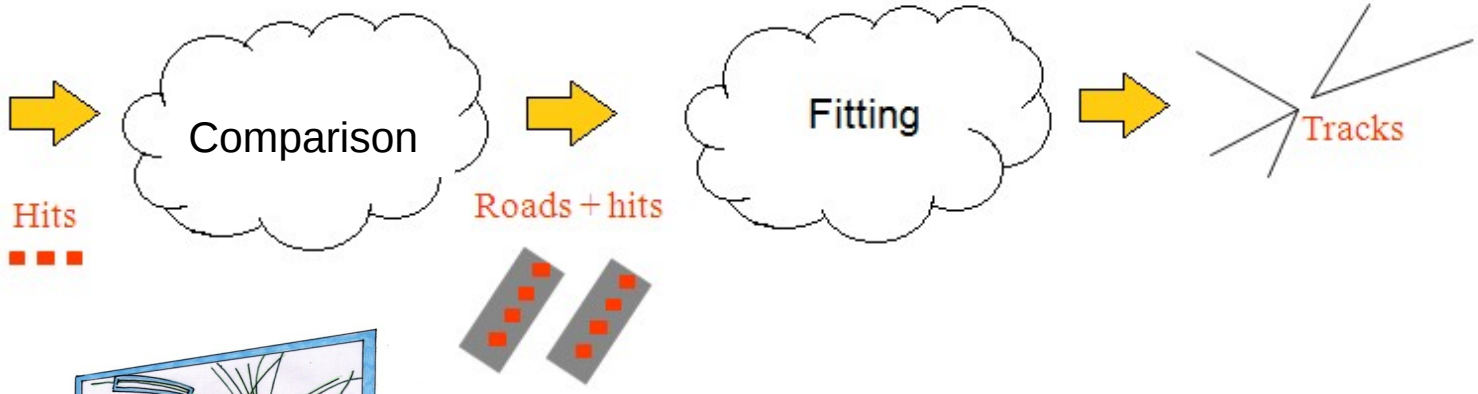
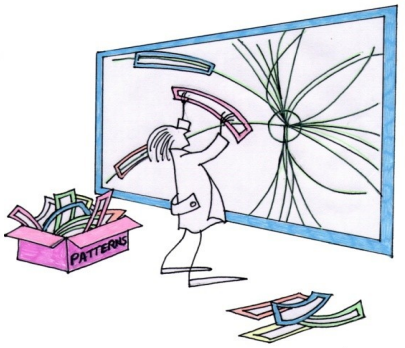
Pattern matching









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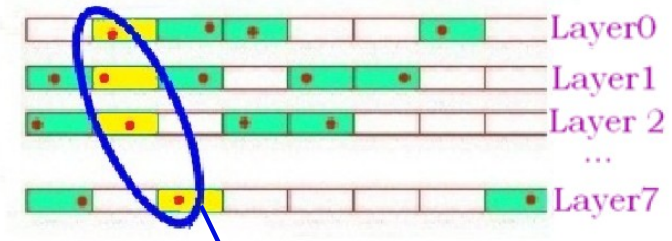
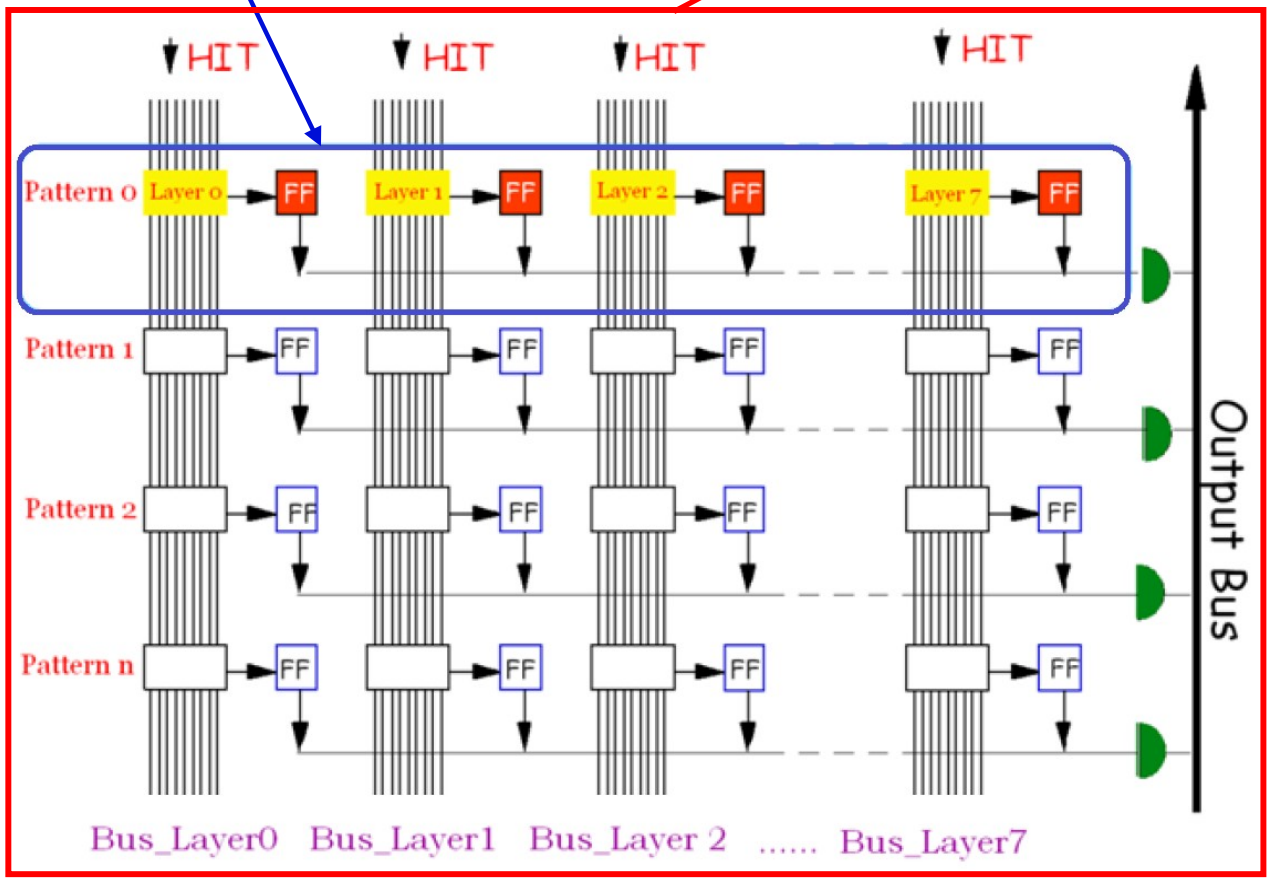
- Track Fitting: Fits of the full resolution silicon HITs contained in each ROAD determine particle tracks parameters.

Associative Memory

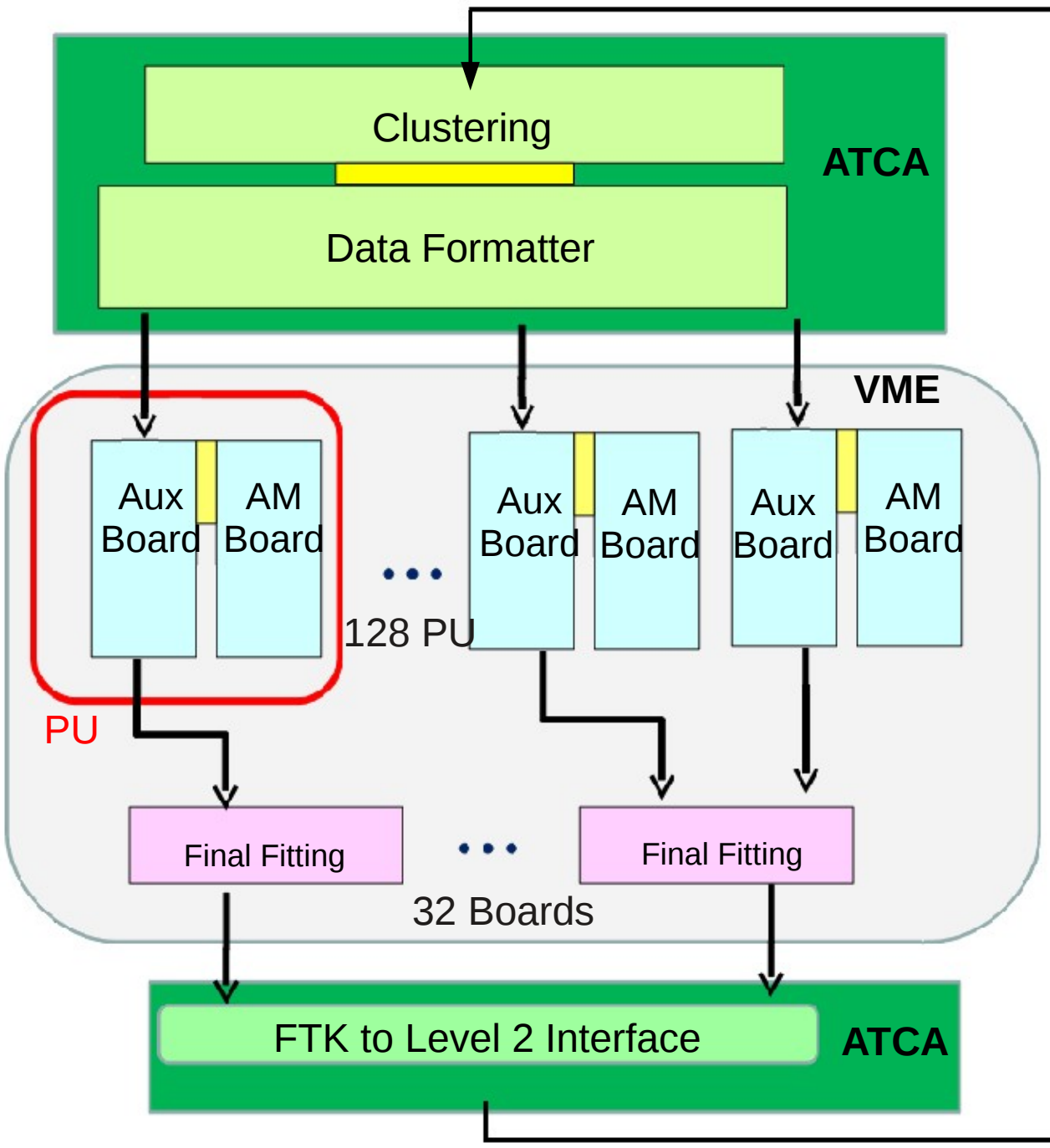


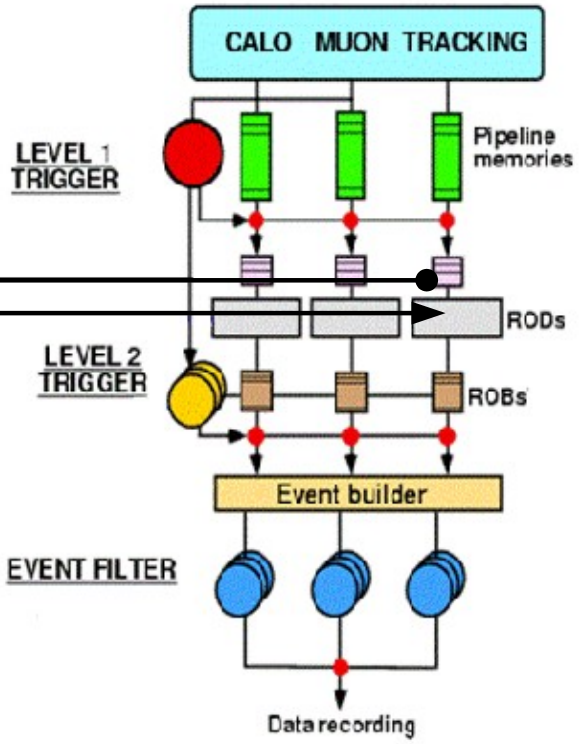


AMchip

- Custom Associative Memory
- Base element of Pattern Bank
- 1 Pattern stored in 1 row
- Data from 8 silicon layers flow separately on 8 parallel buses (vertical lines)
- Programmable matching threshold
- Matched pattern's addresses are read-out

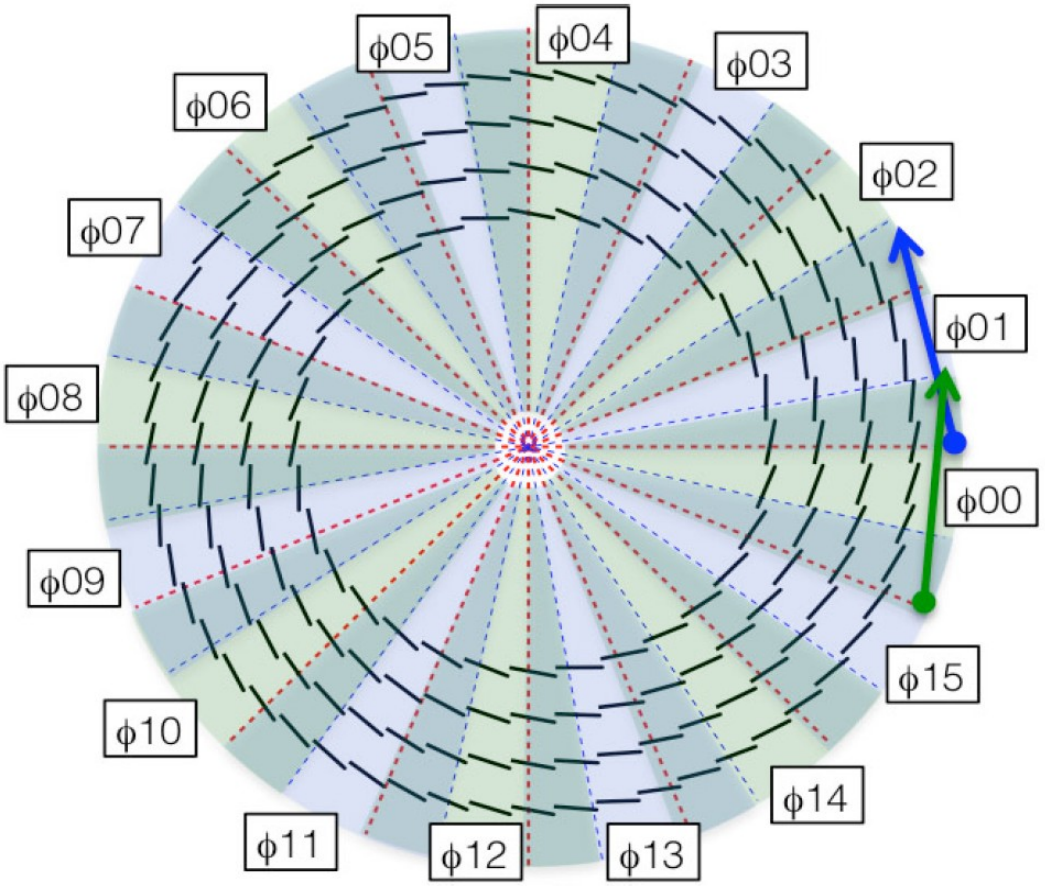
FTK architecture





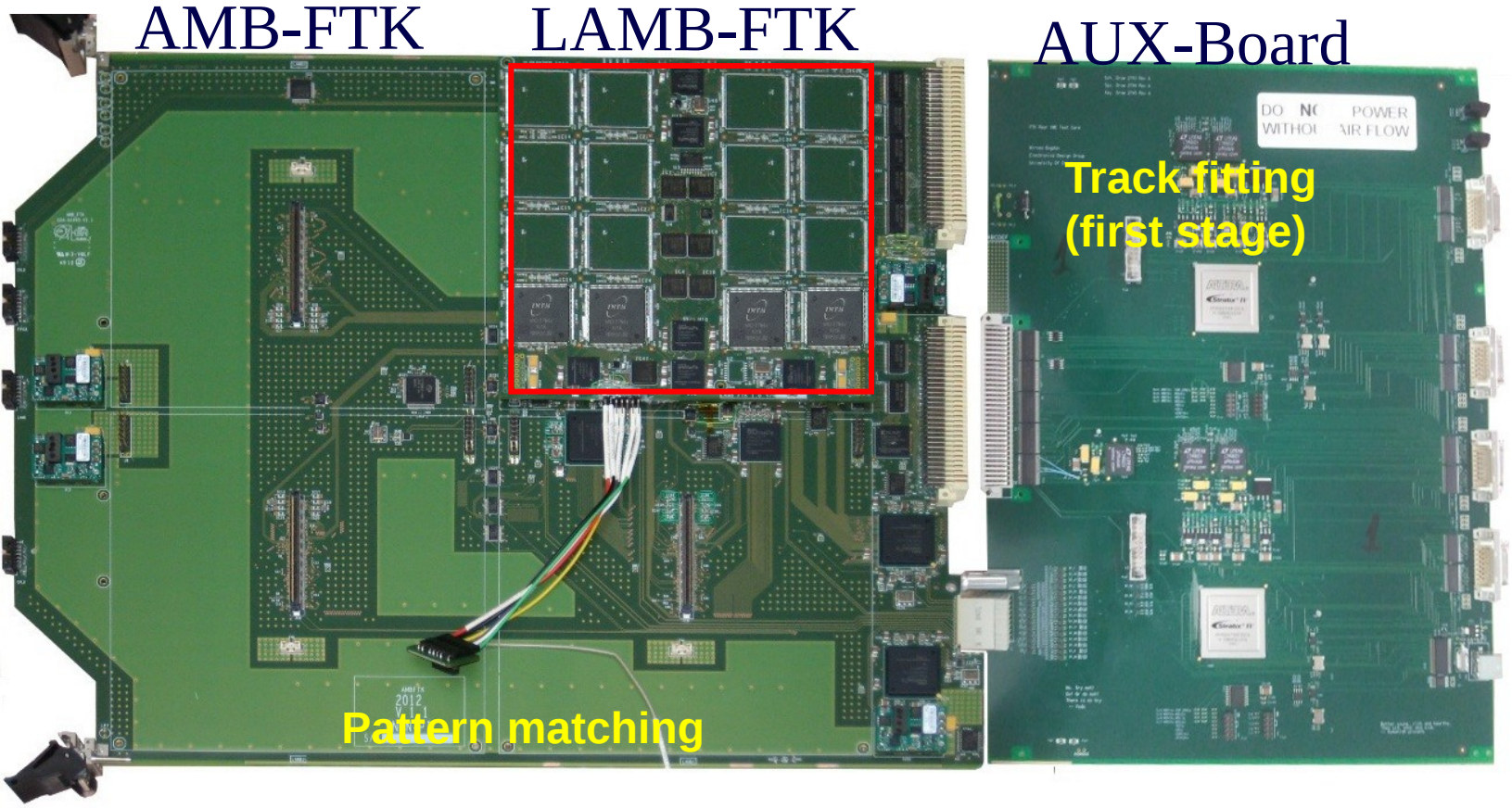
- FTK processor: 8 VME Crates
  5 ATCA Crates
- Processing Unit: track reconstruction core
- 128 Processing Unit:
  ~1500 FPGAs
  ~8200 AMChips

Splitting the silicon detector in 64 η-Φ towers



- FTK is organized in 64 η-Φ towers.
- 4 η sectors times 16 Φ sectors.
- The blue and green arrows is an example of overlap coverage.

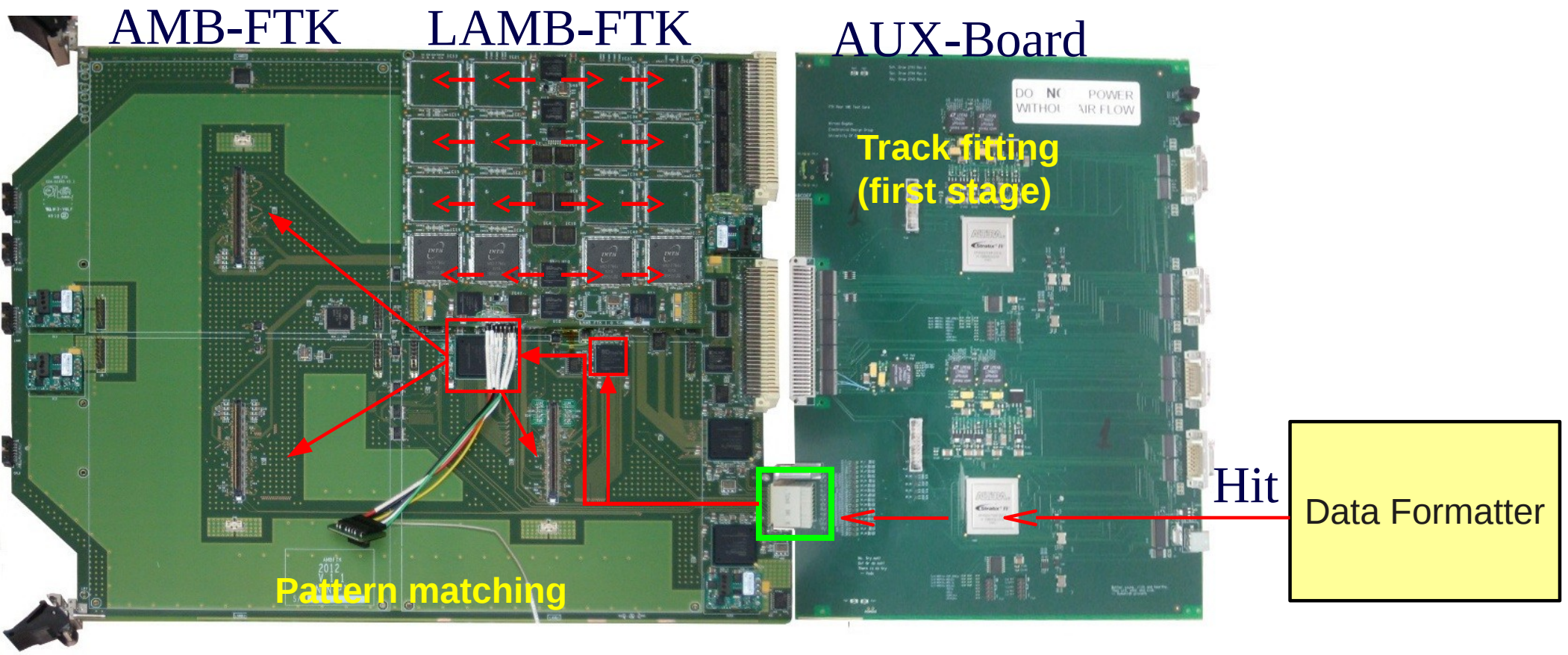
FTK Processor Unit



- Processing Unit: 9U VME board (AMB-FTK) + large Rear card (AUX Card) + 4 little mezzanines (LAMB-FTK).
- Silicon HITs relative to events accepted by Level 1 are distributed to all Amchips, this is done in parallel for the 64 tower (1 tower =128 AMChips).

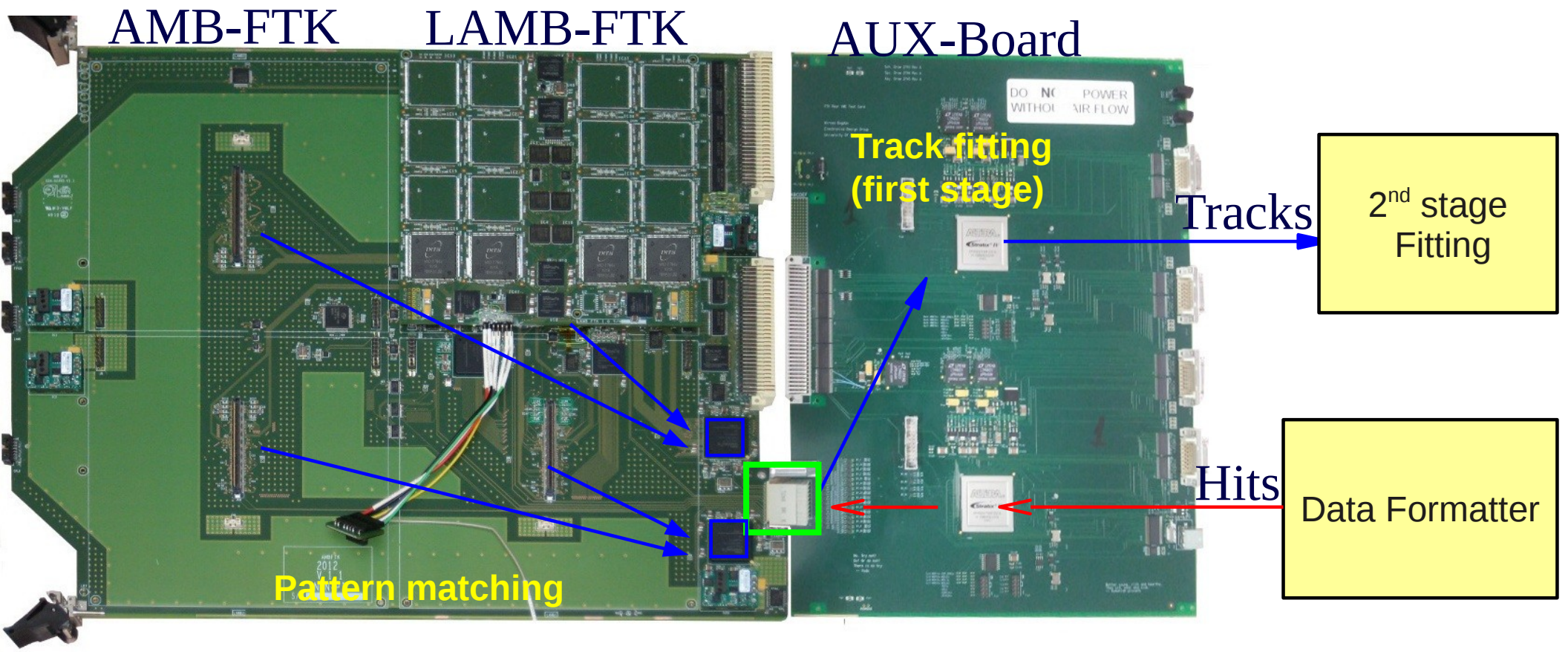
- 1 HIT is compared with ~ 8million of Precalculated pattern.

FTK Processor Unit



- Data from Data Formatter are distributed by 12 2Gb/s serial links from Data Formatter to the Input FPGAs on the AMBoard.
- Through 4 LAMB connectors to all AMchips.

FTK Processor Unit

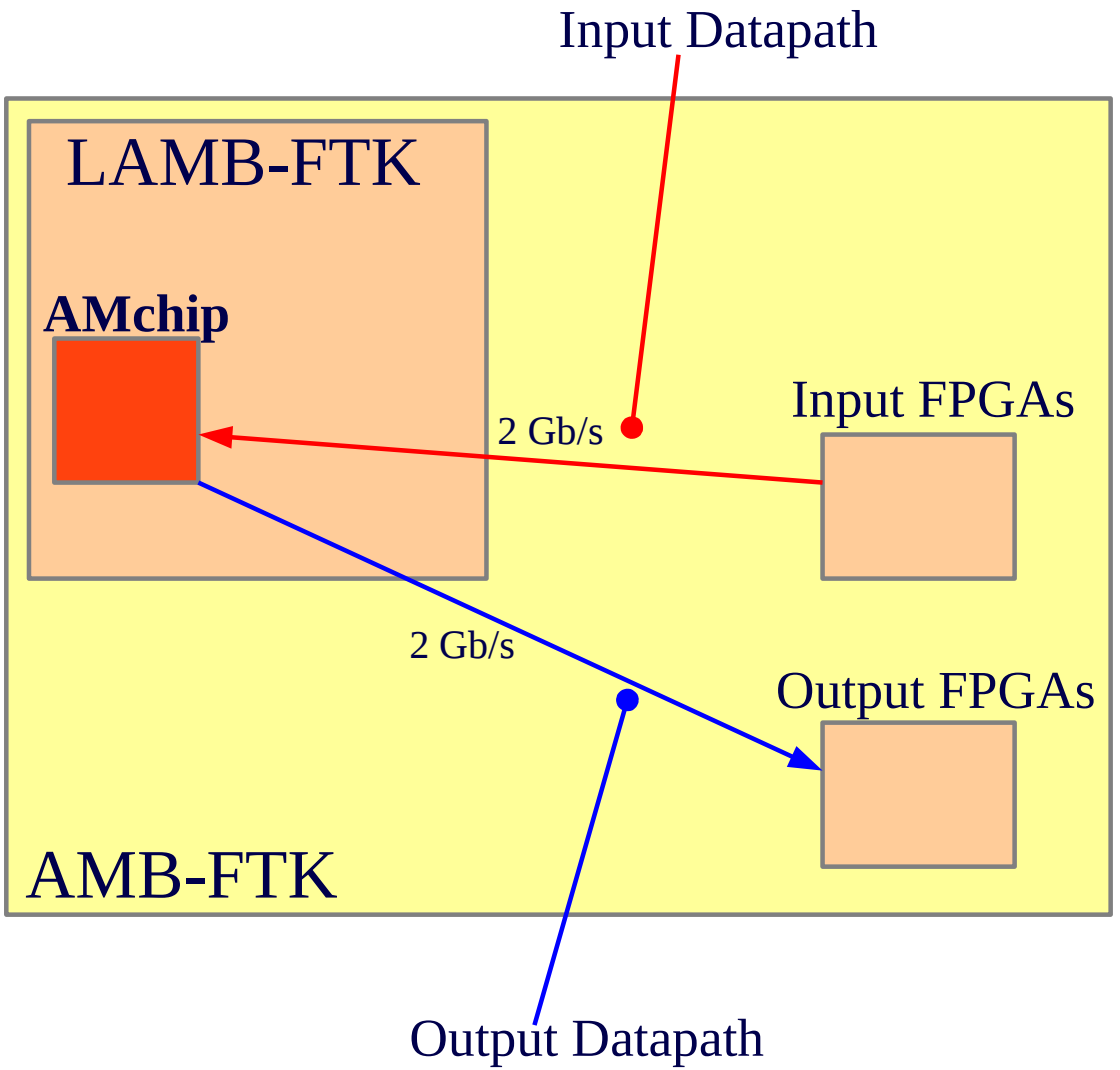


Matched ROADs:

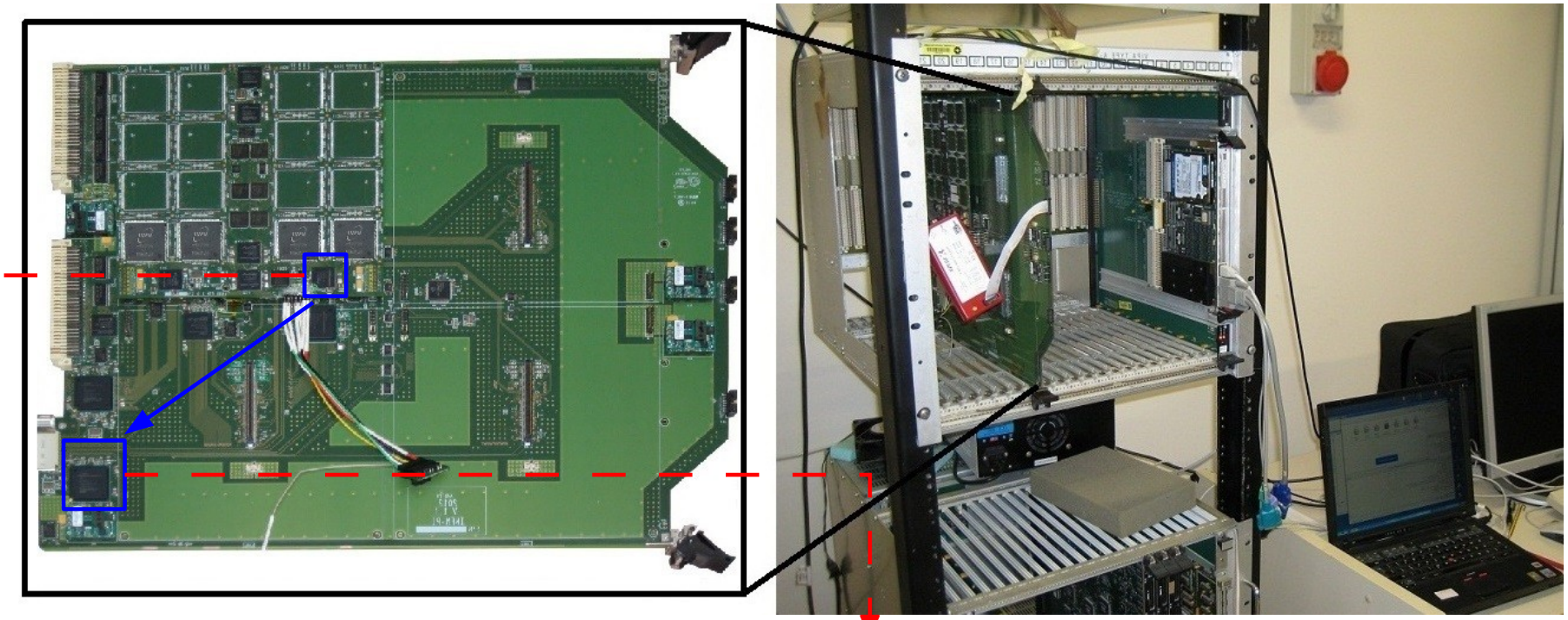
- Collected on the AMB-FTK by 2 Output FPGAs (Blue squares).
- Transmitted to the AUX Board through 16 high-speed links (2Gib/s).

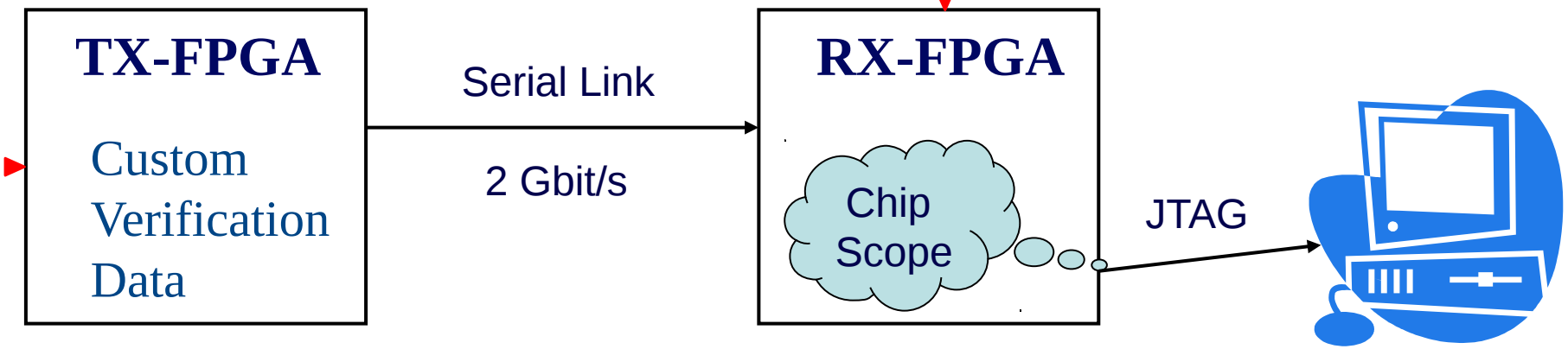
Prototype Tests

- Test Input Links & FPGAs to correctly send HITs to AM chips.
- Test Output Links & FPGAs to correctly collect the ROADs.
- Test the pattern matching.



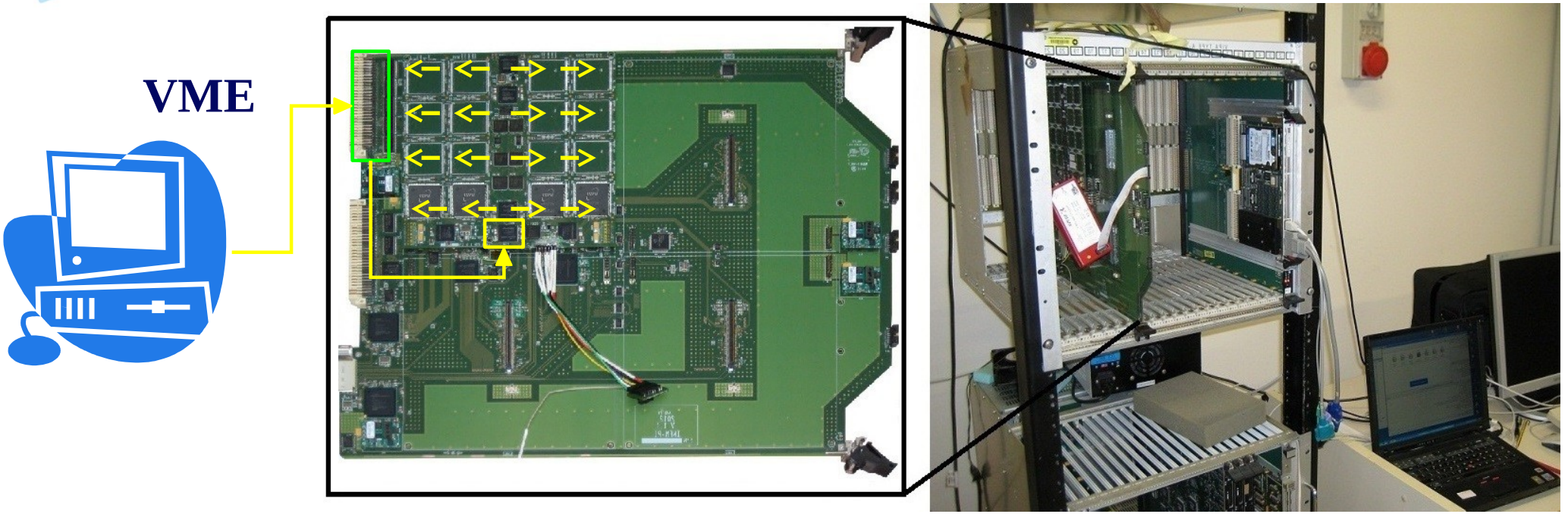
Test direct links: Hit input and Road Output





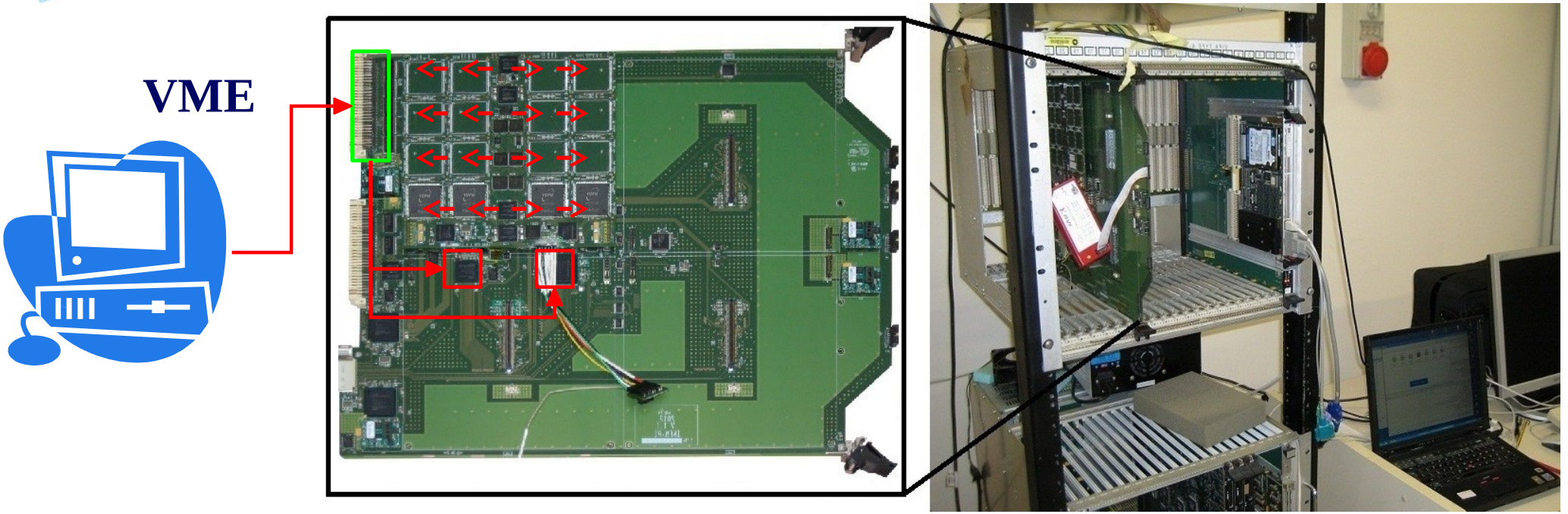
- Sent a known pattern of data from TX and check it in RX with Logical Analyzer.

Test pattern matching: Store Pattern Bank



- Step 1: Store precalculated Patterns into Associative memory chips:
  - Through VME the data are stored in the AM by FPGA (yellow arrows)

Test pattern matching: Send INPUT



- Step 1: Store precalculated Patterns into Associative memory chips:
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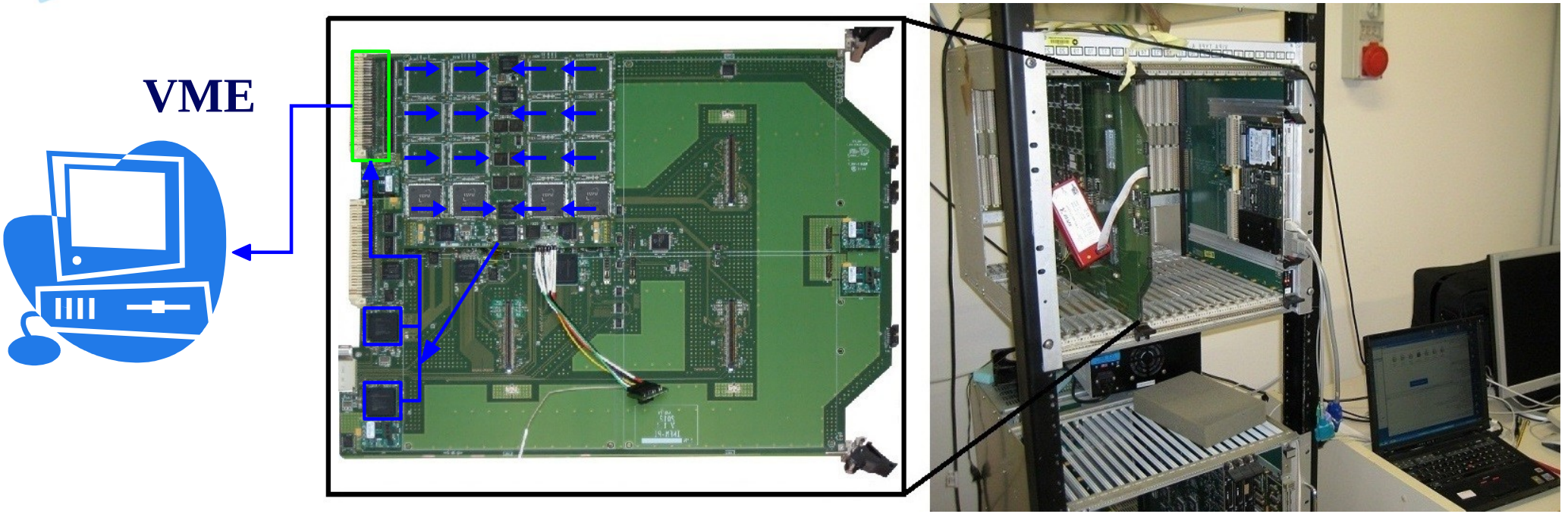
- Step 2: Simulate silicon HITS Input:
  - Silicon HITS Input are loaded into the inputs FPGAs memory (red square) through VME.

Test pattern matching: Check OUTPUT



- Step 1: Store precalculated Patterns into Associative memory chips:
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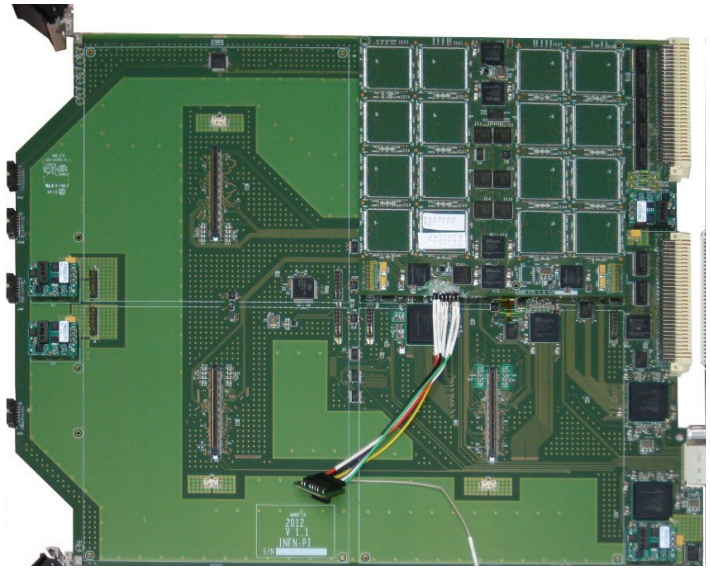
- Step 2: Simulate silicon HITS Input:
  - Silicon HITS Input are loaded into the inputs FPGAs memory (red square) through VME.
  - The FPGAs transimits data to he LAMBs at full speed.
- Step 3: Check pattern matching:
  - Collect ROADs in the Output FPGAs (blue squares).
  - Compare Hardware and Simulation output.

Cooling Tests



Expected power consumption
1 Processing unit ~ 300 Watt.

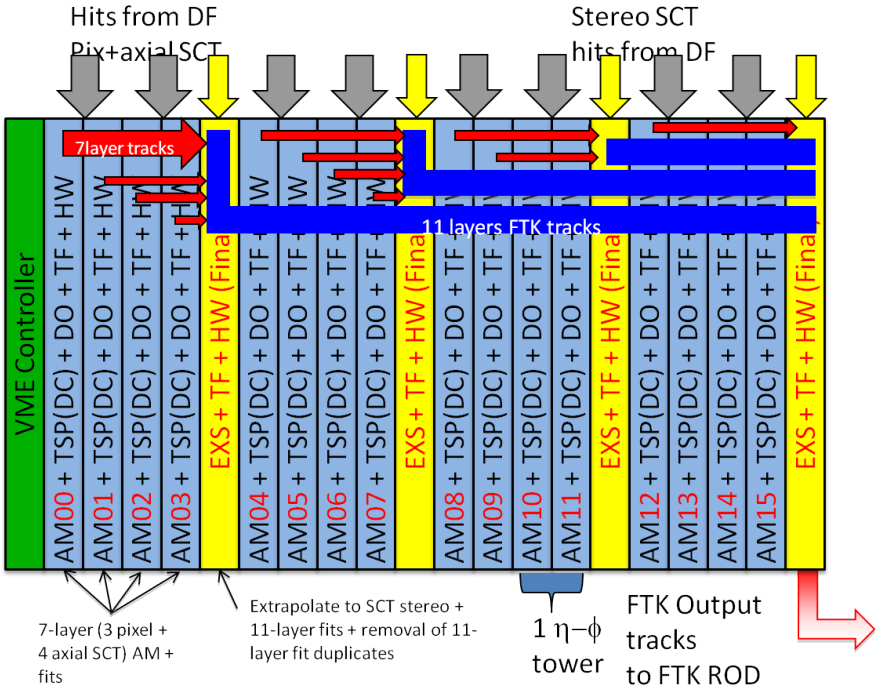
16 PU per crate (plus SSB, CPU)

~ 5 kW per crate.

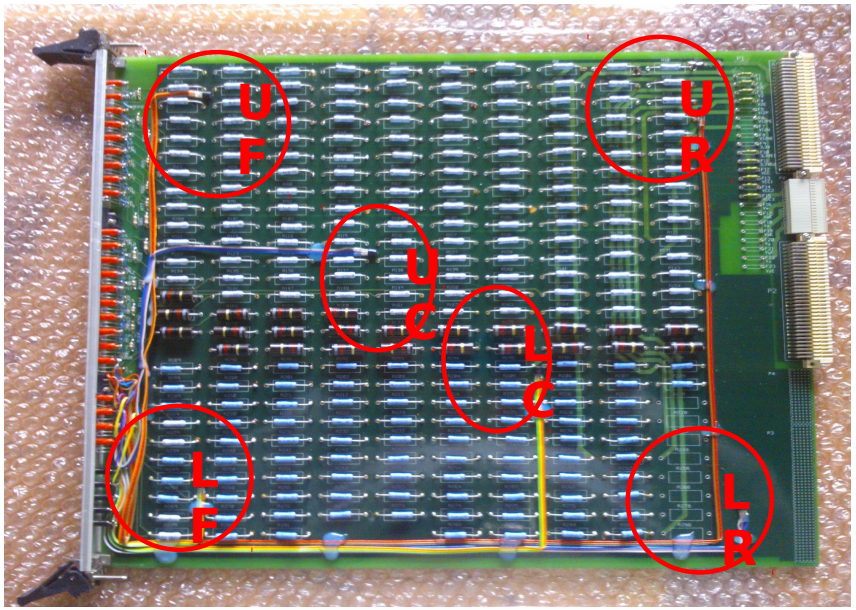
Need Cooling test!

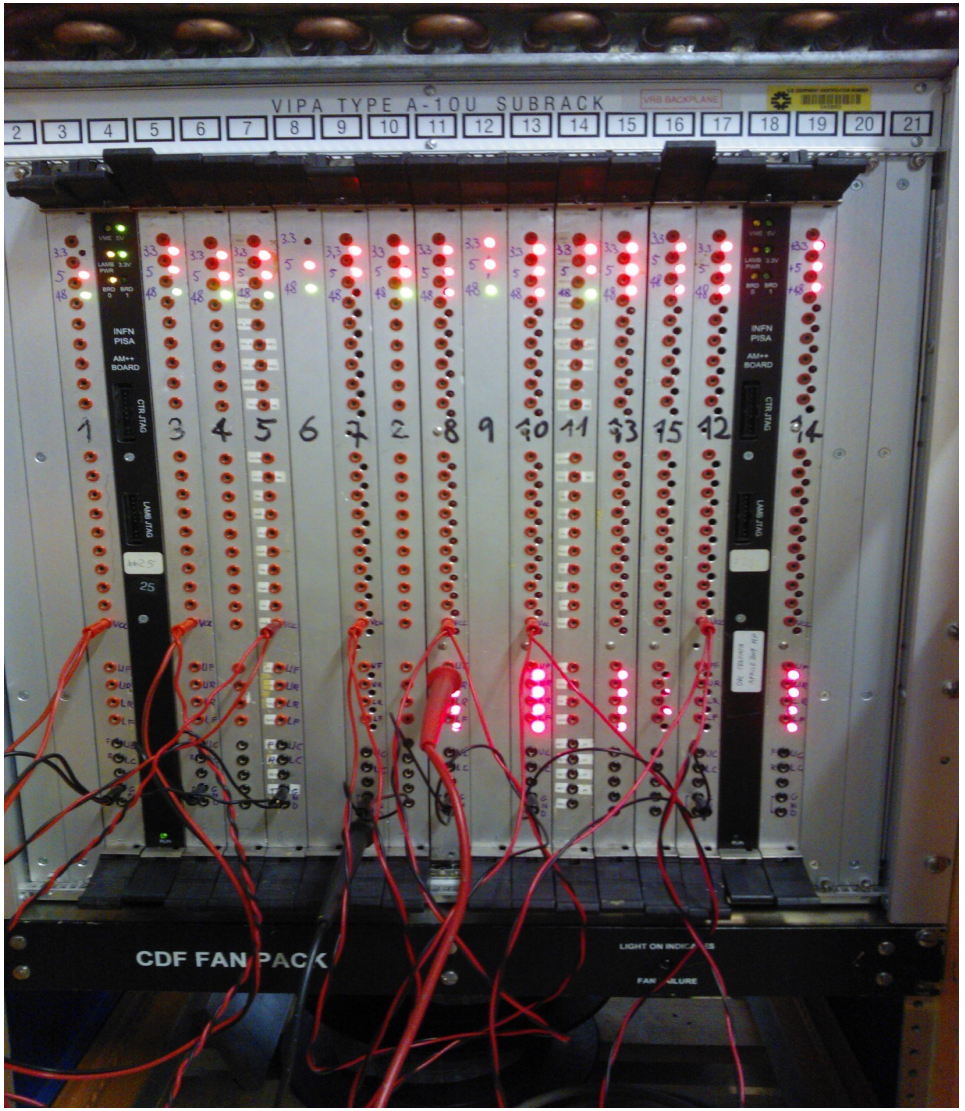
Power supply voltages:

- 5V
- 3,3V
- 1,2V



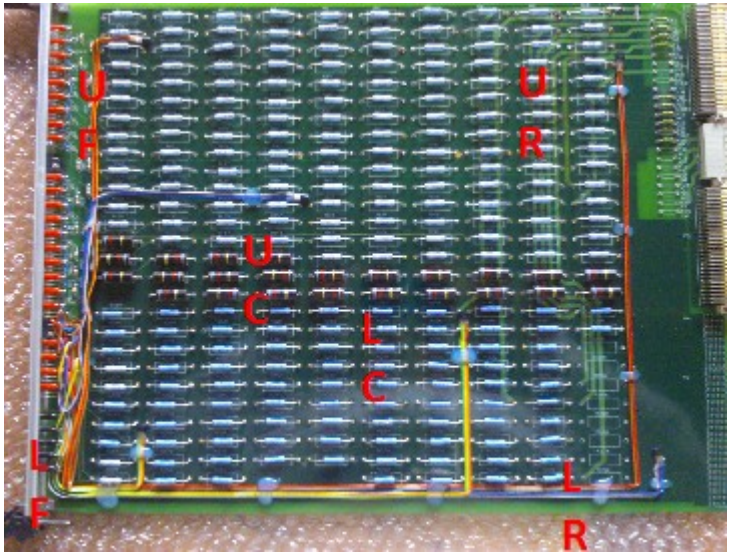
Cooling Tests without chiller

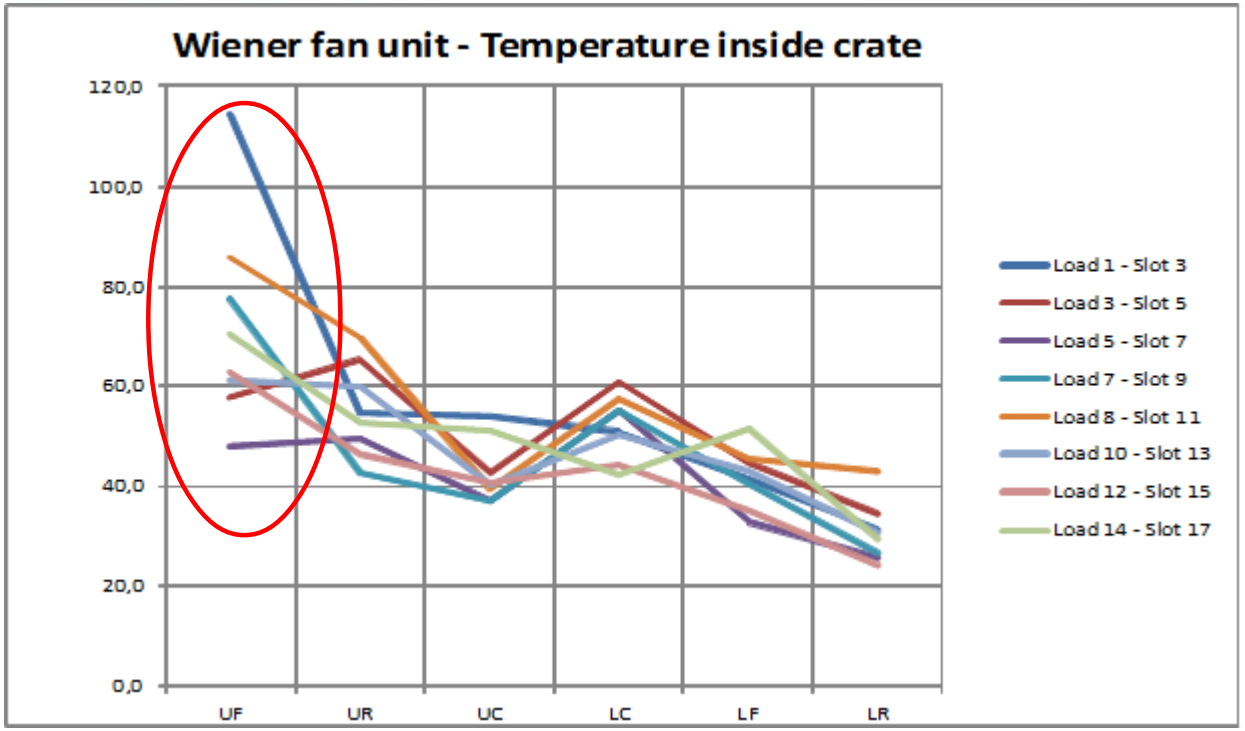




- Cooling test work in progress
  INFN PAVIA.
- Power consumption simulated with resistors.
- Six sensor used to measure the temperature in the crate (red circles)

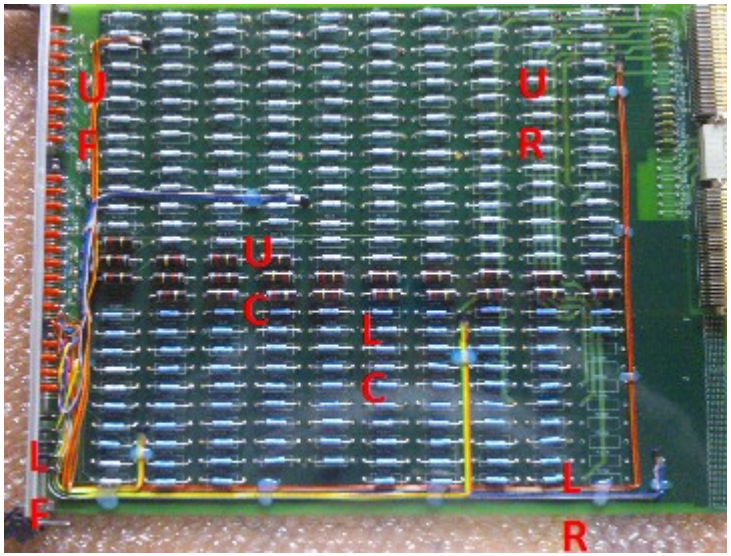
Cooling Tests Result with Wiener Fan

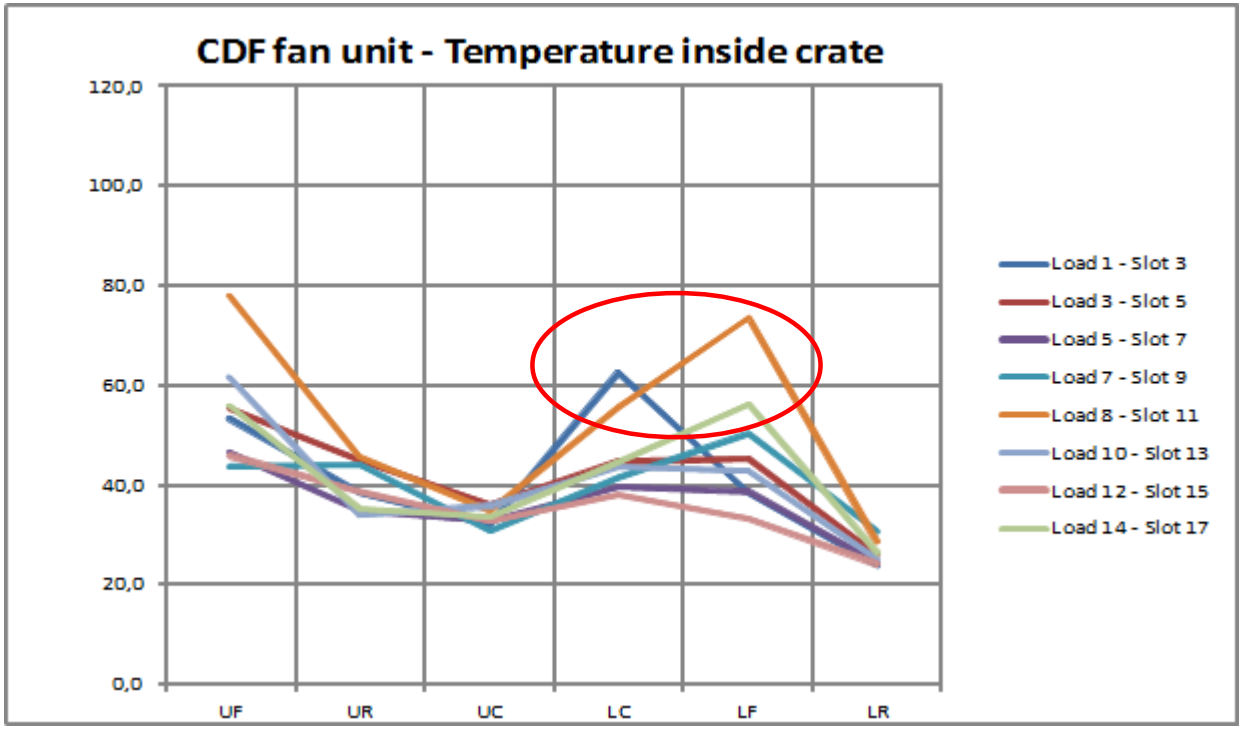




- With the Wiener Fan we have a peak of temperature in the up side of crate.
- The reason is the power of the fans.

Cooling Tests Result with CDF Fan





- With CDF Fan the temperature is lower but there is a peak in the down front side of crate.
- The reason is the missing fan.
- Cooling test are in progress:
  next step is to resolve the problem with fans and use the chiller.

Conclusion

- AM system test results were excellent.
- Cooling test are in progress.
- Now we are improving the system for the final version.
- June 21, 013: ATLAS Collaboration approved the FTK Technical Design Report.
- We will install the system for the next LHC power on, in 2015.

Thank You!

Backup