A new portable test bench for the ATLAS Tile Calorimeter front-end electronics certification

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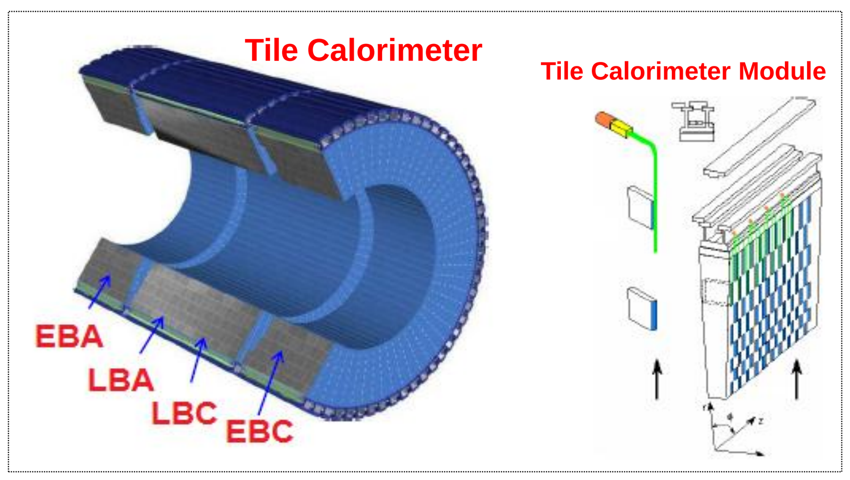
Tile Calorimeter

❖ Sub-detector of the ATLAS experiment installed at the Large Hadron Colider (LHC) of CERN.



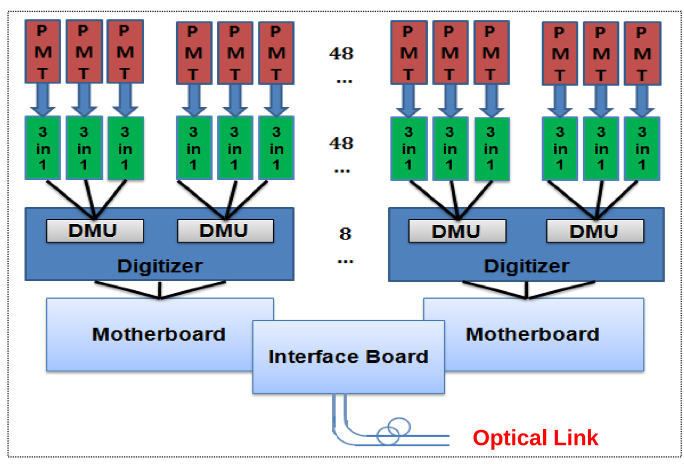
❖Sampling Calorimeter: Steel as absorber and scintillating tiles as active material.

❖ Read-out divided in four cylindrical partitions: two central sections (Long Barrels LBA and LBC) and two endcaps at higher pseudorapidity (Extended Barrels EBA and EBC). Each partition is azimuthally segmented in 64 modules, and each module hosts up 48 photomultipliers (PMTs).

Front-end Electronics

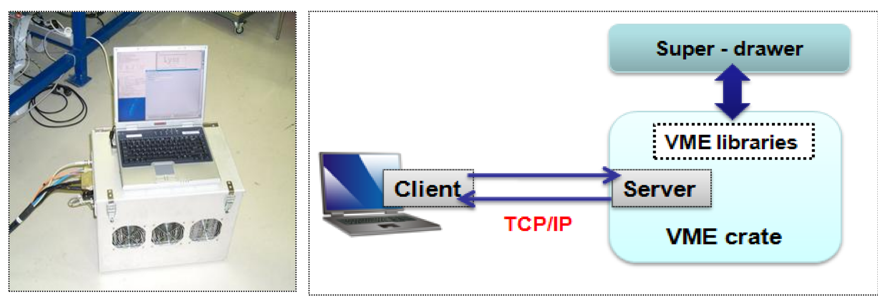
❖ A super-drawer include all the electronics required to perform a read-out of a complete module.

❖ The PMTs convert the light signals into electrical impulses, which serve as input signals of the 3-in-1 cards in the front-end electronics. These cards perform the conditioning and processing of those analog signals, before send them to the digitizer system. The digitizer system performs the required analog to digital conversion, implements pipeline memories, and includes a TTCrx chip for the Timing, Trigger and Control signals receptions. The digitized data from all the Digitizer boards are sent to the interface board, which is responsible to collect, serialize and transmit them to the back-end electronics using optical links.



Previous Version

❖ Contained in a custom aluminum box with dimensions of 50x33x41 cm and the total weight is about 20 kg.



❖ The aluminum box contains a VME crate hosting a set of electronics boards which provide all the functionalities required to control and test the front-end electronics of TileCal.

❖ The software is composed by two parts: The server running in a VME processor and a client running on a laptop.

Software	Function	Language/Platform
Server	Performs all the electronics tests under requests of the client, sends back the results to the client.	C under LynxOS
Client	Requests the server to perform the electronics tests and receive the results.	C++ under Linux

New Test Bench - MobiDICK 4

Motivation

❖ At the present time there are three available units. A fourth one is required for the long shutdown of 2013 to test the four barrels at the same time.

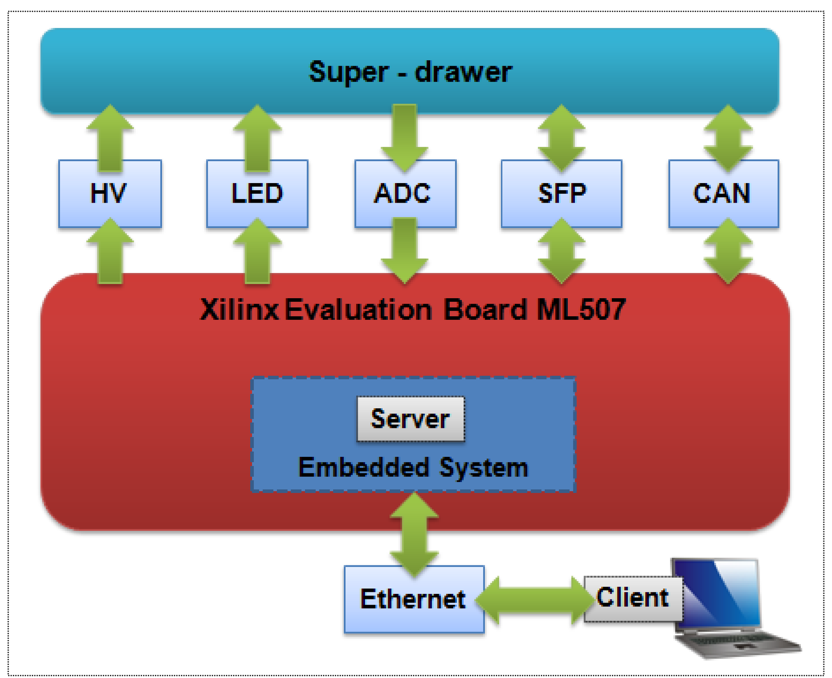
❖ There is no replacement for some old VME modules.

❖ Aim for a reduction of size with a total weight.

❖ Evaluation of new technologies for future upgrades.

Architecture

❖ An embedded system, some programmable logic and custom electronic boards replace the functionality of the VME modules of the previous system.



The Motherboard

❖ The Motherboard is a Xilinx ML507 evaluation platform, equipped with a Virtex-5 FPGA.

❖ Patform's resources:

❖ PowerPC 440 RISC microprocessor

❖ 4.25 Gbps GTX transceivers

❖ 10/100/1000 Mbps ethernet

❖ 256 MB of DDR2 RAM

❖ Configuration storage, such as platform flash devices or a Compact Flash card-based system configuration controller (System ACE Controller)

The Embedded System

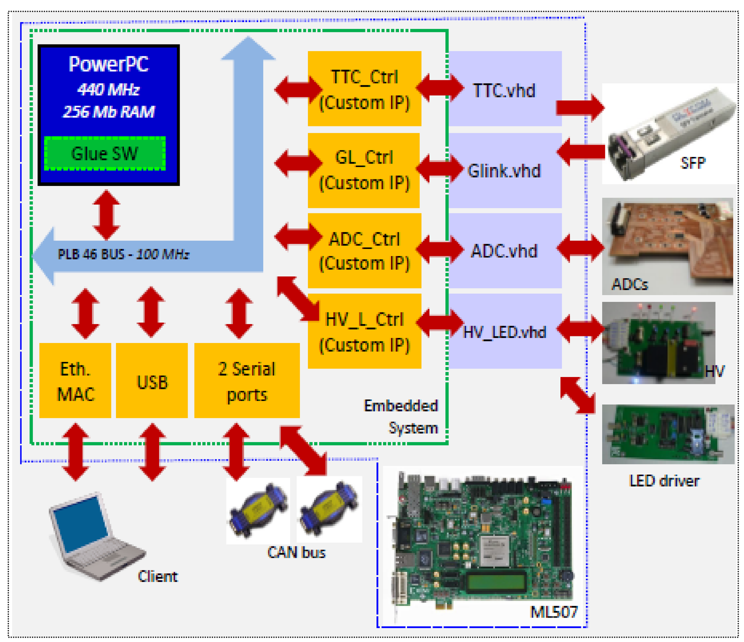
❖ Implemented in the Virtex-5 FPGA available on the motherboard.

	Function	Microprocessor	Bus	Peripherals
Embedded System	Runs the server software (electronic tests to super-drawer)	PowerPC 440 MHz	Processor Local Bus 4.6	Commercial/Xilinx IP cores/Custom IP cores

❖ Operating System: Busybox Linux version with kernel 2.6

❖ An automatic boot of the whole system (bitstream + kernel + root file system): from the Compact Flash using the System ACE Controller.

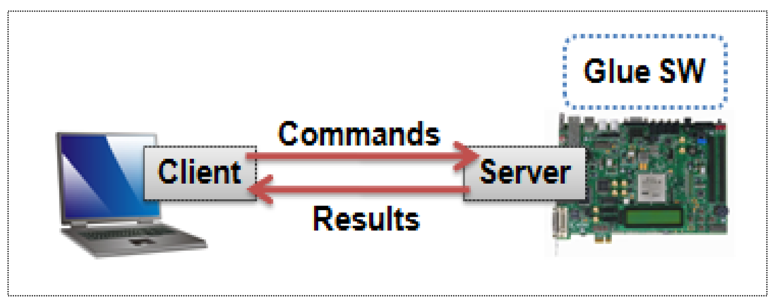
❖ The ELDK 4.2 (Embedded Linux Development Kit) cross compiler tools: building the Linux OS image and for developing the applications.



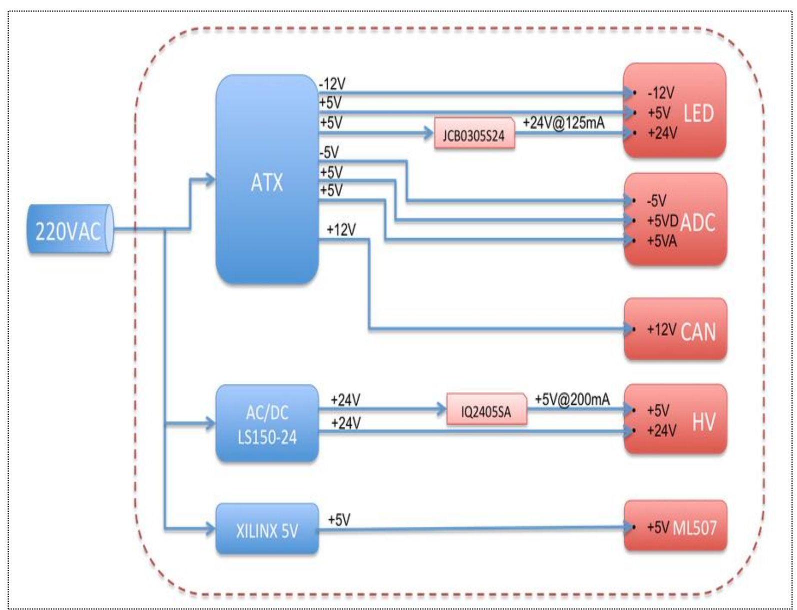
The Software

❖ The software of the MobiDICK4 has a client-server architecture.

❖ A glue software replaces the VME libraries from the previous system.



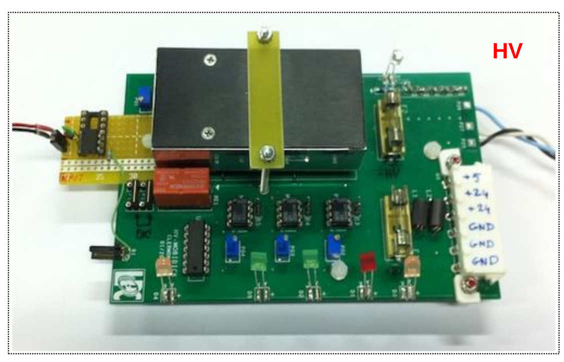
Power Supply Distribution



HV and LED Boards

❖ **HV board:** provides a -830 V power supply to the PMTs of the super-drawer.

❖ **LED board:** provides a 20 V pulses required to calibrate the readout channels of the super-drawer.



ADC Board

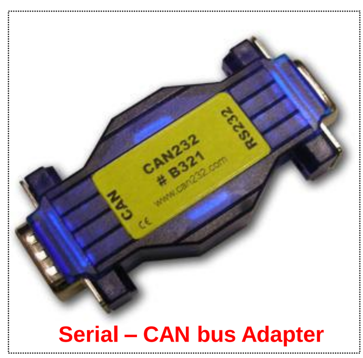
❖ Digitizes analog trigger outputs of the super-drawer with a 40 MHz local oscillator.

SFP Module

❖ Small Factor Pluggable transceiver that provides communication with the interface board of the super-drawer.

CAN Bus

❖ Two commercial adapters and a custom cable is used to convert the RS232 ports of the motherboard to the CAN bus interface of the super-drawers.



Mechanics, Assembly and the First Prototype

❖ **Size**: 35 x 40 x 20 cm

❖ **Weight**: about 4 kg

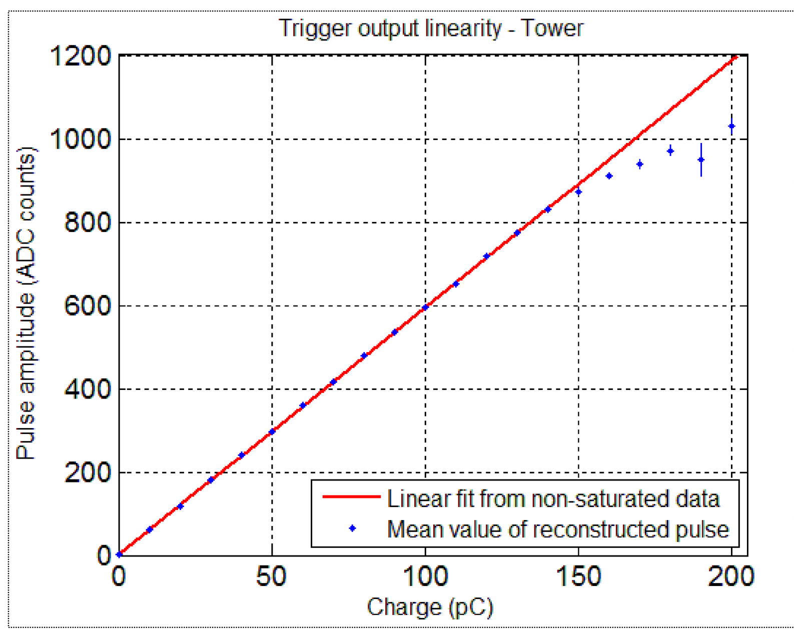
❖ A LCD 16x2 display: mounted in the external part of the box to present the status of the system to the operator.

MobiDICK Tests

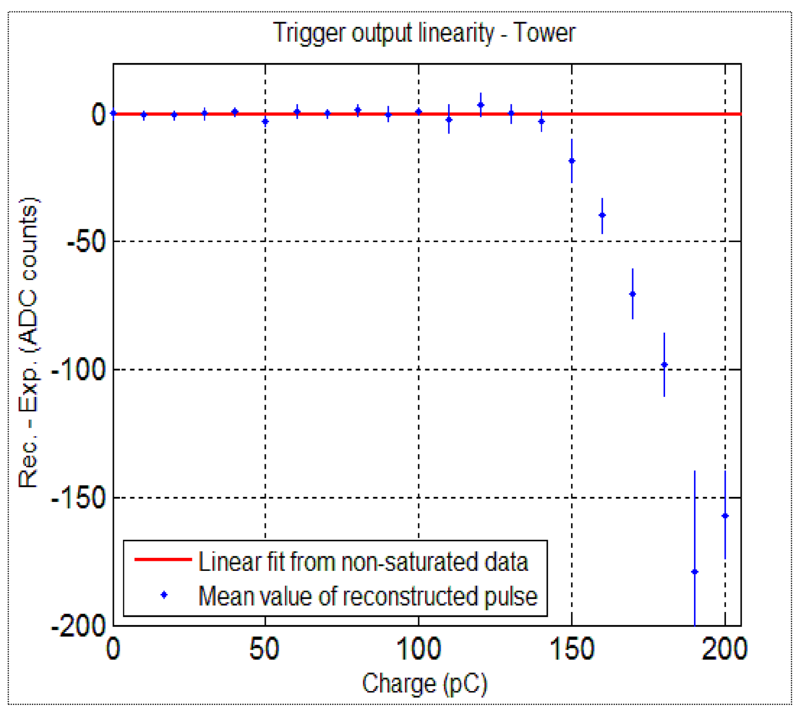
ID	Description	TTC	Glink	CAN	HV	LED	ADC	Status
CommMB	Communication with MB CAN			x				Working
CommHV	Communication with ADC CAN			x				Working
Adder	Trigger tower injection test	x					x	Working
DigCHK	Data integrity test	x	x					Working
DigShape	Charge injection test	x	x					Working
DigShapeLED	LED test	x	x			x		Working
Noise	Noise test	x	x					Working
NoiseHV	Noise test with HV	x	x		x			Working
Integrator	Integrator read-out test	x		x				Working
IntegratorHV	Integrator read-out test with HV	x		x	x			Working
HVon	Turn on HV				x			Working
HVof	Turn of HV				x			Working
Opto	Communication with optocoupler			x				Working
NominalHV	HV regulation test			x	x			Working
LEDon	Turn on LED					x		Working

ADC Board Results

This plot shows the response measured by the ADC board in ADC counts versus the injected charge in pC. The ADC board is capable of reconstructing signals up to 200 pC from the tower signals from the super-drawers.



The plot below shows the difference between the reconstructed response and the expected response extracted from a linear fit to the data of the previous plot. The deviation is of the order of 10% for charges below 200 pC which is within the specifications of the tests.



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