AIDA

Advanced European Infrastructures for Detectors at Accelerators

Deliverable Report

PRODUCTION OF DEDICATED SENSORS

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AIDA

Advanced European Infrastructures for Detectors at Accelerators

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DELIVERABLE REPORT

PRODUCTION OF DEDICATED SENSORS

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Abstract:

Dedicated sensors to be used with special ASIC for 3D interconnection will be produced and become available in time.

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Delivery Slip

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Executive summary

The master plan for the production of demonstrator sensors in 3D technology has been created.

Several subprojects have been defined, each using a different approach of 3D technology and working with different industrial partners.

The subprojects sample technological approaches which range from 'mature' (available for production at low risk without important R&D, however with moderate performance) to 'challenging' (need of R&D with high risk, but having the potential to reach superior performance). Thus a knowledge pool of different technologies and their respective usefulness and potential for HEP applications will be created.

The partners of this work package are grouped into the different subprojects allowing an efficient use of resources.

1. INTRODUCTION

The main objective of AIDA WP3 is the demonstration of the feasibility of 3D interconnection for applications in Particle Physics. This the basic goal of task WP3.2, and will be achieved by the fabrication of pixel detectors and readout electronics, interconnected by advanced 3D integration technologies. The knowledge gained with the construction of these demonstrators can be used to design and fabricate detectors for specific applications in particle physics.

This document discusses the status of the dedicated sensors that the WP3 subprojects have developed as a key element for the construction of demonstrators. As discussed in the following, sensors with a layout matching the 3D-compatible ASICs are already available to some subprojects, as they were developed in the frame of other large experiments or collaborations.

2. PIXEL SENSORS IN WP3 SUBPROJECTS

2.1. PLANS OF SUB-PROJECTS FOR PIXEL SENSORS

- **Bonn/CPPM:** Interconnection of the ATLAS FEI4 chips to sensors using bump bonding and TSVs from IZM (large diameter TSV, large interconnection pitch).
- **CERN:** Interconnection of MEDIPIX3 chips using the CEA-LETI process
- **INFN/IPHC-IRFU:** Interconnection of chips from Tezzaron/Chartered to edgeless sensors and/or CMOS sensors using an advanced interconnection process (T-MICRO or others)
- **LAL/LAPP/LPNHE/MPP:** Readout ASICs in 65nm technology interconnected using the CEA-LETI or EMFT process.
- **MPP/GLA/LAL/LIV/LPNHE:** Interconnection of ATLAS FEI4 chips to sensors using SLID interconnection and ICV (high density TSVs) from EMFT.
- **RAL/UPPSALA**
  Integration of a 2-Tier readout ASIC for a CZT pixel sensor using EMFT SLID technology and TSV including redistribution of I/O connections to the backside for a 4-side buttable device.

For a more details description of these WP3 subprojects, the report for Deliverable 3.1 can be used as a reference.

2.1.1. Bonn/CPPM

The goal of this activity is to develop a 3D integration technology applicable to the innermost pixel layer of the detector at High Luminosity LHC. Within the AIDA R&D framework WP3, we propose to produce real chip/sensor assemblies to test an interconnection technique allowing the access to the wire bond pads of the 3D structures after bonding.

For these prototypes, we propose to use planar ATLAS pixel sensor wafers and the ATLAS pixel FE-I4B electronic chip wafers. The FE-I4 chip contains readout circuitry of 26880 hybrid pixels in 80 columns by 336 rows and it is produced in the 0.13 µm feature size bulk CMOS process by IBM. The pixel pitch in FE-I4 is 50x250 µm. The dimensions, 20x19 mm^2, are the biggest among HEP chips and close to the maximum size allowed by most of the vendors. These chips are already available. Together sensors matching the footprint of the FEI4 chip have been produced and are available. Bonn will purchase them as soon as they are needed in the project.

2.1.2. CERN

The proposed project uses Medipix3 read out chips as the platform for 3D integration development. The aim of the project is to utilize an existing mature TSV technology made available by CEA-LETI as a part of their open 3D initiative.

Medipix3 wafers are already available as well as dedicated sensors.

2.1.3. INFN/IPHC-IRFU

The goal of the INFN/IPHC-IRFU proposal in the framework of the AIDA WP3 is the design and fabrication of a multi-tier pixel sensor resulting from the vertical interconnection of a CMOS readout circuit to a separate CMOS layer optimized for particle sensing and to a fully depleted edgeless or 3D detector. The project relies on CMOS sensors designed by IPHC-IRFU, fully depleted detectors provided by FBK Trento and a mixed signal readout chip designed by INFN.

The fabrication of a batch of planar pixel detectors with a high resisitvity substrate has started in May 2012 at Fondazione Bruno Kessler (FBK), Trento. Detectors are supposed to be out of the foundry by October the same year. The sensors are aimed at vertical integration tests with the Superpix1 3D front-end chip, to be submitted for fabrication with the Tezzaron/Globalfoundries technology by the end of 2012. The layout of the wafer is shown in figure 1. Besides the standard process test structures, the wafer includes:

- 32 x 128 pixel matrices, for vertical interconnection with single Superpix1 chips (with multiplicity 54);
- 32 x 128 pixel matrices with field plate for vertical interconnection with single Superpix1 chips (with multiplicity 54);
- 128 x 128 pixel matrices (with multiplicity 9);
- 128 x 128 pixel matrices with field plate (with multiplicity 9);
- 222 x 128 pixel matrices, for vertical integration with 3 Superpix1 chips (with multiplicity 7);

In all the test structures, the pixel pitch is 50 μm, as in the Superpix1 readout chip.

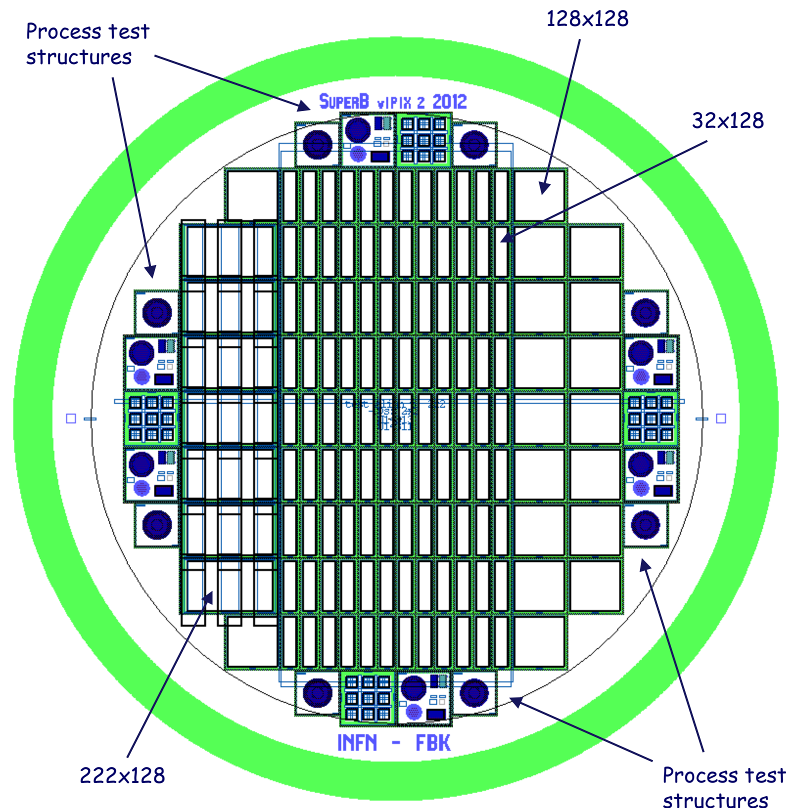

Figure 1: layout of the wafer with the pixel sensor test structures.

The test structures markers for front-end chip and sensor alignment and interconnection both with small pitch bump bonding by IZM and micro-bump bonding with T-Microtec. Backside metallization under the markers has been opened to enable the use of alignment techniques based on an infrared laser. Alignment markers can be observed in Figure 2, showing a partial view of a 32 x 128 pixel array.

Tests are in progress on active edge pixel sensors fabricated in a previous run in view of the fabrication of a new active edge detector batch, starting in March 2013.

The CMOS sensing tier will be designed by IPHC-IRFU in a CMOS process selected for its high performance sensing system, together with cost considerations. An attractive possibility is offered by the XFAB-0.35µm process, featuring a high-resistivity, around 15µm thick, epitaxial layer. An alternative possibility relying on a more radiation tolerant technology is also being considered. In both cases, the chips can be manufactured in engineering runs with restricted reticule area (so-called MLM option), thus reducing the fabrication costs substantially. The tier will therefore be around 1 cm^2 large. This sensor may profit from a prototyping step taking place in 2012 in order to finalise the choice between the two processes considered. The sensor will be fabricated in 2013.

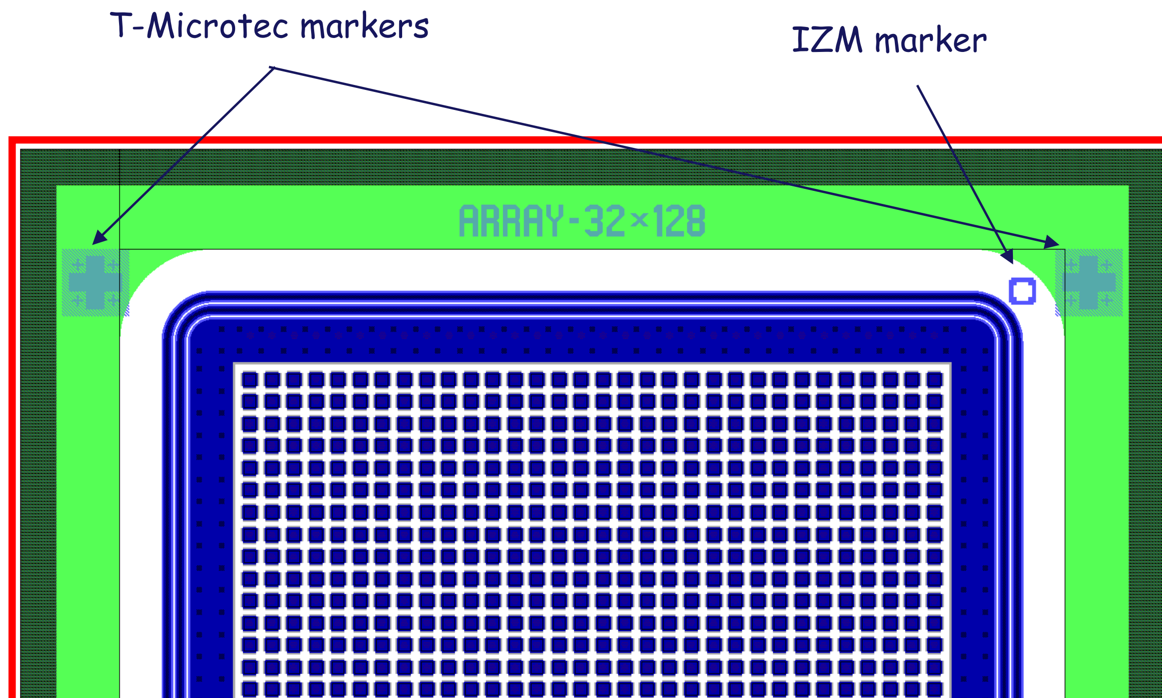

Figure 2: partial view of a 32 x 128 pixel array emphasizing the alignment markers for bump bonding with IZM and micro-bump vertical integration with T-Microtec.

2.1.4. LAL/LAPP/LPNHE/MPP

This subproject plans to exploit the challenging 65 nm CMOS technology to build a single electronic layer that houses both analogue and digital parts, interconnected to a sensor layer using via last and SLID innovative technology. This approach is similar to another proposed subproject using ATLAS FEI4 readout circuit and some synergy will be achieved in terms of SLID evaluation and electrical tests. It is planned to produce sensors 2013-2014 in n-in-p technology and 150µm thickness.

2.1.5. MPP/GLA/LAL/LIV/LPNHE

This activity regards the interconnection of the new FE-I4 ATLAS chip, designed for the upgrades of the ATLAS pixel system, to a compatible sensor by using 3D technologies developed by the Fraunhofer Institute EMFT. We will use the FE-I4 chip in this demonstrator because it is one of the last generation read-out chips for pixel sensors in high energy physics and it will probably evolve in the following years into a 3D compliant version, for the future upgrades of the ATLAS pixel system beyond IBL.

There are several sources for sensors matching the FEI4 footprint:

1) Production of sensors at CIS Erfurt: CiS will upgrade its production line from 4” to 6” wafers, with the possibility to start a test production on 6” wafers in second half of 2012. We are planning a sensor production on 6” wafers, with a layout compatible with the SLID interconnection, to be carried out at CiS (Erfurt). The foreseen technology to be employed is n-in-p, that has already been proven to work up to fluences of 10^{16} cm^{-2} 1 MeV n_{eq} by using FE-I3 and FE-I4 modules with n-in-p sensors from CiS and MPP-HLL productions.

   The wafer procurement has been completed with the purchase of 50 FZ p-type wafers of high resistivity (>10 KΩ cm) that have been successively double-side polished at Rockwood Wafer Reclaim.

   A preliminary wafer layout of the sensors has been prepared. Each wafer hosts 10 sensors with a geometry targeted at FE-I4 Single Chip Modules. Their arrangement is compatible with the SLID interconnection in the chip to wafer approach. This sensor production will be carried out within the framework of the RD50 CERN Collaboration, starting with a batch of 12 wafers.

   A sketch of the preliminary wafer layout is reported in Fig. 3a together with a detail of a corner of a FE-I4 sensor in Fig. 3b.

2) Production in our own semiconductor lab: Sensors (n-in-p) with a thickness of 150µm on SOI material have already been produced. They have already been bump bonded to FEI4 and successfully tested (even after irradiation). However, no wafer is left which could be used for AIDA. However, a new lot can be produced within a reasonable short time (~ 3 months).

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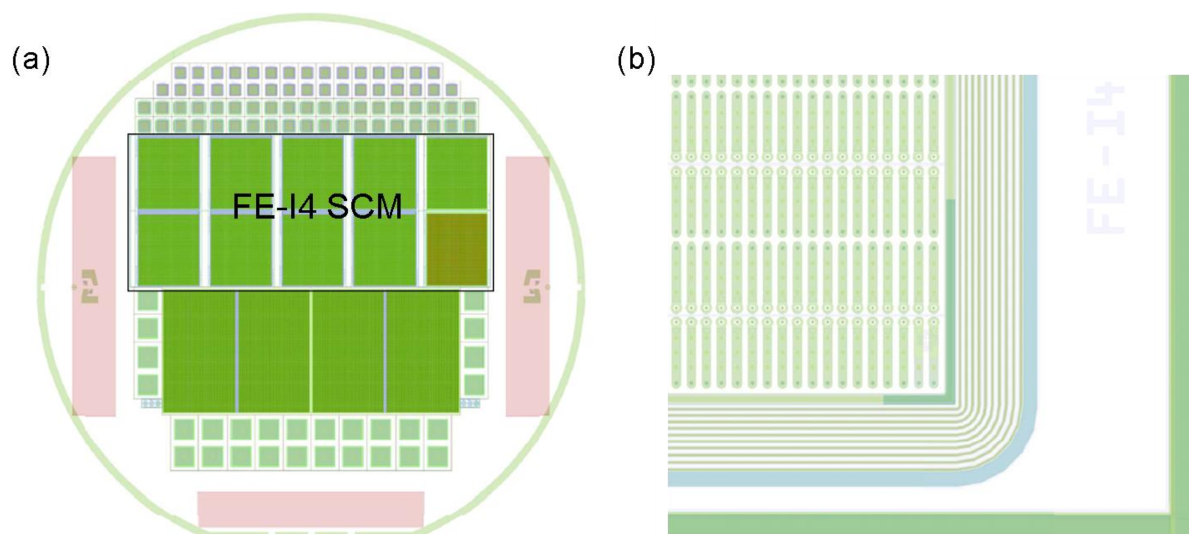

Figure 3: a) Preliminary layout of the 6” sensor wafer designed for the SLID interconnection to the FE-I4 chips; b) Detail of a corner of a FE-I4 sensor in the n-in-p technology.

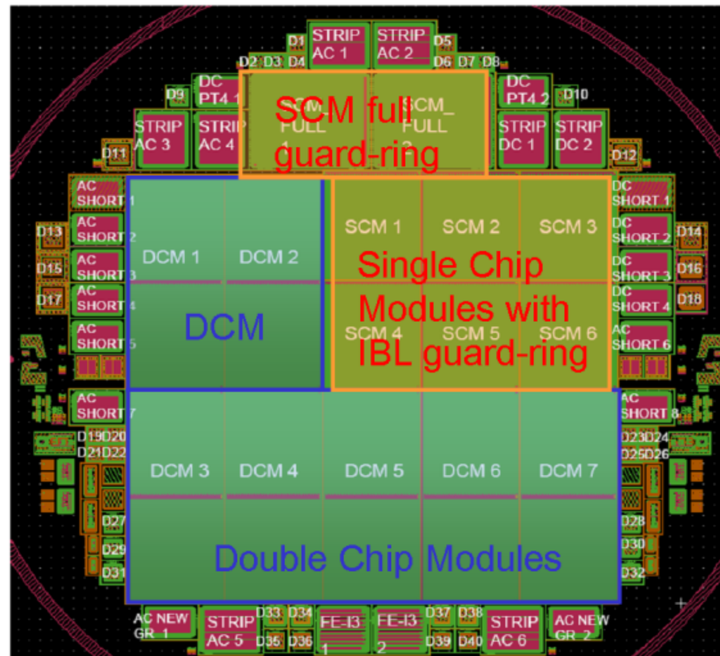

Figure 4: Layout of wafer with FEI4 compatible sensors produced at MPI. The sensors are 150µm thick. It contains variants with different guard ring structures.

2.1.6. RAL/Uppsala

These partners will look at two activities: one is for the construction of a full 3DIC stacked pixel ASIC with pixels interconnected between 2 layers, and the second is for an activity to redistribute I/O connections to the back of an ASIC to enable 4-side butted pixel detectors.

A 40 x 40 pixel readout ASIC has been built based on an existing 80 x 80 pixel Hexitec CZT readout circuitry. Since this projects produces a 2-tier ASIC with SLID interconnection between the two ASIC tiers, no dedicated sensor is needed at this stage.

3. CONCLUSION

This document presented a summary of the plans that AIDA WP3 will pursue with the goal of procuring silicon sensors qualifying 3D integration technologies and of enabling the network to access them for the design of advanced pixel systems for tracking and vertexing in high energy physics experiments. A summary is provided in Table 1. Dedicated sensor production has started with two subprojects, one will follow soon with a second production. Both WP3 coordinators and AIDA management will monitor closely the production of these sensors. For the other subprojects dedicated sensors will be available from other projects or are not needed within the scope of the subproject.

Project name	Sensors	Availability status
Bonn/CPPM	ATLAS pixel sensors	Available
CERN	VTT MEDIPIX3 sensors	Available
INFN/IPHC-IRFU	FBK planar sensors FBK active edge sensors CMOS sensors	4Q 2012 4Q 2013 4Q 2013
LAL/LAPP/LPNHE/MPP	150µm p-in-n	2Q 2014
MPP/GLA/LAL/LIV/LPNHE	CIS sensors MPP sensors	1Q 2013 3Q 2013
RAL/Uppsala	-	No sensors needed

Table 1. Summary of the sensor availability for the fabrication of 3D pixel demonstrators.

4. REFERENCES